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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

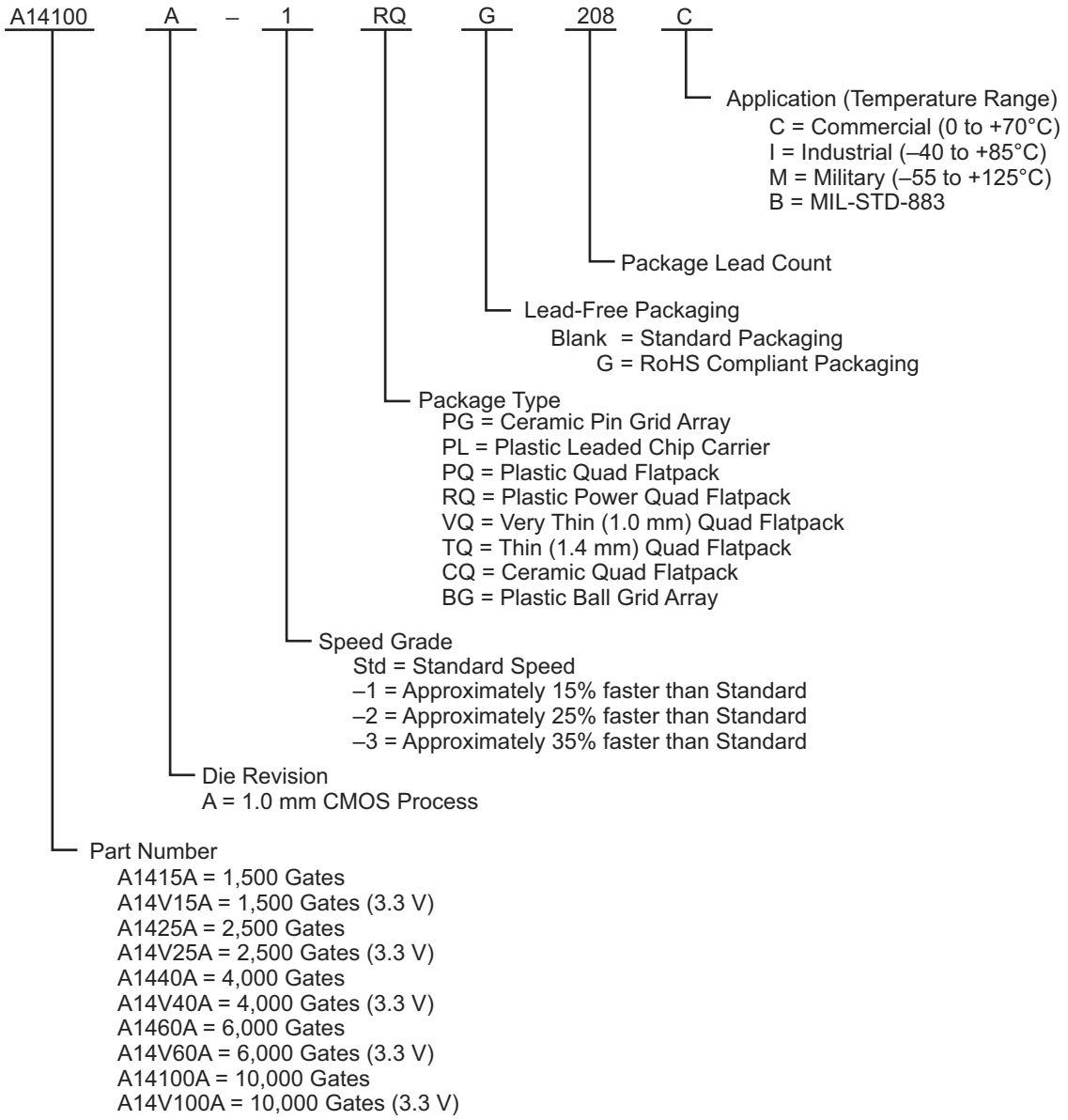
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 310 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 70 |
| Number of Gates | 2500 |
| Voltage - Supply | 3V ~ 3.6V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/a14v25a-pl84c |

# Ordering Information




Notes:

1. *The –2 and –3 speed grades have been discontinued.*
2. *The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.*
3. *The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.*
4. *Military Grade devices are no longer available for the A1440A device.*
5. *For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:*
   *PDN March 2001*
   *PDN 0104*
   *PDN 0203*
   *PDN 0604*
   *PDN 1004*

# Product Plan

| Device/Package | Speed Grade[1] | | | | Application[1] | | | |
|---|---|---|---|---|---|---|---|---|
| | Std. | –1 | –2 | –3 | C | I | M | B |
| **A1415A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | ✓ | D | D | ✓ | ✓ | ✓ | – |
| 100-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | ✓ | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | ✓ | D | D | ✓ | ✓ | ✓ | – |
| 100-Pin Ceramic Pin Grid Array (CPGA) | D | D | D | D | D | – | – | – |
| **A14V15A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | – | – | – | ✓ | – | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | – | – | – | ✓ | – | – | – |
| **A1425A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | ✓ | D | D | ✓ | ✓ | | |
| 100-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 132-Pin Ceramic Quad Flatpack (CQFP) | ✓ | ✓ | – | – | ✓ | – | ✓ | ✓ |
| 133-Pin Ceramic Pin Grid Array (CPGA) | D | D | D | D | D | – | D | D |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| **A14V25A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | – | – | – | ✓ | – | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | – | – | – | ✓ | – | – | – |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | – | – | – | ✓ | – | – | – |
| **A1440A Device** | | | | | | | | |
| 84-Pin Plastic Leaded Chip Carrier (PLCC) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 100-Pin Very Thin Quad Flatpack (VQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 160-Pin Plastic Quad Flatpack (PQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |
| 175-Pin Ceramic Pin Grid Array (CPGA) | D | D | D | D | D | – | – | – |
| 176-Pin Thin Quad Flatpack (TQFP) | ✓ | ✓ | D | D | ✓ | ✓ | – | – |

*Notes:*

1. *Applications:*
   *C = Commercial*
   *I = Industrial*
   *M = Military*
2. *Commercial only*

*Availability:*
*✓ = Available*
*P = Planned*
*– = Not planned*
*D = Discontinued*

*Speed Grade:*
*–1 = Approx. 15% faster than Std.*
*–2 = Approx. 25% faster than Std.*
*–3 = Approx. 35% faster than Std.*
*(–2 and –3 speed grades have been discontinued.)*

## ACT 3 Family Overview



## Detailed Specifications



## Package Pin Assignments



## Datasheet Information

## A1425A, A14V25A Timing Characteristics (continued)

***Table 2-23* • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module Input Propagation Delays | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{INY}$ | Input Data Pad to Y | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| $t_{ICKY}$ | Input Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCKY}$ | Output Reg IOCLK Pad to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{ICLRY}$ | Input Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| $t_{OCLRY}$ | Output Asynchronous Clear to Y | | 4.7 | | 5.3 | | 6.0 | | 7.0 | | 9.2 | ns |
| **Predicted Input Routing Delays[2]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **I/O Module Sequential Timing (wrt IOCLK pad)** | | | | | | | | | | | | |
| $t_{INH}$ | Input F-F Data Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input F-F Data Setup | 1.8 | | 2.0 | | 2.3 | | 2.7 | | 3.0 | | ns |
| $t_{IDEH}$ | Input Data Enable Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IDESU}$ | Input Data Enable Setup | 5.8 | | 6.5 | | 7.5 | | 8.6 | | 8.6 | | ns |
| $t_{OUTH}$ | Output F-F Data hold | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{OUTSU}$ | Output F-F Data Setup | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | | ns |
| $t_{ODEH}$ | Output Data Enable Hold | 0.3 | | 0.4 | | 0.4 | | 0.5 | | 0.5 | | ns |
| $f_{ODESU}$ | Output Data Enable Setup | 1.3 | | 1.5 | | 1.7 | | 2.0 | | 2.0 | | ns |

*Notes: **

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1425A, A14V25A Timing Characteristics (continued)

**Table 2-24 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| I/O Module – TTL Output Timing[1] | | –3 Speed[2] | | –2 Speed[2] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DHS}$ | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 6.5 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 7.5 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 11.3 | | 11.3 | | 13.5 | | 15.0 | | 19.5 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| **I/O Module – CMOS Output Timing[1]** | | | | | | | | | | | | |
| $t_{DHS}$ | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 6.7 | | 7.5 | | 8.5 | | 10.0 | | 13.0 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 6.7 | | 7.5 | | 9.0 | | 10.0 | | 13.0 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 8.9 | | 8.9 | | 10.7 | | 11.8 | | 15.3 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 13.0 | | 13.0 | | 15.6 | | 17.3 | | 22.5 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

*Notes: **

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

## A1440A, A14V40A Timing Characteristics (continued)

*Table 2-29* • **A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

| Dedicated (hardwired) I/O Clock Network | | –3 Speed[1] | | –2 Speed[1] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter/Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | |
| $t_{IOCKH}$ | Input Low to High (pad to I/O module input) | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{IOPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IPOWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IOSAPW}$ | Minimum Asynchronous Pulse Width | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{IOCKSW}$ | Maximum Skew | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | ns |
| $t_{IOP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{IOMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Dedicated (hardwired) Array Clock** | | | | | | | | | | | | |
| $t_{HCKH}$ | Input Low to High (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| $t_{HCKL}$ | Input High to Low (pad to S-module input) | | 3.0 | | 3.4 | | 3.9 | | 4.5 | | 5.5 | ns |
| $t_{HPWH}$ | Minimum Pulse Width High | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{HPWL}$ | Minimum Pulse Width Low | 1.9 | | 2.4 | | 3.3 | | 3.8 | | 4.8 | | ns |
| $t_{HCKSW}$ | Delta High to Low, Low Slew | | 0.3 | | 0.3 | | 0.3 | | 0.3 | | 0.3 | ns |
| $t_{HP}$ | Minimum Period | 4.0 | | 5.0 | | 6.8 | | 8.0 | | 10.0 | | ns |
| $f_{HMAX}$ | Maximum Frequency | | 250 | | 200 | | 150 | | 125 | | 100 | MHz |
| **Routed Array Clock Networks** | | | | | | | | | | | | |
| $t_{RCKH}$ | Input Low to High (FO = 64) | | 3.7 | | 4.1 | | 4.7 | | 5.5 | | 9.0 | ns |
| $t_{RCKL}$ | Input High to Low (FO = 64) | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 9.0 | ns |
| $t_{RPWH}$ | Min. Pulse Width High (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| $t_{RPWL}$ | Min. Pulse Width Low (FO = 64) | 3.3 | | 3.8 | | 4.2 | | 4.9 | | 6.5 | | ns |
| $t_{RCKSW}$ | Maximum Skew (FO = 128) | | 0.7 | | 0.8 | | 0.9 | | 1.0 | | 1.0 | ns |
| $t_{RP}$ | Minimum Period (FO = 64) | 6.8 | | 8.0 | | 8.7 | | 10.0 | | 13.4 | | ns |
| $f_{RMAX}$ | Maximum Frequency (FO = 64) | | 150 | | 125 | | 115 | | 100 | | 75 | MHz |
| **Clock-to-Clock Skews** | | | | | | | | | | | | |
| $t_{IOHCKSW}$ | I/O Clock to H-Clock Skew | 0.0 | 1.7 | 0.0 | 1.8 | 0.0 | 2.0 | 0.0 | 2.2 | 0.0 | 3.0 | ns |
| $t_{IORCKSW}$ | I/O Clock to R-Clock Skew (FO = 64)<br>(FO = 144) | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 3.0<br>3.0 | ns |
| $t_{HRCKSW}$ | H-Clock to R-Clock Skew (FO = 64)<br>(FO = 144) | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | 0.0<br>0.0 | 1.0<br>3.0 | ns |

*Notes:*

1. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
2. *Delays based on 35 pF loading.*

## A1460A, A14V60A Timing Characteristics

**Table 2-30 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C[1]**

| Logic Module Propagation Delays[2] | | –3 Speed[3] | | –2 Speed [3] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | Internal Array Module | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CO}$ | Sequential Clock to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| $t_{CLR}$ | Asynchronous Clear to Q | | 2.0 | | 2.3 | | 2.6 | | 3.0 | | 3.9 | ns |
| **Predicted Routing Delays[4]** | | | | | | | | | | | | |
| $t_{RD1}$ | FO = 1 Routing Delay | | 0.9 | | 1.0 | | 1.1 | | 1.3 | | 1.7 | ns |
| $t_{RD2}$ | FO = 2 Routing Delay | | 1.2 | | 1.4 | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{RD3}$ | FO = 3 Routing Delay | | 1.4 | | 1.6 | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{RD4}$ | FO = 4 Routing Delay | | 1.7 | | 1.9 | | 2.2 | | 2.5 | | 3.3 | ns |
| $t_{RD8}$ | FO = 8 Routing Delay | | 2.8 | | 3.2 | | 3.6 | | 4.2 | | 5.5 | ns |
| **Logic Module Sequential Timing** | | | | | | | | | | | | |
| $t_{SUD}$ | Flip-Flop Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Flip-Flop Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUD}$ | Latch Data Input Setup | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.8 | | ns |
| $t_{HD}$ | Latch Data Input Hold | 0.0 | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WASYN}$ | Asynchronous Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_{WCLKA}$ | Flip-Flop Clock Pulse Width | 2.4 | | 3.2 | | 3.8 | | 4.8 | | 6.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 5.0 | | 6.8 | | 8.0 | | 10.0 | | 13.4 | | ns |
| $f_{MAX}$ | Flip-Flop Clock Frequency | | 200 | | 150 | | 125 | | 100 | | 75 | MHz |

*Notes:*

1. *VCC = 3.0 V for 3.3 V specifications.*
2. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn} + t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
3. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*
4. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A14100A, A14V100A Timing Characteristics (continued)

**Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, $T_J$ = 70°C**

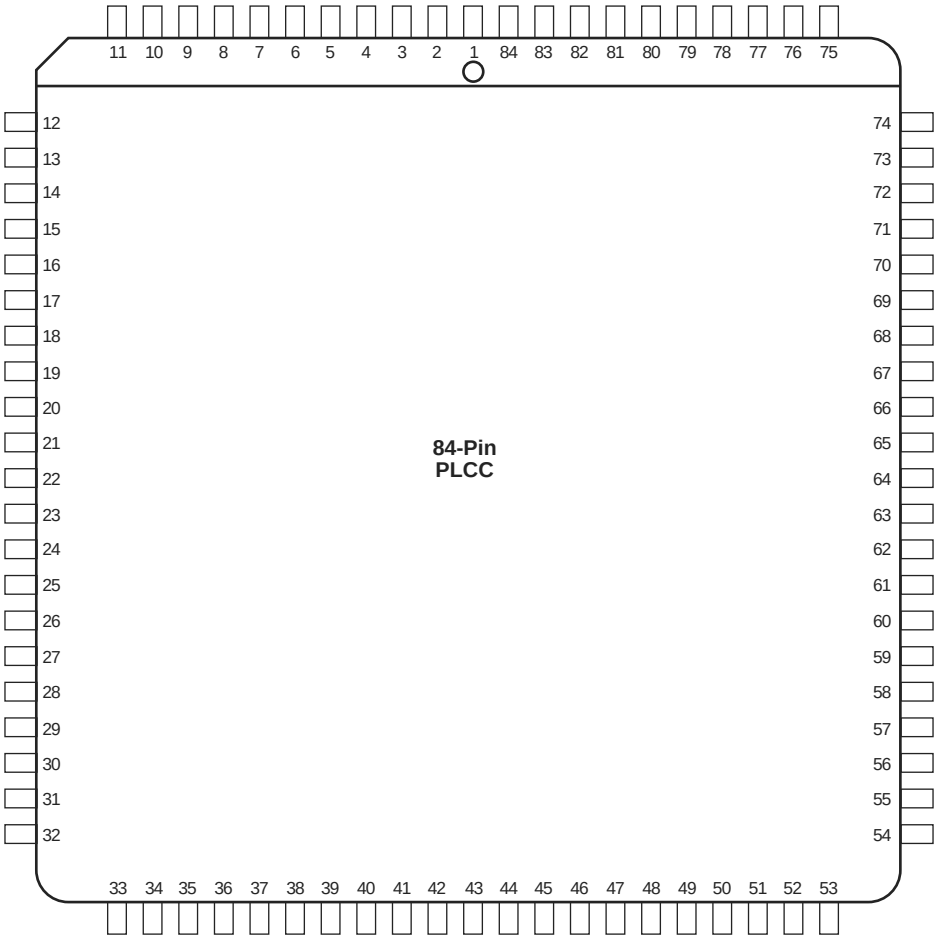
| I/O Module – TTL Output Timing[1] | | –3 Speed[2] | | –2 Speed[2] | | –1 Speed | | Std. Speed | | 3.3 V Speed[1] | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter/Description | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{DHS}$ | Data to Pad, High Slew | | 5.0 | | 5.6 | | 6.4 | | 7.5 | | 9.8 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 4.0 | | 4.5 | | 5.1 | | 6.0 | | 7.8 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 8.0 | | 9.0 | | 10.2 | | 12.0 | | 15.6 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 9.5 | | 9.5 | | 10.5 | | 12.0 | | 15.6 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 12.8 | | 12.8 | | 15.3 | | 17.0 | | 22.1 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.02 | | 0.02 | | 0.03 | | 0.03 | | 0.04 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.05 | | 0.05 | | 0.06 | | 0.07 | | 0.09 | ns/pF |
| **I/O Module – CMOS Output Timing[1]** | | | | | | | | | | | | |
| $t_{DHS}$ | Data to Pad, High Slew | | 6.2 | | 7.0 | | 7.9 | | 9.3 | | 12.1 | ns |
| $t_{DLS}$ | Data to Pad, Low Slew | | 11.7 | | 13.1 | | 14.9 | | 17.5 | | 22.8 | ns |
| $t_{ENZHS}$ | Enable to Pad, Z to H/L, High Slew | | 5.2 | | 5.9 | | 6.6 | | 7.8 | | 10.1 | ns |
| $t_{ENZLS}$ | Enable to Pad, Z to H/L, Low Slew | | 8.9 | | 10.0 | | 11.3 | | 13.3 | | 17.3 | ns |
| $t_{ENHSZ}$ | Enable to Pad, H/L to Z, High Slew | | 8.0 | | 9.0 | | 10.0 | | 12.0 | | 15.6 | ns |
| $t_{ENLSZ}$ | Enable to Pad, H/L to Z, Low Slew | | 7.4 | | 8.3 | | 9.4 | | 11.0 | | 14.3 | ns |
| $t_{CKHS}$ | IOCLK Pad to Pad H/L, High Slew | | 10.4 | | 10.4 | | 12.4 | | 13.8 | | 17.9 | ns |
| $t_{CKLS}$ | IOCLK Pad to Pad H/L, Low Slew | | 14.5 | | 14.5 | | 17.4 | | 19.3 | | 25.1 | ns |
| $d_{TLHHS}$ | Delta Low to High, High Slew | | 0.04 | | 0.04 | | 0.05 | | 0.06 | | 0.08 | ns/pF |
| $d_{TLHLS}$ | Delta Low to High, Low Slew | | 0.07 | | 0.08 | | 0.09 | | 0.11 | | 0.14 | ns/pF |
| $d_{THLHS}$ | Delta High to Low, High Slew | | 0.03 | | 0.03 | | 0.03 | | 0.04 | | 0.05 | ns/pF |
| $d_{THLLS}$ | Delta High to Low, Low Slew | | 0.04 | | 0.04 | | 0.04 | | 0.05 | | 0.07 | ns/pF |

*Notes: **

1. *Delays based on 35 pF loading.*
2. *The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at http://www.microsemi.com/soc/support/notifications/default.aspx#pdn.*

# 3 – Package Pin Assignments

## PL84

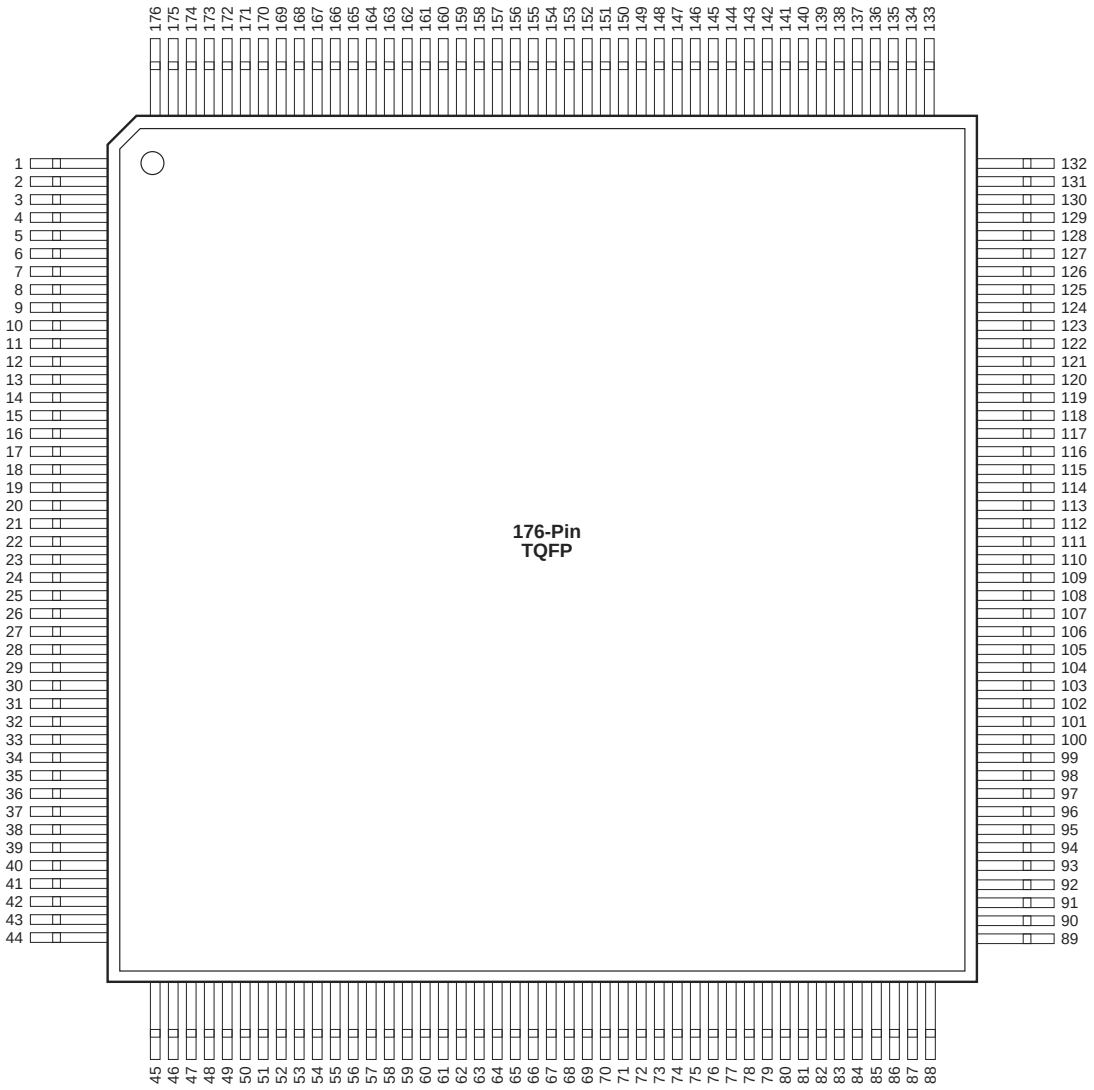



*Note: This is the top view of the package.*

### *Note*

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

# TQ176

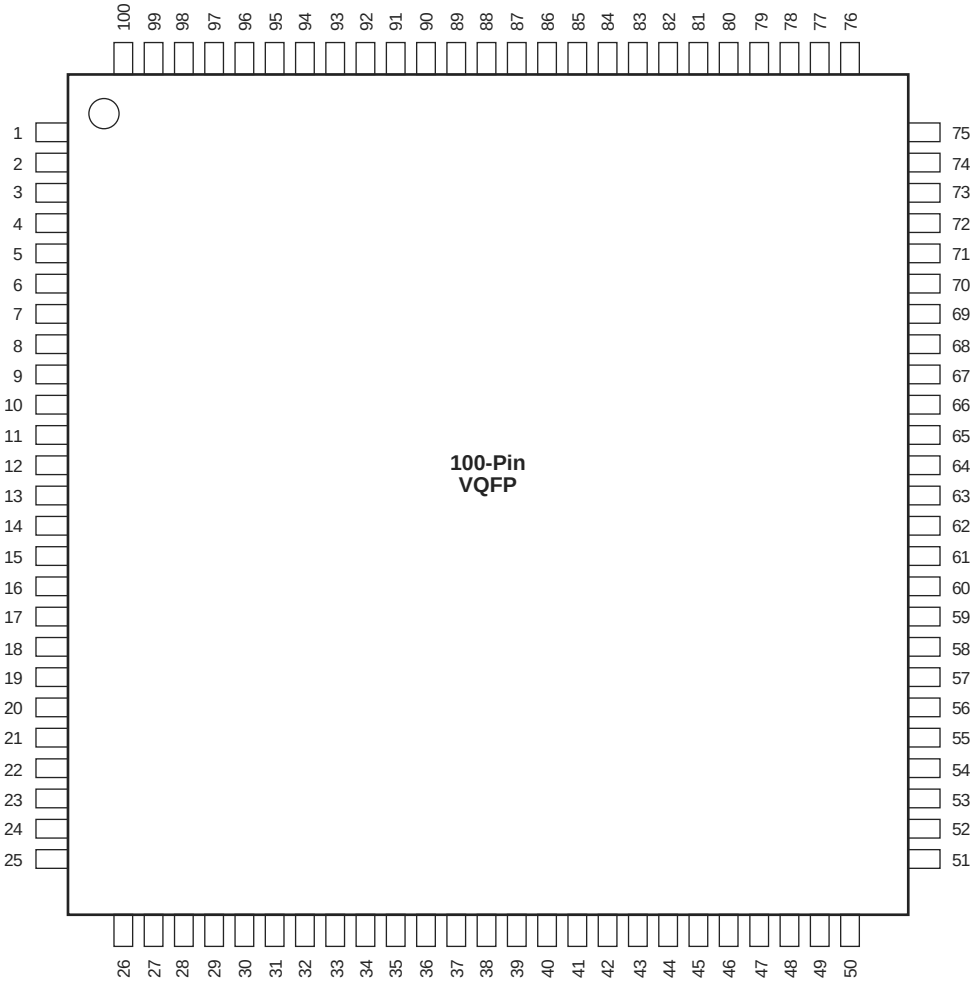



*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

# VQ100




*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| VQ100 | | | |
|---|---|---|---|
| **Pin Number** | **A1415, A14V15 Function** | **A1425, A14V25 Function** | **A1440, A14V40 Function** |
| 1 | GND | GND | GND |
| 2 | SDI, I/O | SDI, I/O | SDI, I/O |
| 7 | MODE | MODE | MODE |
| 8 | VCC | VCC | VCC |
| 9 | GND | GND | GND |
| 20 | VCC | VCC | VCC |
| 21 | NC | I/O | I/O |
| 34 | PRB, I/O | PRB, I/O | PRB, I/O |
| 35 | VCC | VCC | VCC |
| 36 | GND | GND | GND |
| 37 | VCC | VCC | VCC |
| 39 | HCLK, I/O | HCLK, I/O | HCLK, I/O |
| 49 | SDO | SDO | SDO |
| 50 | IOPCL, I/O | IOPCL, I/O | IOPCL, I/O |
| 51 | GND | GND | GND |
| 57 | VCC | VCC | VCC |
| 58 | VCC | VCC | VCC |
| 67 | VCC | VCC | VCC |
| 68 | GND | GND | GND |
| 69 | GND | GND | GND |
| 74 | NC | I/O | I/O |
| 75 | IOCLK, I/O | IOCLK, I/O | IOCLK, I/O |
| 87 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 88 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 89 | VCC | VCC | VCC |
| 90 | VCC | VCC | VCC |
| 91 | GND | GND | GND |
| 92 | PRA, I/O | PRA, I/O | PRA, I/O |
| 93 | NC | I/O | I/O |
| 100 | DCLK, I/O | DCLK, I/O | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

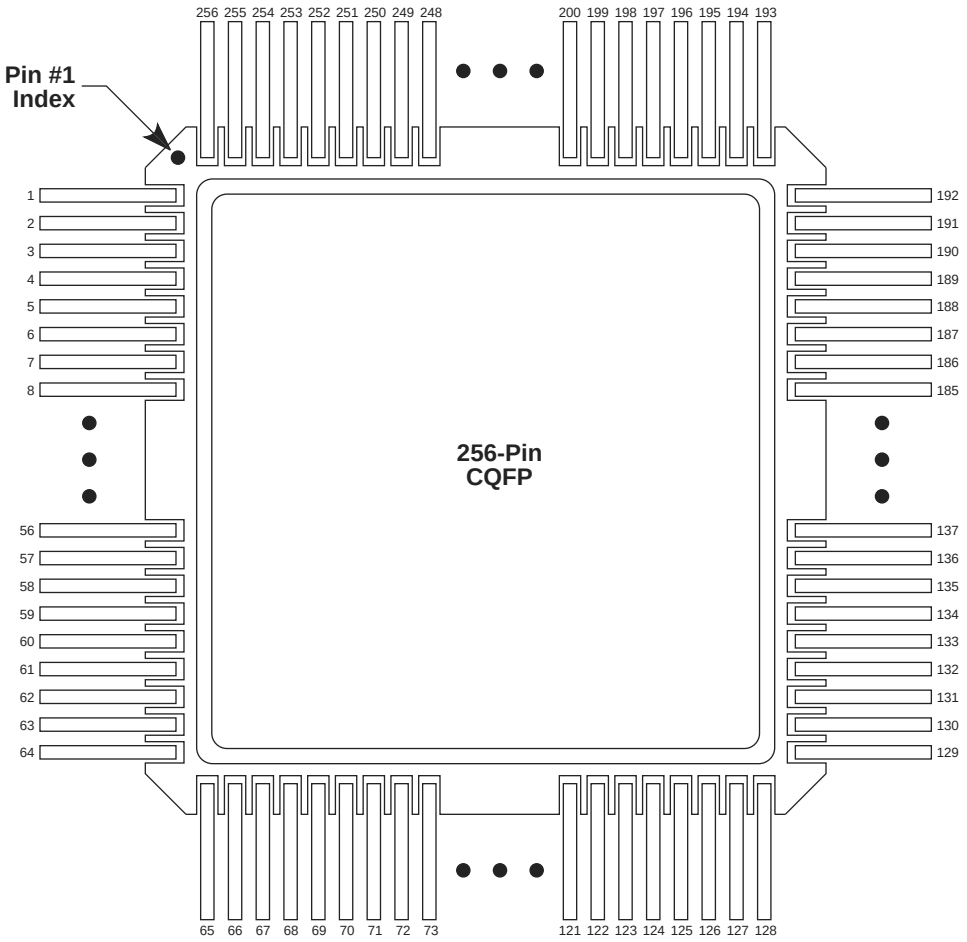
| CQ132 | |
|---|---|
| **Pin Number** | **A1425 Function** |
| 1 | NC |
| 2 | GND |
| 3 | SDI, I/O |
| 9 | MODE |
| 10 | GND |
| 11 | VCC |
| 22 | VCC |
| 26 | GND |
| 27 | VCC |
| 34 | NC |
| 36 | GND |
| 42 | GND |
| 43 | VCC |
| 48 | PRB, I/O |
| 50 | HCLK, I/O |
| 58 | GND |
| 59 | VCC |
| 63 | SDO |
| 64 | IOPCL, I/O |
| 65 | GND |
| 66 | NC |

| CQ132 | |
|---|---|
| **Pin Number** | **A1425 Function** |
| 67 | NC |
| 74 | GND |
| 75 | VCC |
| 78 | VCC |
| 89 | VCC |
| 90 | GND |
| 91 | VCC |
| 92 | GND |
| 98 | IOCLK, I/O |
| 99 | NC |
| 100 | NC |
| 101 | GND |
| 106 | GND |
| 107 | VCC |
| 116 | CLKA, I/O |
| 117 | CLKB, I/O |
| 118 | PRA, I/O |
| 122 | GND |
| 123 | VCC |
| 131 | DCLK, I/O |
| 132 | NC |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# CQ256




*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

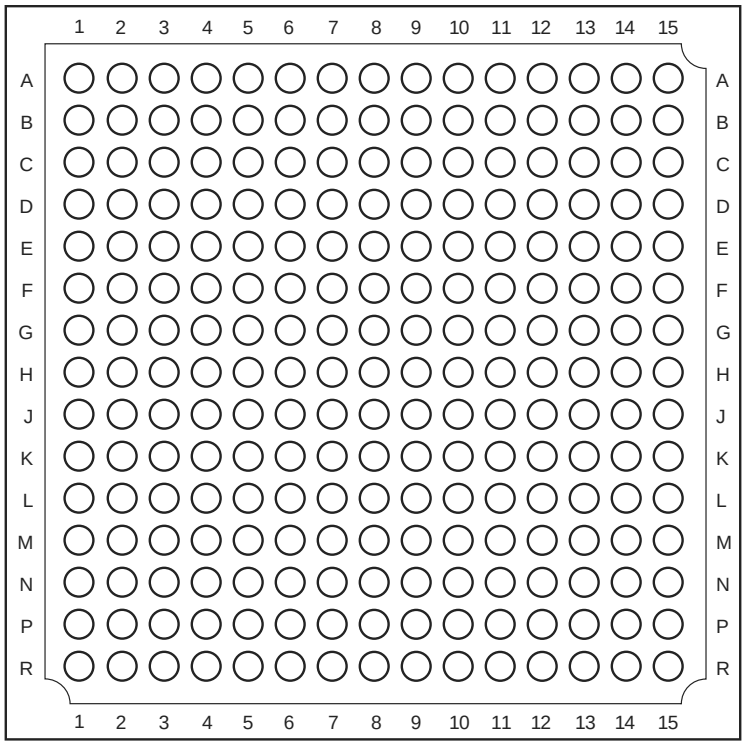
| CQ256 | |
|---|---|
| **Pin Number** | **A14100 Function** |
| 1 | GND |
| 2 | SDI, I/O |
| 11 | MODE |
| 28 | VCC |
| 29 | GND |
| 30 | VCC |
| 31 | GND |
| 46 | VCC |
| 59 | GND |
| 90 | PRB, I/O |
| 91 | GND |
| 92 | VCC |
| 93 | GND |
| 94 | VCC |
| 96 | HCLK, I/O |
| 110 | GND |
| 126 | SDO |
| 127 | IOPCL, I/O |
| 128 | GND |

| CQ256 | |
|---|---|
| **Pin Number** | **A14100 Function** |
| 141 | VCC |
| 158 | GND |
| 159 | VCC |
| 160 | GND |
| 161 | VCC |
| 174 | VCC |
| 175 | GND |
| 176 | GND |
| 188 | IOCLK, I/O |
| 189 | GND |
| 219 | CLKA, I/O |
| 220 | CLKB, I/O |
| 221 | VCC |
| 222 | GND |
| 223 | VCC |
| 224 | GND |
| 225 | PRA, I/O |
| 240 | GND |
| 256 | DCLK, I/O |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

# BG225




*Note: This is the top view.*

## Note

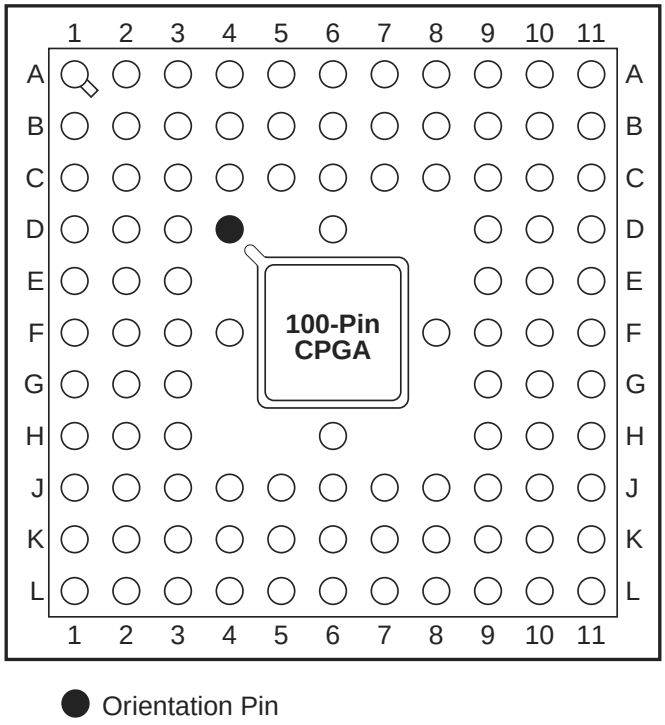
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| BG225 | |
|---|---|
| **A1460 Function** | **Location** |
| CLKA or I/O | C8 |
| CLKB or I/O | B8 |
| DCLK or I/O | B2 |
| GND | A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15 |
| HCLK or I/O | P9 |
| IOCLK or I/O | B14 |
| IOPCL or I/O | P14 |
| MODE | D1 |
| NC | A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14 |
| PRA or I/O | A7 |
| PRB or I/O | L7 |
| SDI or I/O | D4 |
| SDO | N13 |
| VCC | A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

# PG100




*Note: This is the top view.*

## Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

| PG100 | |
|---|---|
| **A1415 Function** | **Location** |
| CLKA or I/O | C7 |
| CLKB or I/O | D6 |
| DCLK or I/O | C4 |
| GND | C3, C6, C9, E9, F3, F9, J3, J6, J8, J9 |
| HCLK or I/O | H6 |
| IOCLK or I/O | C10 |
| IOPCL or I/O | K9 |
| MODE | C2 |
| PRA or I/O | A6 |
| PRB or I/O | L3 |
| SDI or I/O | B3 |
| SDO | L9 |
| VCC | B6, B10, E11, F2, F10, G2, K2, K6, K10 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

| PG175 | |
|---|---|
| **A1440 Function** | **Location** |
| CLKA or I/O | C9 |
| CLKB or I/O | A9 |
| DCLK or I/O | D5 |
| GND | D4, D8, D11, D12, E4, E14, H4, H12, L4, L12, M4, M8, M12 |
| HCLK or I/O | R8 |
| IOCLK or I/O | E12 |
| IOPCL or I/O | P13 |
| MODE | F3 |
| NC | A1, A2, A15, B2, B3, P2, P14, R1, R2, R14, R15 |
| PRA or I/O | B8 |
| PRB or I/O | R7 |
| SDI or I/O | D3 |
| SDO | N12 |
| VCC | C3, C8, C13, E15, H3, H13, L1, L14, N3, N8, N13 |

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG175 package has been discontinued.