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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	310
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	83
Number of Gates	2500
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a14v25a-vq100c">https://www.e-xfl.com/product-detail/microsemi/a14v25a-vq100c</a>

## Ordering Information



### Notes:

1. The -2 and -3 speed grades have been discontinued.
2. The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
3. The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
4. Military Grade devices are no longer available for the A1440A device.
5. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:  
PDN March 2001  
PDN 0104  
PDN 0203  
PDN 0604  
PDN 1004

## Plastic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PL84	PQ100	PQ160	PQ/RQ208	VQ100	TQ176	BG225*	BG313
A1415	200	1500	70	80	–	–	80	–	–	–
A1425	310	2500	70	80	100	–	83	–	–	–
A1440	564	4000	70	–	131	–	83	140	–	–
A1460	848	6000	–	–	131	167	–	151	168	–
A14100	1377	10000	–	–	–	175	–	–	–	228

Note: \*Discontinued

## Hermetic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PG100*	PG133*	PG175*	PG207	PG257	CQ132	CQ196	CQ256
A1415	200	1500	80	–	–	–	–	–	–	–
A1425	310	2500	–	100	–	–	–	100	–	–
A1440	564	4000	–	–	140	–	–	–	–	–
A1460	848	6000	–	–	–	168	–	–	168	–
A14100	1377	10000	–	–	–	–	228	–	–	228

Note: \*Discontinued

Contact your local Microsemi SoC Products Group (formerly Actel) representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

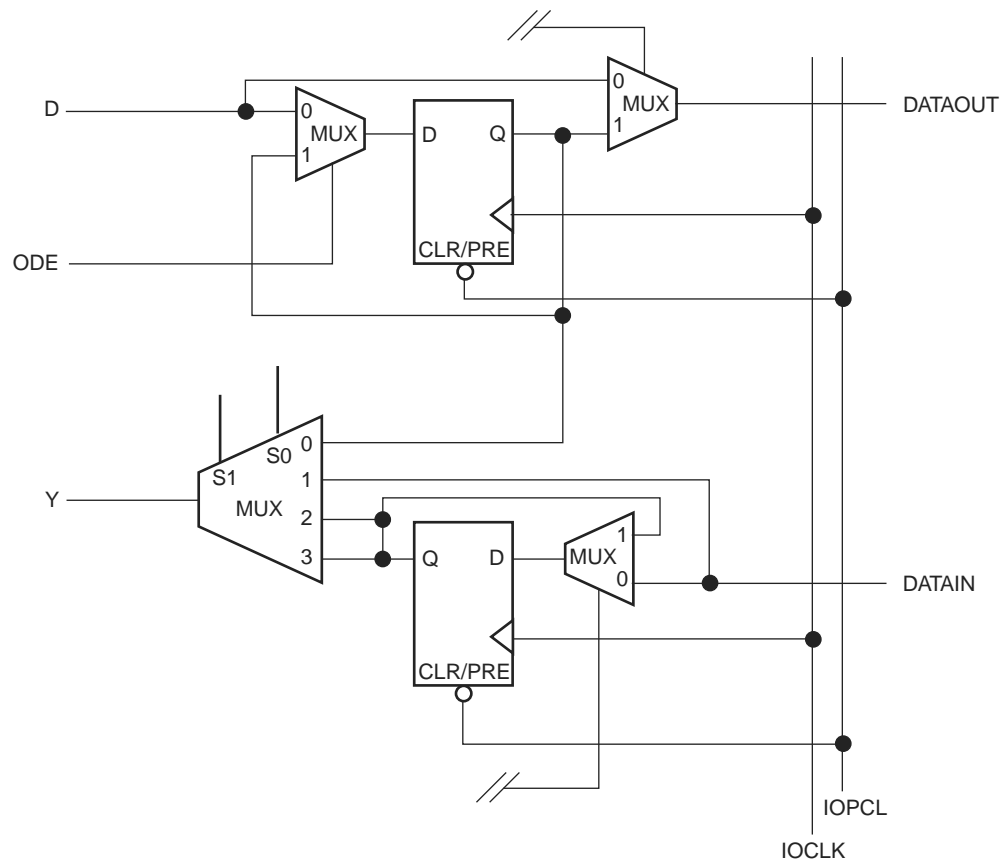
The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Designer Series Development System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLKA, CLKB, or HCLK. The C-module and S-module functional descriptions are shown in Figure 2-2 and Figure 2-3 on page 2-2. The clock selection is determined by a multiplexer select at the clock input to the S-module.

## I/Os

### I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. The I/O module schematic is shown in Figure 4. The signals DataIn and DataOut connect to the I/O pad driver.



**Figure 2-4 • Functional Diagram for I/O Module**

Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

## Antifuse Connections

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.)

Table 2-1 shows four types of antifuses.

**Table 2-1 • Antifuse Types**

Type	Description
XF	Horizontal-to-vertical connection
HF	Horizontal-to-horizontal connection
VF	Vertical-to-vertical connection
FF	"Fast" vertical connection

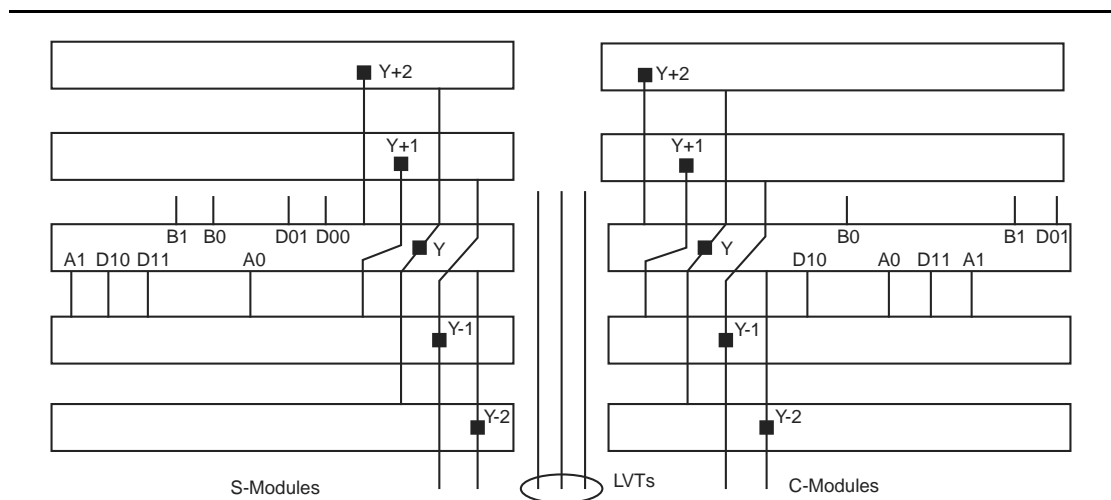
Examples of all four types of connections are shown in Figure 2-7 on page 2-6 and Figure 2-8 on page 2-6.

## Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

### Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below, as shown in Figure 2-9.



**Figure 2-9 • Logic Module Routing Interface**

## Package Thermal Characteristics

The device junction to case thermal characteristic is  $\theta_{jc}$ , and the junction to ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 175-pin package at commercial temperature and still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ °C/W}} = \frac{150\text{°C} - 70\text{°C}}{25\text{°C/W}} = 3.2 \text{ W}$$

EQ 2

**Table 2-8 • Package Thermal Characteristics**

Package Type*	Pin Count	$\theta_{jc}$	$\theta_{ja}$ Still Air	$\theta_{ja}$ 300 ft./min.	Units
Ceramic Pin Grid Array	100	20	35	17	°C/W
	133	20	30	15	°C/W
	175	20	25	14	°C/W
	207	20	22	13	°C/W
	257	20	15	8	°C/W
Ceramic Quad Flatpack	132	13	55	30	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W
Plastic Quad Flatpack	100	13	51	40	°C/W
	160	10	33	26	°C/W
	208	10	33	26	°C/W
Very Thin Quad Flatpack	100	12	43	35	°C/W
Thin Quad Flatpack	176	11	32	25	°C/W
Power Quad Flatpack	208	0.4	17	13	°C/W
Plastic Leaded Chip Carrier	84	12	37	28	°C/W
Plastic Ball Grid Array	225	10	25	19	°C/W
	313	10	23	17	°C/W

Note: Maximum power dissipation in still air:

PQ160 = 2.4 W

PQ208 = 2.4 W

PQ100 = 1.6 W

VQ100 = 1.9 W

TQ176 = 2.5 W

PL84 = 2.2 W

RQ208 = 4.7 W

BG225 = 3.2 W

BG313 = 3.5 W

## Power Dissipation

$$P = [ICC_{\text{standby}} + I_{\text{active}}] * VCC * IOL * VOL * N + IOH * (VCC - VOH) * M$$

EQ 3

where:

ICC standby is the current flowing when no inputs or outputs are changing

Iactive is the current flowing due to CMOS switching.

IOL and IOH are TTL sink/source current.

VOL and VOH are TTL level output voltages.

N is the number of outputs driving TTL loads to VOL.

M equals the number of outputs driving TTL loads to VOH.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

## Static Power Component

Microsemi FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated in Table 2-9 for commercial, worst case conditions.

**Table 2-9 • Standby Power Calculation**

ICC	VCC	Power
2 mA	5.25 V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

## Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

## Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by EQ 4.

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * VCC^2 * F$$

EQ 4

Where:

C<sub>EQ</sub> is the equivalent capacitance expressed in pF.

VCC is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown in Figure 2-10.

**Table 2-10 • CEQ Values for Microsemi FPGAs**

Item	CEQ Value
Modules ( $C_{EQM}$ )	6.7
Input Buffers ( $C_{EQI}$ )	7.2
Output Buffers ( $C_{EQO}$ )	10.4
Routed Array Clock Buffer Loads ( $C_{EQCR}$ )	1.6
Dedicated Clock Buffer Loads ( $C_{EQCD}$ )	0.7
I/O Clock Buffer Loads ( $C_{EQCI}$ )	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. EQ 5 shows a piece-wise linear summation over all components.

$$\begin{aligned}
 \text{Power} = & VCC^2 * [(m * C_{EQM} * f_m)_{\text{modules}} + (n * C_{EQI} * f_n)_{\text{inputs}} \\
 & + (p * (C_{EQO} + C_L) * f_p)_{\text{outputs}} \\
 & + 0.5 * (q1 * C_{EQCR} * f_{q1})_{\text{routed\_Clk1}} + (r1 * f_{q1})_{\text{routed\_Clk1}} \\
 & + 0.5 * (q2 * C_{EQCR} * f_{q2})_{\text{routed\_Clk2}} \\
 & + (r2 * f_{q2})_{\text{routed\_Clk2}} + 0.5 * (s1 * C_{EQCD} * f_{s1})_{\text{dedicated\_Clk}} \\
 & + (s2 * C_{EQCI} * f_{s2})_{\text{IO\_Clk}}]
 \end{aligned}$$

EQ 5

Where:

m = Number of logic modules switching at  $f_m$

n = Number of input buffers switching at  $f_n$

p = Number of output buffers switching at  $f_p$

q1 = Number of clock loads on the first routed array clock

q2 = Number of clock loads on the second routed array clock

r1 = Fixed capacitance due to first routed array clock

r2 = Fixed capacitance due to second routed array clock

s1 = Fixed number of clock loads on the dedicated array clock

s2 = Fixed number of clock loads on the dedicated I/O clock

$C_{EQM}$  = Equivalent capacitance of logic modules in pF

$C_{EQI}$  = Equivalent capacitance of input buffers in pF

$C_{EQO}$  = Equivalent capacitance of output buffers in pF

$C_{EQCR}$  = Equivalent capacitance of routed array clock in pF

$C_{EQCD}$  = Equivalent capacitance of dedicated array clock in pF

$C_{EQCI}$  = Equivalent capacitance of dedicated I/O clock in pF

$C_L$  = Output lead capacitance in pF

$f_m$  = Average logic module switching rate in MHz

$f_n$  = Average input buffer switching rate in MHz

$f_p$  = Average output buffer switching rate in MHz

$f_{q1}$  = Average first routed array clock rate in MHz

$f_{q2}$  = Average second routed array clock rate in MHz

$f_{s1}$  = Average dedicated array clock rate in MHz

$f_{s2}$  = Average dedicated I/O clock rate in MHz



## A1415A, A14V15A Timing Characteristics (continued)

**Table 2-19 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

I/O Module Input Propagation Delays		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>2</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>INY</sub>	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t <sub>ICKY</sub>	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCKY</sub>	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>ICLRY</sub>	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t <sub>OCLRY</sub>	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
<b>Predicted Input Routing Delays<sup>2</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>I/O Module Sequential Timing (wrt IOCLK pad)</b>												
t <sub>INH</sub>	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>INSU</sub>	Input F-F Data Setup	2.0		2.3		2.5		3.0		3.0		ns
t <sub>IDEH</sub>	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>IDESU</sub>	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t <sub>OUTH</sub>	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t <sub>OUTSU</sub>	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t <sub>ODEH</sub>	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f <sub>ODESU</sub>	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

**Notes:**

- The –2 and –3 speed grades have been discontinued. Please refer to the Product Discontinuation Notices (PDNs) listed below:  
PDN March 2001  
PDN 0104  
PDN 0203  
PDN 0604  
PDN 1004
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1440A, A14V40A Timing Characteristics

**Table 2-26 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C<sup>1</sup>**

Logic Module Propagation Delays <sup>2</sup>		–3 Speed <sup>3</sup>		–2 Speed <sup>3</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Internal Array Module		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CO</sub>	Sequential Clock to Q		2.0		2.3		2.6		3.0		3.9	ns
t <sub>CLR</sub>	Asynchronous Clear to Q		2.0		2.3		2.6		3.0		3.9	ns
<b>Predicted Routing Delays<sup>4</sup></b>												
t <sub>RD1</sub>	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t <sub>RD2</sub>	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t <sub>RD3</sub>	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t <sub>RD4</sub>	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t <sub>RD8</sub>	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
<b>Logic Module Sequential Timing</b>												
t <sub>SUD</sub>	Flip-Flop Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>SUD</sub>	Latch Data Input Setup	0.5		0.6		0.7		0.8		0.8		ns
t <sub>HD</sub>	Latch Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t <sub>WASYN</sub>	Asynchronous Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>WCLKA</sub>	Flip-Flop Clock Pulse Width	1.9		2.4		3.2		3.8		4.8		ns
t <sub>A</sub>	Flip-Flop Clock Input Period	4.0		5.0		6.8		8.0		10.0		ns
f <sub>MAX</sub>	Flip-Flop Clock Frequency		250		200		150		125		100	MHz

**Notes:**

1. VCC = 3.0 V for 3.3 V specifications.
2. For dual-module macros, use t<sub>PD</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> + t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub> or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, whichever is appropriate.
3. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
4. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

## A1460A, A14V60A Timing Characteristics (continued)

**Table 2-33 • A1460A, A14V60A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>IOCKH</sub>	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	2.4		3.2		3.8		4.8		6.5		ns
t <sub>IOCKSW</sub>	Maximum Skew		0.6		0.6		0.6		0.6		0.6	ns
t <sub>IOP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>IOMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	2.4		3.2		3.8		4.8		6.5		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	2.4		3.2		3.8		4.8		6.5		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.6		0.6		0.6		0.6		0.6	ns
t <sub>HP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>HMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 216)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	0.0	5.0	ns
		0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 216)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

**Notes:**

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.

## A14100A, A14V100A Timing Characteristics (continued)

Table 2-36 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C

I/O Module – TTL Output Timing <sup>1</sup>		–3 Speed <sup>2</sup>		–2 Speed <sup>2</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>DHS</sub>	Data to Pad, High Slew		5.0		5.6		6.4		7.5		9.8	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		4.0		4.5		5.1		6.0		7.8	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.2		12.0		15.6	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		9.5		9.5		10.5		12.0		15.6	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		12.8		12.8		15.3		17.0		22.1	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.02		0.02		0.03		0.03		0.04	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.04		0.04		0.04		0.05		0.07	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.05		0.05		0.06		0.07		0.09	ns/pF
I/O Module – CMOS Output Timing <sup>1</sup>												
t <sub>DHS</sub>	Data to Pad, High Slew		6.2		7.0		7.9		9.3		12.1	ns
t <sub>DLS</sub>	Data to Pad, Low Slew		11.7		13.1		14.9		17.5		22.8	ns
t <sub>ENZHS</sub>	Enable to Pad, Z to H/L, High Slew		5.2		5.9		6.6		7.8		10.1	ns
t <sub>ENZLS</sub>	Enable to Pad, Z to H/L, Low Slew		8.9		10.0		11.3		13.3		17.3	ns
t <sub>ENHSZ</sub>	Enable to Pad, H/L to Z, High Slew		8.0		9.0		10.0		12.0		15.6	ns
t <sub>ENLSZ</sub>	Enable to Pad, H/L to Z, Low Slew		7.4		8.3		9.4		11.0		14.3	ns
t <sub>CKHS</sub>	IOCLK Pad to Pad H/L, High Slew		10.4		10.4		12.4		13.8		17.9	ns
t <sub>CKLS</sub>	IOCLK Pad to Pad H/L, Low Slew		14.5		14.5		17.4		19.3		25.1	ns
d <sub>TLHHS</sub>	Delta Low to High, High Slew		0.04		0.04		0.05		0.06		0.08	ns/pF
d <sub>TLHLS</sub>	Delta Low to High, Low Slew		0.07		0.08		0.09		0.11		0.14	ns/pF
d <sub>THLHS</sub>	Delta High to Low, High Slew		0.03		0.03		0.03		0.04		0.05	ns/pF
d <sub>THLLS</sub>	Delta High to Low, Low Slew		0.04		0.04		0.04		0.05		0.07	ns/pF

Notes: \*

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

**SDO                      Serial Data Output (Output)**

Serial data output for diagnostic probe. SDO is active when the MODE pin is High. This pin functions as an I/O when the MODE pin is Low.

**DCLK                      Diagnostic Clock (Input)**

Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**VCC                      5 V Supply Voltage**

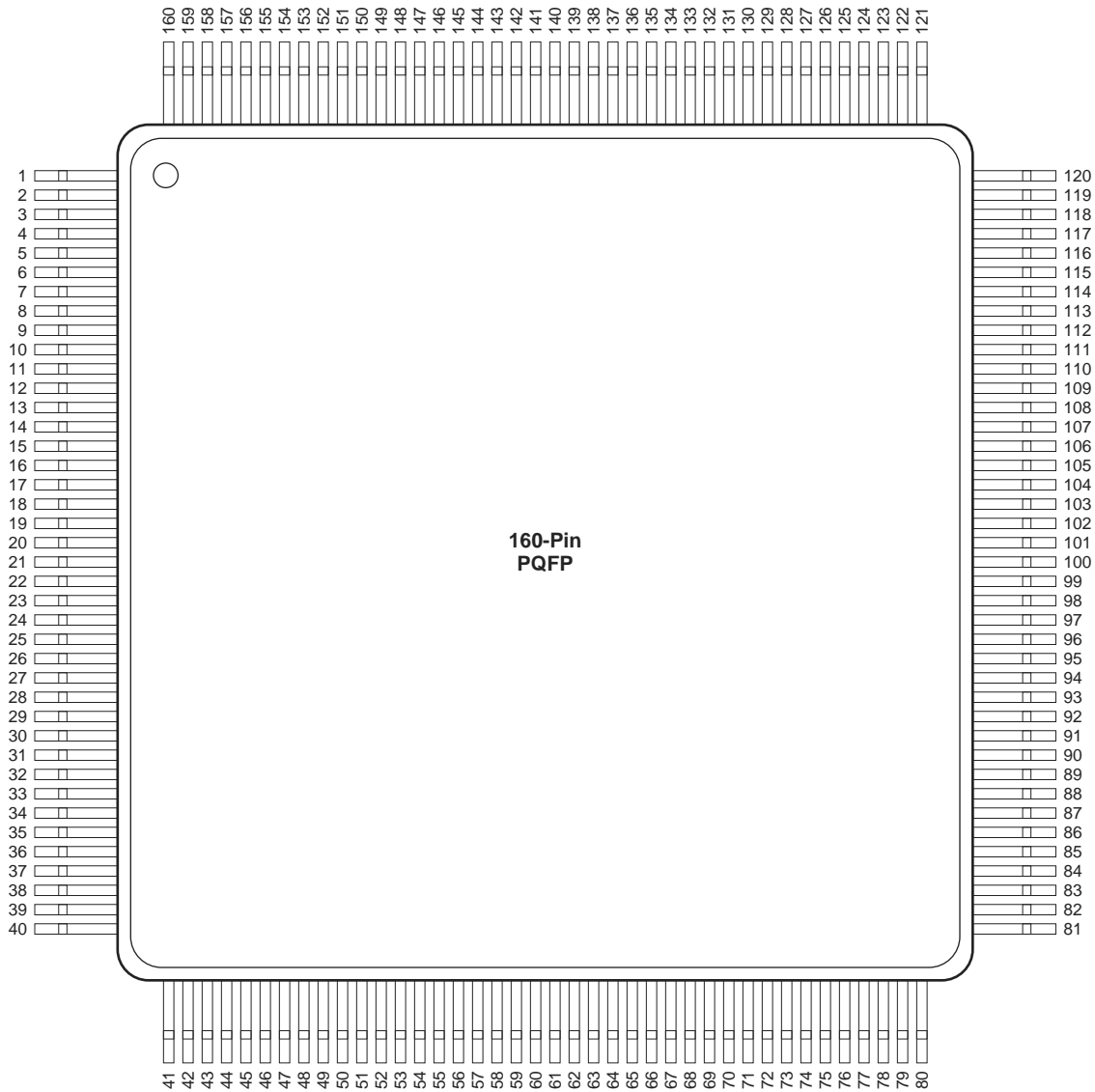
HIGH supply voltage.

PL84			
Pin Number	A1415, A14V15 Function	A1425, A14V25 Function	A1440, A14V40 Function
1	VCC	VCC	VCC
2	GND	GND	GND
3	VCC	VCC	VCC
4	PRA, I/O	PRA, I/O	PRA, I/O
11	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	SDI, I/O	SDI, I/O	SDI, I/O
16	MODE	MODE	MODE
27	GND	GND	GND
28	VCC	VCC	VCC
40	PRB, I/O	PRB, I/O	PRB, I/O
41	VCC	VCC	VCC
42	GND	GND	GND
43	VCC	VCC	VCC
45	HCLK, I/O	HCLK, I/O	HCLK, I/O
52	SDO	SDO	SDO
53	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
59	VCC	VCC	VCC
60	VCC	VCC	VCC
61	GND	GND	GND
68	VCC	VCC	VCC
69	GND	GND	GND
74	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	CLKB, I/O	CLKB, I/O	CLKB, I/O

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PQ160



*Note:* This is the top view of the package

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

CQ132		CQ132	
Pin Number	A1425 Function	Pin Number	A1425 Function
1	NC	67	NC
2	GND	74	GND
3	SDI, I/O	75	VCC
9	MODE	78	VCC
10	GND	89	VCC
11	VCC	90	GND
22	VCC	91	VCC
26	GND	92	GND
27	VCC	98	IOCLK, I/O
34	NC	99	NC
36	GND	100	NC
42	GND	101	GND
43	VCC	106	GND
48	PRB, I/O	107	VCC
50	HCLK, I/O	116	CLKA, I/O
58	GND	117	CLKB, I/O
59	VCC	118	PRA, I/O
63	SDO	122	GND
64	IOPCL, I/O	123	VCC
65	GND	131	DCLK, I/O
66	NC	132	NC

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



CQ256	
Pin Number	A14100 Function
1	GND
2	SDI, I/O
11	MODE
28	VCC
29	GND
30	VCC
31	GND
46	VCC
59	GND
90	PRB, I/O
91	GND
92	VCC
93	GND
94	VCC
96	HCLK, I/O
110	GND
126	SDO
127	IOPCL, I/O
128	GND

CQ256	
Pin Number	A14100 Function
141	VCC
158	GND
159	VCC
160	GND
161	VCC
174	VCC
175	GND
176	GND
188	IOCLK, I/O
189	GND
219	CLKA, I/O
220	CLKB, I/O
221	VCC
222	GND
223	VCC
224	GND
225	PRA, I/O
240	GND
256	DCLK, I/O

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

BG225	
A1460 Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

BG313	
A14100, A14V100 Function	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA or I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
SDO	AE23
VCC	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG257	
A14100 Function	Location
CLKA or I/O	L4
CLKB or I/O	L5
DCLK or I/O	E4
GND	B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7
HCLK or I/O	J16
IOCLK or I/O	T5
IOPCL or I/O	R16
MODE	A5
NC	E5
PRA or I/O	J1
PRB or I/O	J17
SDI or I/O	B4
SDO	R17
VCC	C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## 4 – Datasheet Information

### List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades –2 and –3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	I and others
	The "Features" section was revised to state the clock-to-output time and on-chip performance for –1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 • ACT 3 Family Product Information, and now reflect worst-case commercial for the –1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	III
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the –1 speed grade instead of –3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	3-1