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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

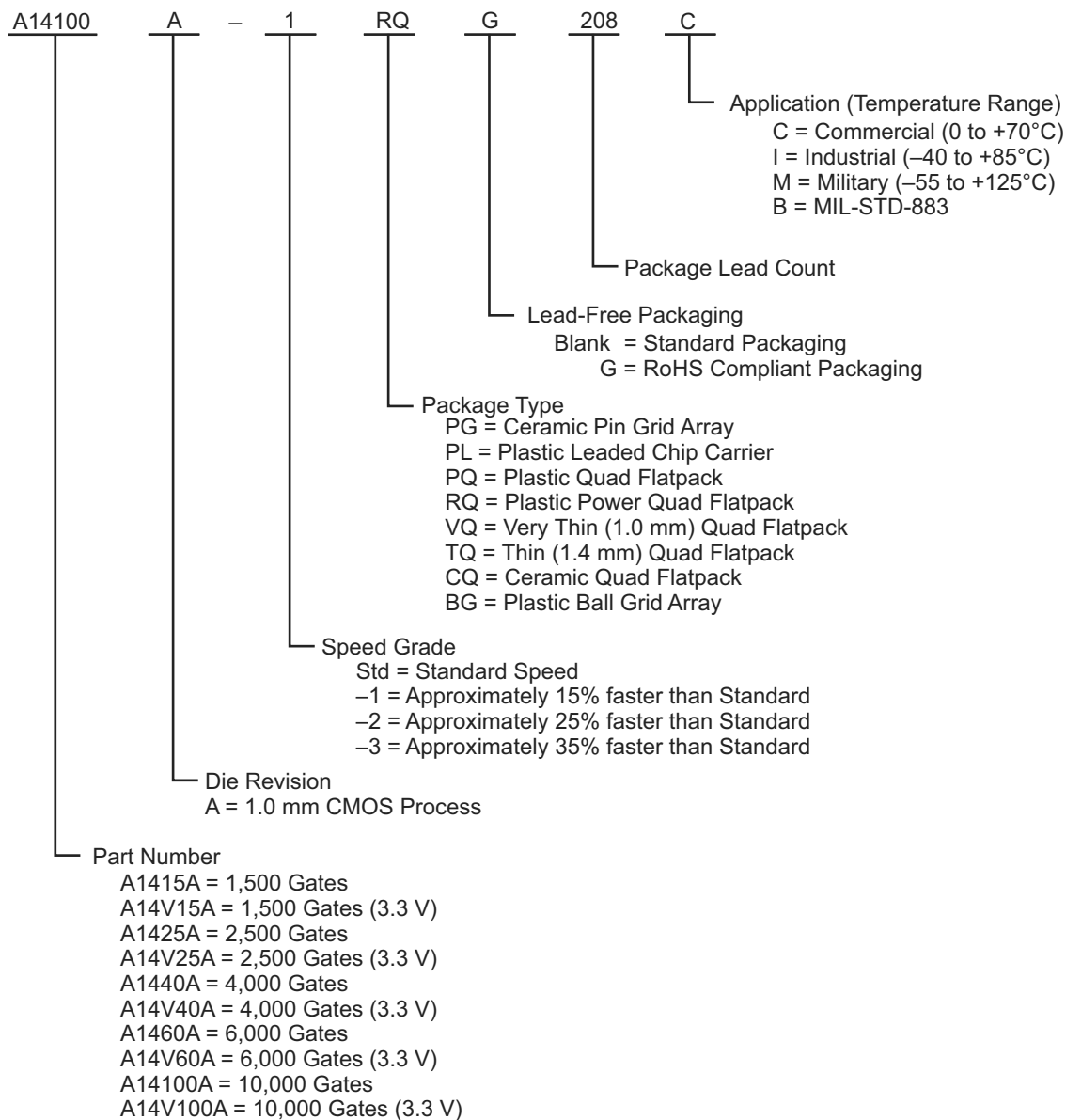
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	564
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	131
Number of Gates	4000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a14v40a-pqg160c

Ordering Information



Notes:

- The -2 and -3 speed grades have been discontinued.
- The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
- The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
- Military Grade devices are no longer available for the A1440A device.
- For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:
 PDN March 2001
 PDN 0104
 PDN 0203
 PDN 0604
 PDN 1004

1 – ACT 3 Family Overview

General Description

Microsemi's ACT 3 Accelerator Series of FPGAs offers the industry's fastest high-capacity programmable logic device. ACT 3 FPGAs offer a high performance, PCI compliant programmable solution capable of 186 MHz on-chip performance and 9.0 nanosecond clock-to-output (–1 speed grade), with capacities spanning from 1,500 to 10,000 gate array equivalent gates.

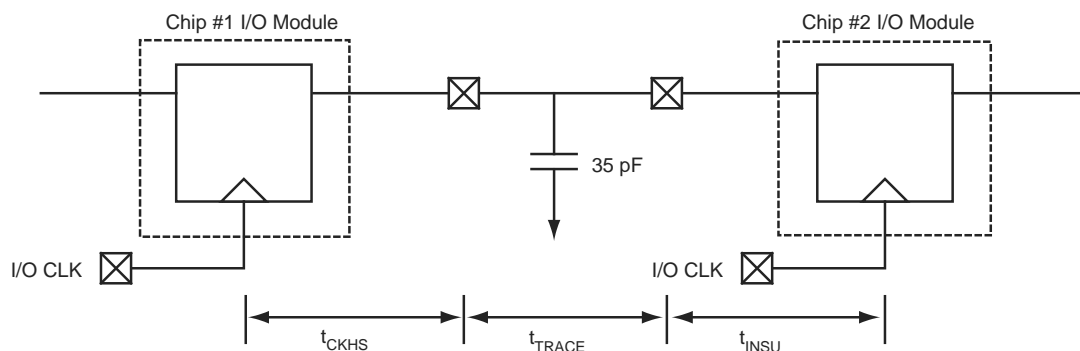
The ACT 3 family builds on the proven two-module architecture consisting of combinatorial and sequential logic modules used in Microsemi's 3200DX and 1200XL families. In addition, the ACT 3 I/O modules contain registers which deliver 9.0 nanosecond clock-to-out times (–1 speed grade). The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals such as flip-flop resets and output.

The ACT 3 family is supported by Microsemi's Designer Series Development System which offers automatic placement and routing (with automatic or fixed pin assignments), static timing analysis, user programming, and debug and diagnostic probe capabilities.

Accumulators (16-Bit)	47 MHz
Loadable Counters (16-Bit)	82 MHz
Prescaled Loadable Counters (16-Bit)	186 MHz
Shift Registers	186 MHz

Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade)

System Performance Model



Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

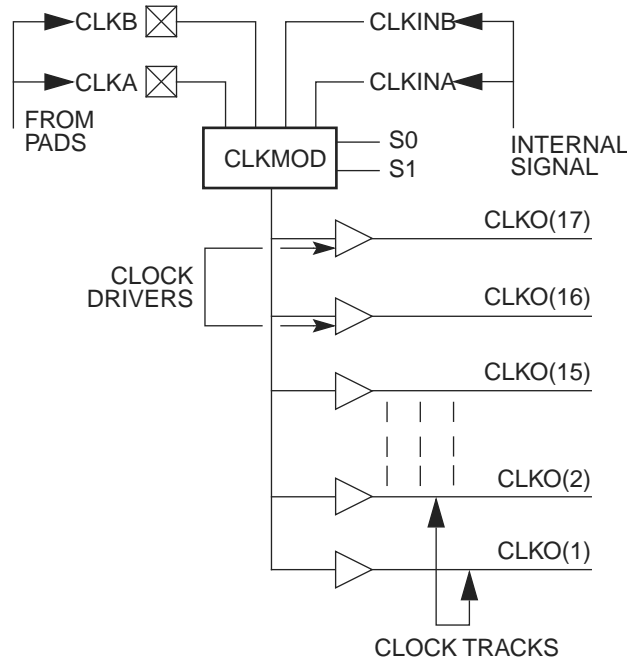


Figure 2-6 • Clock Networks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (Figure 2-6):

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINA input
- Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 2-7. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

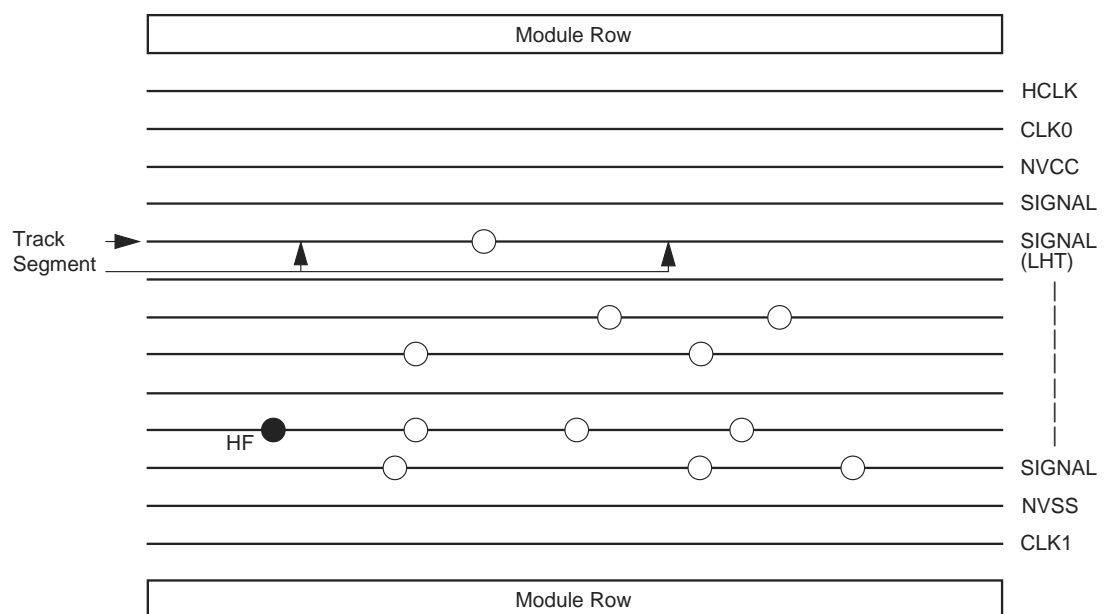


Figure 2-7 • Horizontal Routing Tracks and Segments

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 2-8.

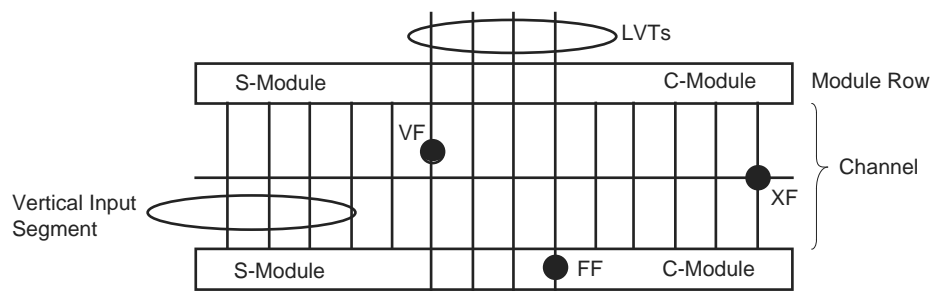


Figure 2-8 • Vertical Routing Tracks and Segments

A1415A, A14V15A Timing Characteristics (continued)

Table 2-21 • A1415A, A14V15A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Dedicated (hardwired) I/O Clock Network		–3 Speed		–2 Speed		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ILOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t _{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t _{ILOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t _{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t _{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t _{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t _{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t _{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f _{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
t _{IOHCKSW}	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t _{IORCKSW}	I/O Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% maximum)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns

Notes:

1. Delays based on 35 pF loading.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

A1425A, A14V25A Timing Characteristics (continued)

Table 2-25 • A1425A, A14V25A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

Dedicated (hardwired) I/O Clock Network		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{ILOCKH}	Input Low to High (pad to I/O module input)		2.0		2.3		2.6		3.0		3.5	ns
t _{IOPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{IPOWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{IOSAPW}	Minimum Asynchronous Pulse Width	1.9		2.4		3.3		3.8		4.8		ns
t _{ILOCKSW}	Maximum Skew		0.4		0.4		0.4		0.4		0.4	ns
t _{IOP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{IOMAX}	Maximum Frequency		250		200		150		125		100	MHz
Dedicated (hardwired) Array Clock												
t _{HCKH}	Input Low to High (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HCKL}	Input High to Low (pad to S-module input)		3.0		3.4		3.9		4.5		5.5	ns
t _{HPWH}	Minimum Pulse Width High	1.9		2.4		3.3		3.8		4.8		ns
t _{HPWL}	Minimum Pulse Width Low	1.9		2.4		3.3		3.8		4.8		ns
t _{HCKSW}	Delta High to Low, Low Slew		0.3		0.3		0.3		0.3		0.3	ns
t _{HP}	Minimum Period	4.0		5.0		6.8		8.0		10.0		ns
f _{HMAX}	Maximum Frequency		250		200		150		125		100	MHz
Routed Array Clock Networks												
t _{RCKH}	Input Low to High (FO = 64)		3.7		4.1		4.7		5.5		9.0	ns
t _{RCKL}	Input High to Low (FO = 64)		4.0		4.5		5.1		6.0		9.0	ns
t _{RPWH}	Min. Pulse Width High (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RPWL}	Min. Pulse Width Low (FO = 64)	3.3		3.8		4.2		4.9		6.5		ns
t _{RCKSW}	Maximum Skew (FO = 128)		0.7		0.8		0.9		1.0		1.0	ns
t _{RP}	Minimum Period (FO = 64)	6.8		8.0		8.7		10.0		13.4		ns
f _{RMAX}	Maximum Frequency (FO = 64)		150		125		115		100		75	MHz
Clock-to-Clock Skews												
t _{IOHCKSW}	I/O Clock to H-Clock Skew	0.0	1.7	0.0	1.8	0.0	2.0	0.0	2.2	0.0	3.0	ns
t _{IORCKSW}	I/O Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	3.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	
t _{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 80)	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

Notes:

- The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
- Delays based on 35 pF loading.

A1440A, A14V40A Timing Characteristics (continued)

Table 2-27 • A1440A, A14V40A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

I/O Module Input Propagation Delays		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	1.8		1.7		2.0		2.3		2.3		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		0.9		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		0.9		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.4		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		1.7		2.0		2.0		ns

Notes:

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A14100A, A14V100A Timing Characteristics (continued)

Table 2-35 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T_J = 70°C

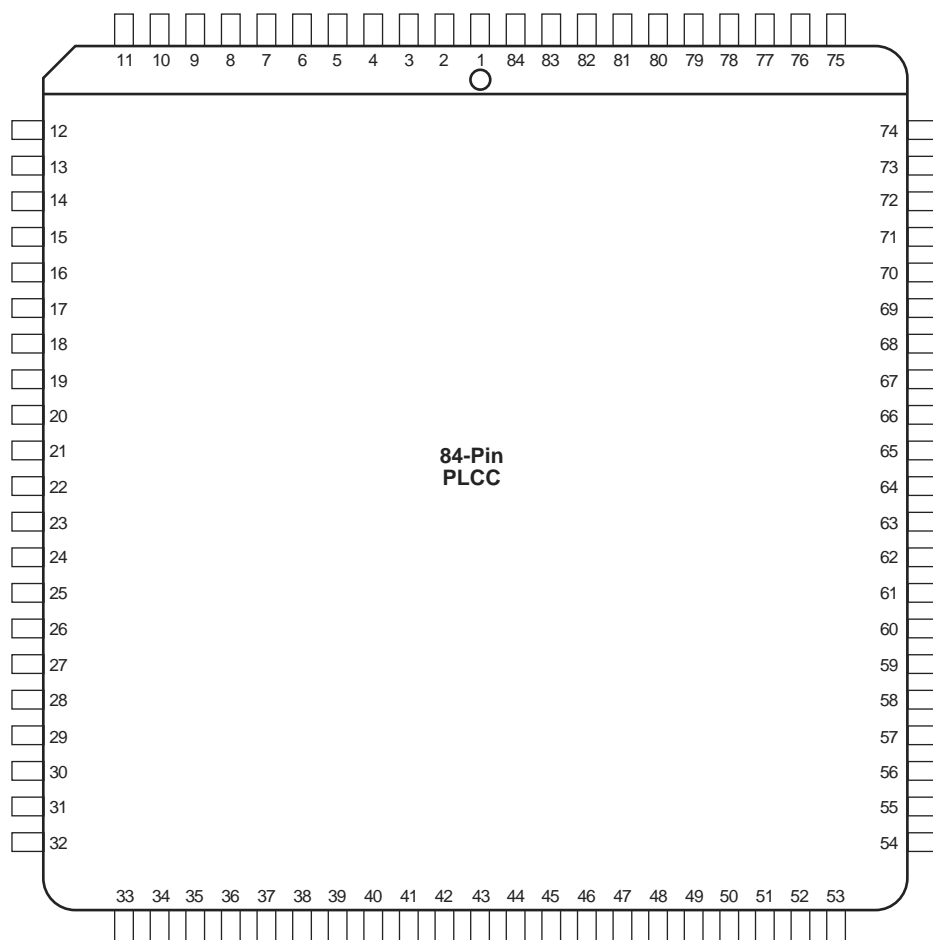
I/O Module Input Propagation Delays		–3 Speed ¹		–2 Speed ¹		–1 Speed		Std. Speed		3.3 V Speed ¹		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{INY}	Input Data Pad to Y		2.8		3.2		3.6		4.2		5.5	ns
t _{ICKY}	Input Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCKY}	Output Reg IOCLK Pad to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{ICLRY}	Input Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
t _{OCLRY}	Output Asynchronous Clear to Y		4.7		5.3		6.0		7.0		9.2	ns
Predicted Input Routing Delays²												
t _{RD1}	FO = 1 Routing Delay		0.9		1.0		1.1		1.3		1.7	ns
t _{RD2}	FO = 2 Routing Delay		1.2		1.4		1.6		1.8		2.4	ns
t _{RD3}	FO = 3 Routing Delay		1.4		1.6		1.8		2.1		2.8	ns
t _{RD4}	FO = 4 Routing Delay		1.7		1.9		2.2		2.5		3.3	ns
t _{RD8}	FO = 8 Routing Delay		2.8		3.2		3.6		4.2		5.5	ns
I/O Module Sequential Timing (wrt IOCLK pad)												
t _{INH}	Input F-F Data Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{INSU}	Input F-F Data Setup	1.2		1.4		1.5		1.8		1.8		ns
t _{IDEH}	Input Data Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t _{IDESU}	Input Data Enable Setup	5.8		6.5		7.5		8.6		8.6		ns
t _{OUTH}	Output F-F Data hold	0.7		0.8		1.0		1.0		1.0		ns
t _{OUTSU}	Output F-F Data Setup	0.7		0.8		1.0		1.0		1.0		ns
t _{ODEH}	Output Data Enable Hold	0.3		0.4		0.5		0.5		0.5		ns
f _{ODESU}	Output Data Enable Setup	1.3		1.5		2.0		2.0		2.0		ns

Notes: *

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

3 – Package Pin Assignments

PL84

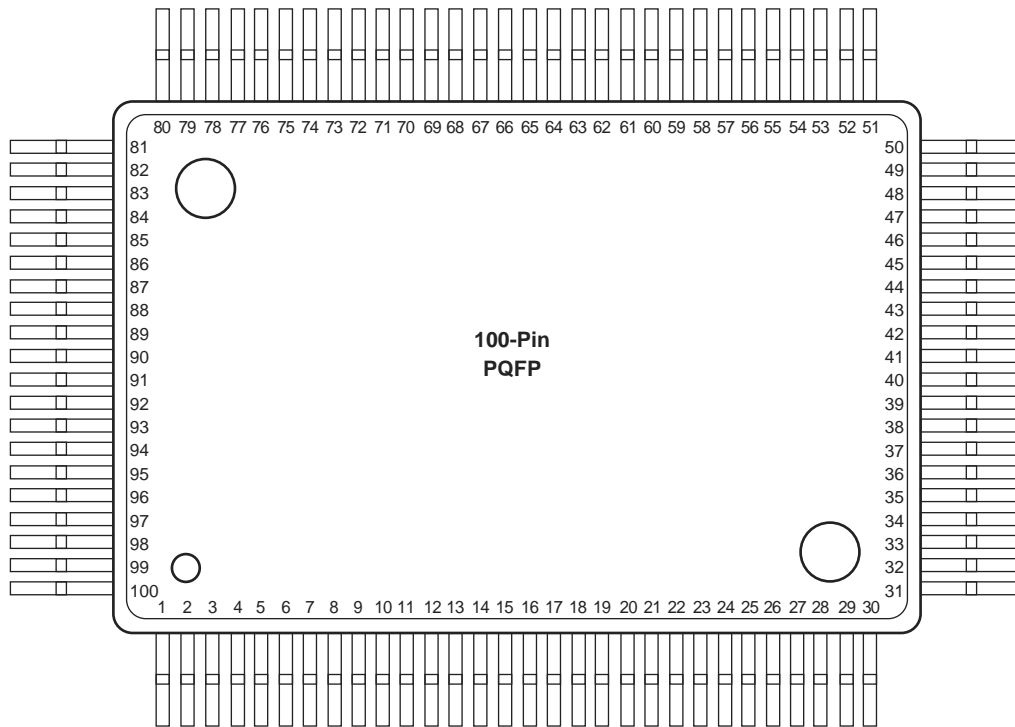


Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

PQ100

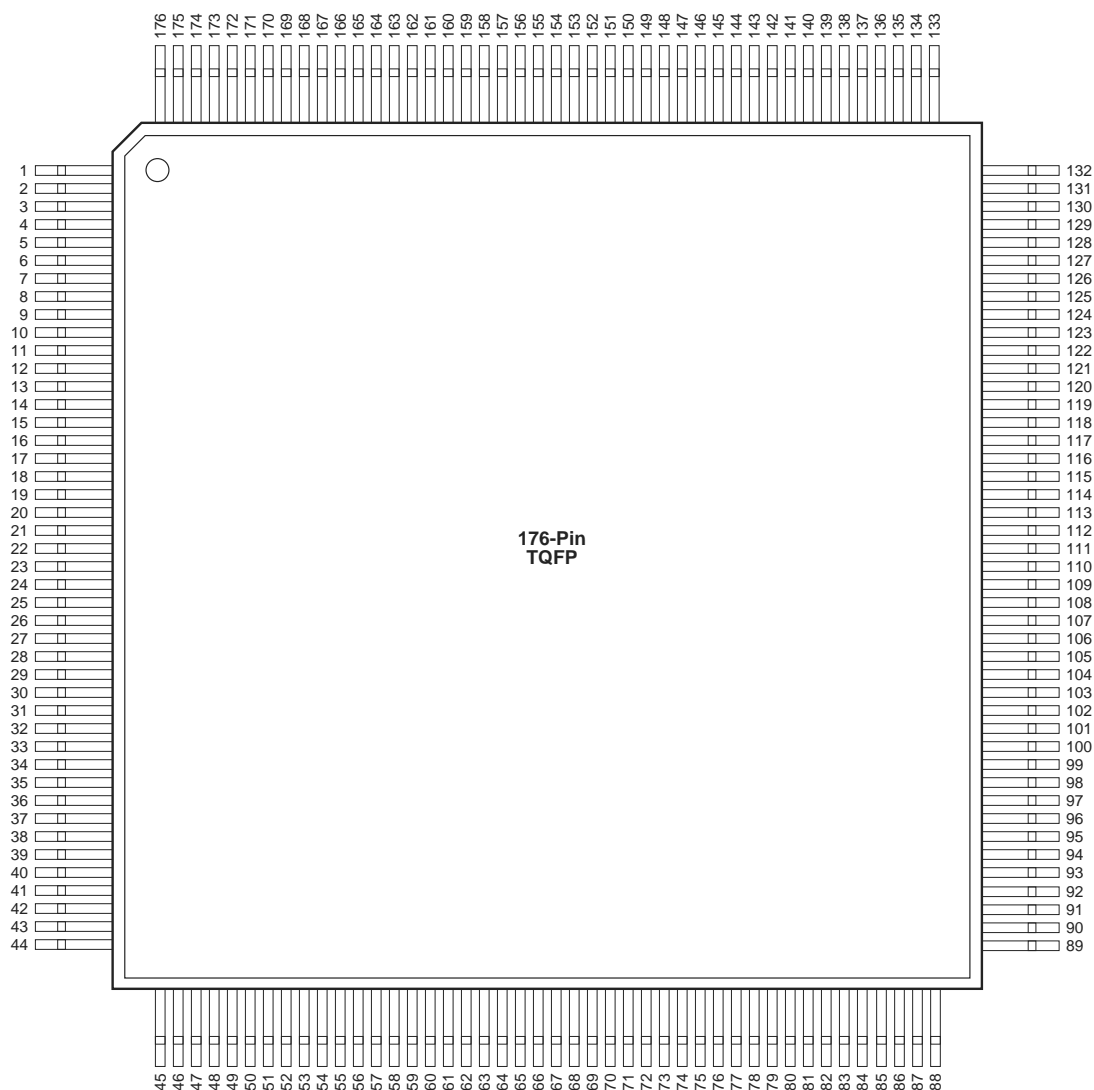


Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

TQ176



Note: This is the top view.

Note

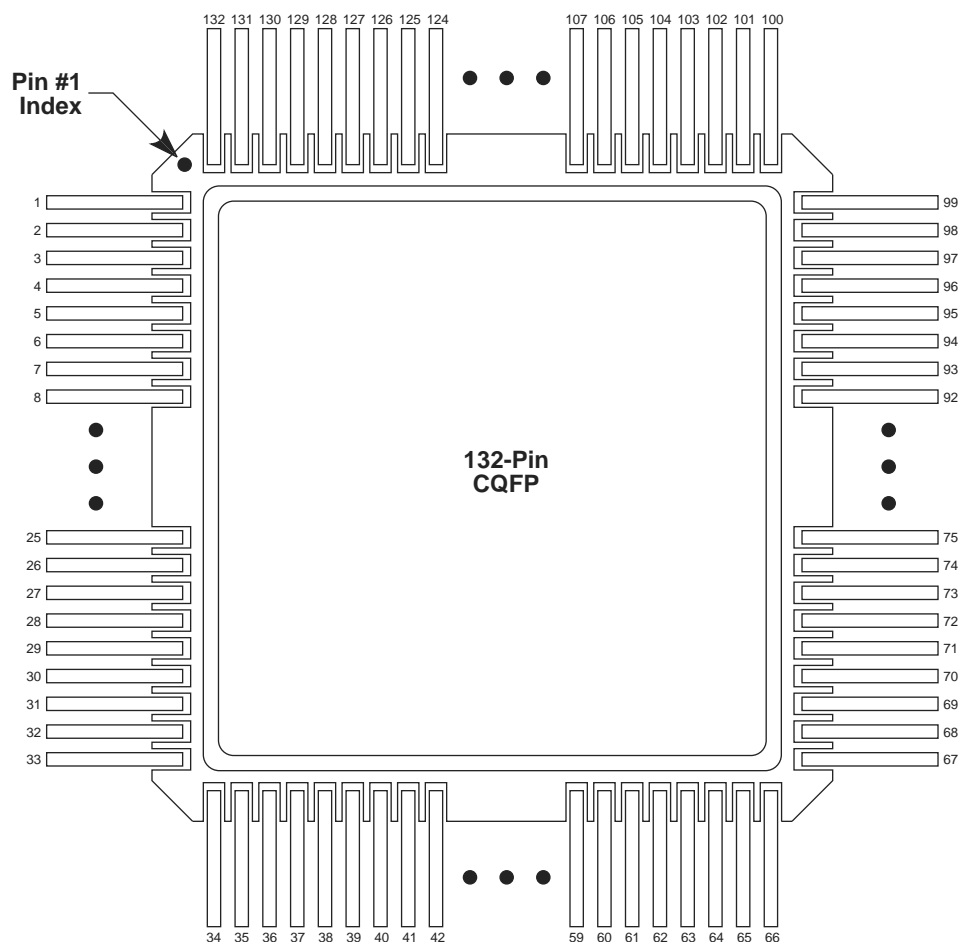
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

VQ100			
Pin Number	A1415, A14V15 Function	A1425, A14V25 Function	A1440, A14V40 Function
1	GND	GND	GND
2	SDI, I/O	SDI, I/O	SDI, I/O
7	MODE	MODE	MODE
8	VCC	VCC	VCC
9	GND	GND	GND
20	VCC	VCC	VCC
21	NC	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	VCC	VCC	VCC
36	GND	GND	GND
37	VCC	VCC	VCC
39	HCLK, I/O	HCLK, I/O	HCLK, I/O
49	SDO	SDO	SDO
50	IOPCL, I/O	IOPCL, I/O	IOPCL, I/O
51	GND	GND	GND
57	VCC	VCC	VCC
58	VCC	VCC	VCC
67	VCC	VCC	VCC
68	GND	GND	GND
69	GND	GND	GND
74	NC	I/O	I/O
75	IOCLK, I/O	IOCLK, I/O	IOCLK, I/O
87	CLKA, I/O	CLKA, I/O	CLKA, I/O
88	CLKB, I/O	CLKB, I/O	CLKB, I/O
89	VCC	VCC	VCC
90	VCC	VCC	VCC
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	NC	I/O	I/O
100	DCLK, I/O	DCLK, I/O	DCLK, I/O

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

CQ132

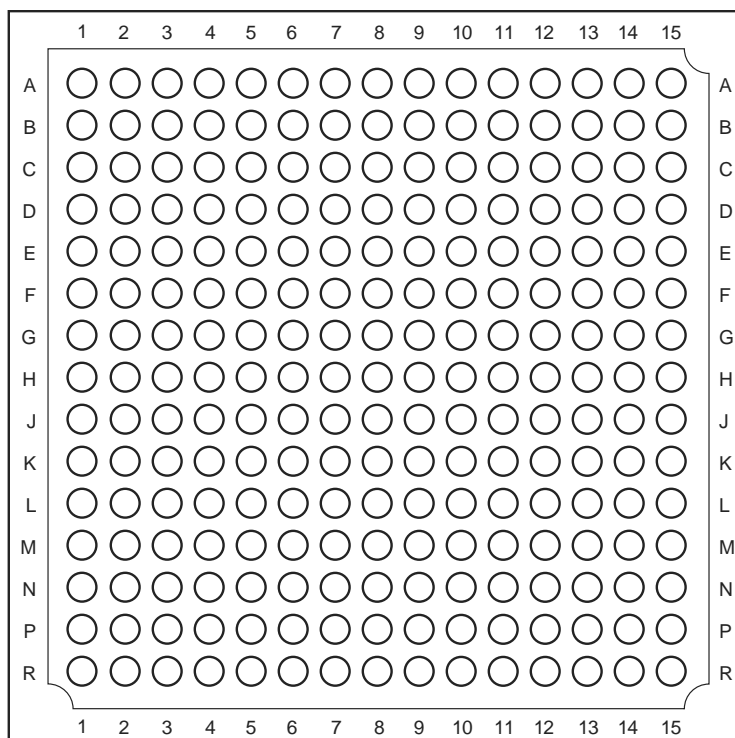


Note: This is the top view

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

BG225



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

BG225	
A1460 Function	Location
CLKA or I/O	C8
CLKB or I/O	B8
DCLK or I/O	B2
GND	A1, A15, D15, F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8, P2, R15
HCLK or I/O	P9
IOCLK or I/O	B14
IOPCL or I/O	P14
MODE	D1
NC	A11, B5, B7, D8, D12, F6, F11, H1, H12, H14, K11, L1, L13, N8, P5, R1, R8, R11, R14
PRA or I/O	A7
PRB or I/O	L7
SDI or I/O	D4
SDO	N13
VCC	A8, B12, D5, D14, E3, E8, E13, H2, H3, H11, H15, K4, L2, L12, M8, M15, P4, P8, R13

Notes:

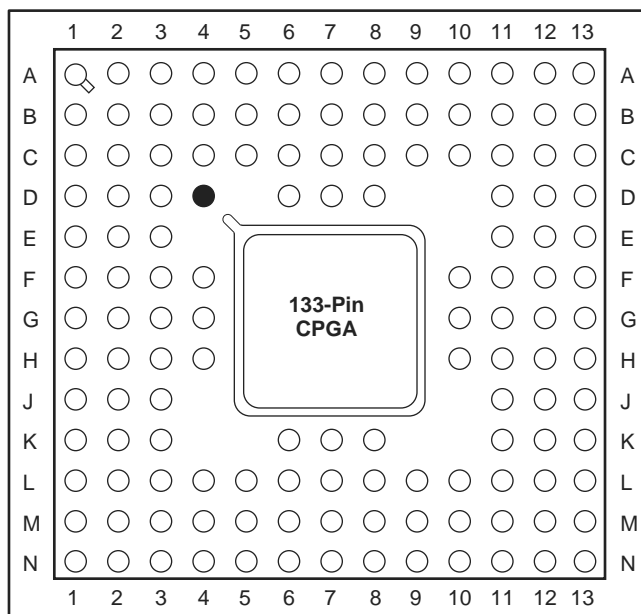
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The BG225 package has been discontinued.

PG100	
A1415 Function	Location
CLKA or I/O	C7
CLKB or I/O	D6
DCLK or I/O	C4
GND	C3, C6, C9, E9, F3, F9, J3, J6, J8, J9
HCLK or I/O	H6
IOCLK or I/O	C10
IOPCL or I/O	K9
MODE	C2
PRA or I/O	A6
PRB or I/O	L3
SDI or I/O	B3
SDO	L9
VCC	B6, B10, E11, F2, F10, G2, K2, K6, K10

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG100 package has been discontinued.

PG133



Note: This is the top view.

Note

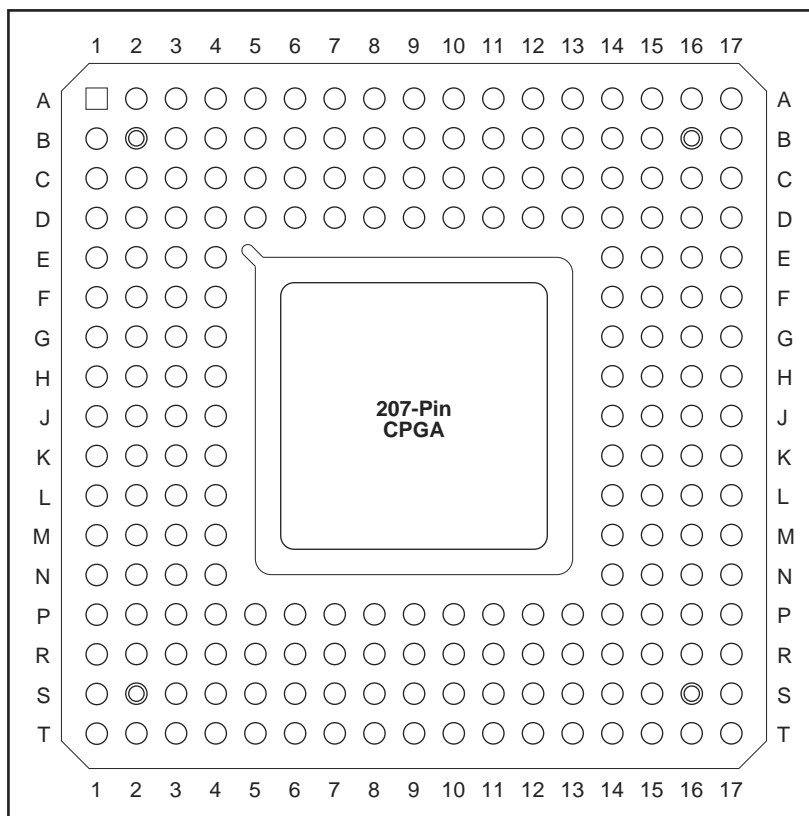
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

PG133	
A1425 Function	Location
CLKA or I/O	D7
CLKB or I/O	B6
DCLK or I/O	D4
GND	A2, C3, C7, C11, C12, F10, G3, G11, L3, L7, L11, M3, N12
HCLK or I/O	K7
IOCLK or I/O	C10
IOPCL or I/O	L10
MODE	E3
NC	A1, A7, A13, G1, G13, N1, N7, N13
PRA or I/O	A6
PRB or I/O	L6
SDI or I/O	C2
SDO	M11
VCC	B2, B7, B12, E11, G2, G12, J2, J12, M2, M7, M12

Notes:

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.
4. The PG133 package has been discontinued.

PG207



Note: This is the top view.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

