



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	848
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	131
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microsemi/a14v60a-pq160c">https://www.e-xfl.com/product-detail/microsemi/a14v60a-pq160c</a>

## Ordering Information



### Notes:

1. The -2 and -3 speed grades have been discontinued.
2. The Ceramic Pin Grid Array packages PG100, PG133, and PG175 have been discontinued in all device densities, speed grades, and temperature grades.
3. The Plastic Ball Grid Array package BG225 has been discontinued in all device densities (specifically for A1460A), all speed grades, and all temperature grades.
4. Military Grade devices are no longer available for the A1440A device.
5. For more information about discontinued devices, refer to the Product Discontinuation Notices (PDNs) listed below, available on the Microsemi SoC Products Group website:  
 PDN March 2001  
 PDN 0104  
 PDN 0203  
 PDN 0604  
 PDN 1004

## Plastic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PL84	PQ100	PQ160	PQ/RQ208	VQ100	TQ176	BG225*	BG313
A1415	200	1500	70	80	–	–	80	–	–	–
A1425	310	2500	70	80	100	–	83	–	–	–
A1440	564	4000	70	–	131	–	83	140	–	–
A1460	848	6000	–	–	131	167	–	151	168	–
A14100	1377	10000	–	–	–	175	–	–	–	228

Note: \*Discontinued

## Hermetic Device Resources

Device Series	Logic Modules	Gates	User I/Os							
			PG100*	PG133*	PG175*	PG207	PG257	CQ132	CQ196	CQ256
A1415	200	1500	80	–	–	–	–	–	–	–
A1425	310	2500	–	100	–	–	–	100	–	–
A1440	564	4000	–	–	140	–	–	–	–	–
A1460	848	6000	–	–	–	168	–	–	168	–
A14100	1377	10000	–	–	–	–	228	–	–	228

Note: \*Discontinued

Contact your local Microsemi SoC Products Group (formerly Actel) representative for device availability:

<http://www.microsemi.com/soc/contact/default.aspx>.

## ACT 3 Family Overview

General Description .....	1-1
---------------------------	-----

## Detailed Specifications

Topology .....	2-1
Logic Modules .....	2-2
I/Os .....	2-3
Clock Networks .....	2-4
Routing Structure .....	2-5
5 V Operating Conditions .....	2-9
3.3 V Operating Conditions .....	2-10
Package Thermal Characteristics .....	2-11
ACT 3 Timing Model .....	2-16
Pin Descriptions .....	2-42

## Package Pin Assignments

PL84 .....	3-1
PQ100 .....	3-3
PQ160 .....	3-5
PQ208, RQ208 .....	3-8
VQ100 .....	3-12
CQ132 .....	3-14
CQ196 .....	3-16
CQ256 .....	3-18
BG225 .....	3-20
BG313 .....	3-22
PG100 .....	3-24
PG133 .....	3-26
PG175 .....	3-28
PG207 .....	3-30
PG257 .....	3-32

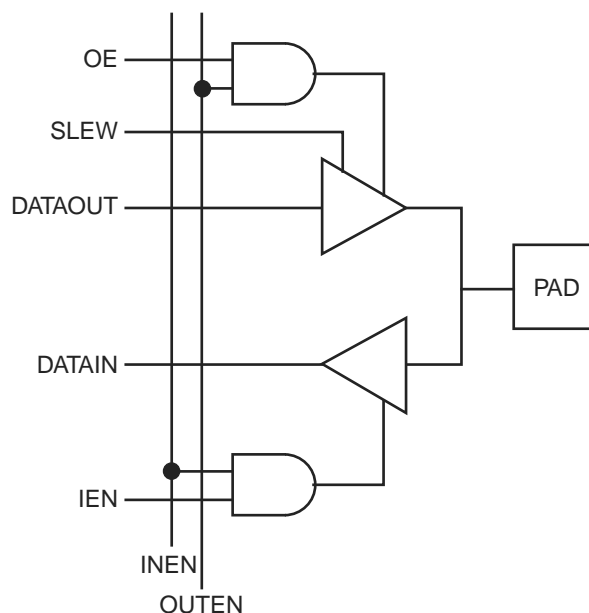
## Datasheet Information

List of Changes .....	4-1
Datasheet Categories .....	4-3
Safety Critical, Life Support, and High-Reliability Applications Policy .....	4-3

The I/O module output Y is used to bring Pad signals into the array or to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below (similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

## I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 2-5.



**Figure 2-5 • Function Diagram for I/O Pad Driver**

## Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

## Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 200 MHz, while the general purpose routed networks function up to 150 MHz.

## 3.3 V Operating Conditions

**Table 2-5 • Absolute Maximum Ratings<sup>1</sup>, Free Air Temperature Range**

Symbol	Parameter	Limits	Units
VCC	DC supply voltage	−0.5 to +7.0	V
VI	Input voltage	−0.5 to VCC + 0.5	V
VO	Output voltage	−0.5 to VCC + 0.5	V
IIO	I/O source sink current <sup>2</sup>	±20	mA
T <sub>STG</sub>	Storage temperature	−65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than VCC + 0.5 V for less than GND −0.5 V, the internal protection diodes will forward bias and can draw excessive current.

**Table 2-6 • Recommended Operating Conditions**

Parameter	Commercial	Units
Temperature range*	0 to +70	°C
Power supply tolerance	3.0 to 3.6	V

Note: \*Ambient temperature (T<sub>A</sub>) is used for commercial.

**Table 2-7 • Electrical Specifications**

Parameter		Commercial		Units
		Min.	Max.	
VOH <sup>1</sup>	I <sub>OH</sub> = −4 mA	2.15	–	V
	I <sub>OH</sub> = −3.2 mA	2.4		V
VOL <sup>1</sup>	I <sub>OL</sub> = 6 mA		0.4	V
VIL		−0.3	0.8	V
VIH		2.0	VCC + 0.3	V
Input transition time t <sub>R</sub> , t <sub>F</sub> <sup>2</sup>	VI = VCC or GND	−10	+10	μA
C <sub>IO</sub> I/O Capacitance <sup>2,3</sup>			10	pF
Standby current, I <sub>CC</sub> <sup>4</sup> (typical = 0.3 mA)			0.75	mA
Leakage current <sup>5</sup>		−10	10	μA

1. Only one output tested at a time. VCC = minimum.
2. Not tested; for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V<sub>OUT</sub> = 0 V, f = 1 MHz.
4. Typical standby current = 0.3 mA. All outputs unloaded. All inputs = VCC or GND.
5. VO, VIN = VCC or GND

## Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track. The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Microsemi's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 micron m lithography, offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse. The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

**Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions**

Speed Grade	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8
ACT 3 –3	2.9	3.2	3.4	3.7	4.8
ACT 3 –2	3.3	3.7	3.9	4.2	5.5
ACT 3 –1	3.7	4.2	4.4	4.8	6.2
ACT 3 STD	4.3	4.8	5.1	5.5	7.2

Notes:

1. Obtained by added  $t_{RD(x=FO)}$  to  $t_{PD}$  from the Logic Module Timing Characteristics Tables found in this datasheet.
2. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.

## Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

### Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

### Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO = 8) routing delays in the datasheet specifications section.

## A14100A, A14V100A Timing Characteristics (continued)

**Table 2-37 • A14100A, A14V100A Worst-Case Commercial Conditions, VCC = 4.75 V, T<sub>J</sub> = 70°C**

Dedicated (hardwired) I/O Clock Network		–3 Speed <sup>1</sup>		–2 Speed <sup>1</sup>		–1 Speed		Std. Speed		3.3 V Speed <sup>1</sup>		Units
Parameter/Description		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>ILOCKH</sub>	Input Low to High (pad to I/O module input)		2.3		2.6		3.0		3.5		4.5	ns
t <sub>IOPWH</sub>	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IPOWL</sub>	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t <sub>IOSAPW</sub>	Minimum Asynchronous Pulse Width	2.4		3.3		3.8		4.8		6.5		ns
t <sub>ILOCKSW</sub>	Maximum Skew		0.6		0.6		0.7		0.8		0.6	ns
t <sub>IOP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>IOMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Dedicated (hardwired) Array Clock</b>												
t <sub>HCKH</sub>	Input Low to High (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HCKL</sub>	Input High to Low (pad to S-module input)		3.7		4.1		4.7		5.5		7.0	ns
t <sub>HPWH</sub>	Minimum Pulse Width High	2.4		3.3		3.8		4.8		6.5		ns
t <sub>HPWL</sub>	Minimum Pulse Width Low	2.4		3.3		3.8		4.8		6.5		ns
t <sub>HCKSW</sub>	Delta High to Low, Low Slew		0.6		0.6		0.7		0.8		0.6	ns
t <sub>HP</sub>	Minimum Period	5.0		6.8		8.0		10.0		13.4		ns
f <sub>HMAX</sub>	Maximum Frequency		200		150		125		100		75	MHz
<b>Routed Array Clock Networks</b>												
t <sub>RCKH</sub>	Input Low to High (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RCKL</sub>	Input High to Low (FO = 64)		6.0		6.8		7.7		9.0		11.8	ns
t <sub>RPWH</sub>	Min. Pulse Width High (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RPWL</sub>	Min. Pulse Width Low (FO = 64)	4.1		4.5		5.4		6.1		8.2		ns
t <sub>RCKSW</sub>	Maximum Skew (FO = 128)		1.2		1.4		1.6		1.8		1.8	ns
t <sub>RP</sub>	Minimum Period (FO = 64)	8.3		9.3		11.1		12.5		16.7		ns
f <sub>RMAX</sub>	Maximum Frequency (FO = 64)		120		105		90		80		60	MHz
<b>Clock-to-Clock Skews</b>												
t <sub>IOHCKSW</sub>	I/O Clock to H-Clock Skew	0.0	2.6	0.0	2.7	0.0	2.9	0.0	3.0	0.0	3.0	ns
t <sub>IORCKSW</sub>	I/O Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0	1.7	0.0	1.7	0.0	1.7	0.0	1.7	0.0	5.0	ns
		0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	0.0	5.0	
t <sub>HRCKSW</sub>	H-Clock to R-Clock Skew (FO = 64) (FO = 350)	0.0	1.3	0.0	1.0	0.0	1.0	0.0	1.0	0.0	1.0	ns
		0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	0.0	3.0	

Notes: \*

1. The –2 and –3 speed grades have been discontinued. Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004 at <http://www.microsemi.com/soc/support/notifications/default.aspx#pdn>.
2. Delays based on 35 pF loading.



## Pin Descriptions

### **CLKA**                      **Clock A (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **CLKB**                      **Clock B (Input)**

Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

### **GND**                      **Ground**

LOW supply voltage.

### **HCLK**                      **Dedicated (Hard-wired) Array Clock (Input)**

Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

### **I/O**                      **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tristated by the Designer Series software.

### **IOCLK**                      **Dedicated (Hard-wired) I/O Clock (Input)**

Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

### **IOPCL**                      **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

Input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

### **MODE**                      **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

### **NC**                      **No Connection**

This pin is not connected to circuitry within the device.

### **PRA**                      **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **PRB**                      **Probe B (Output)**

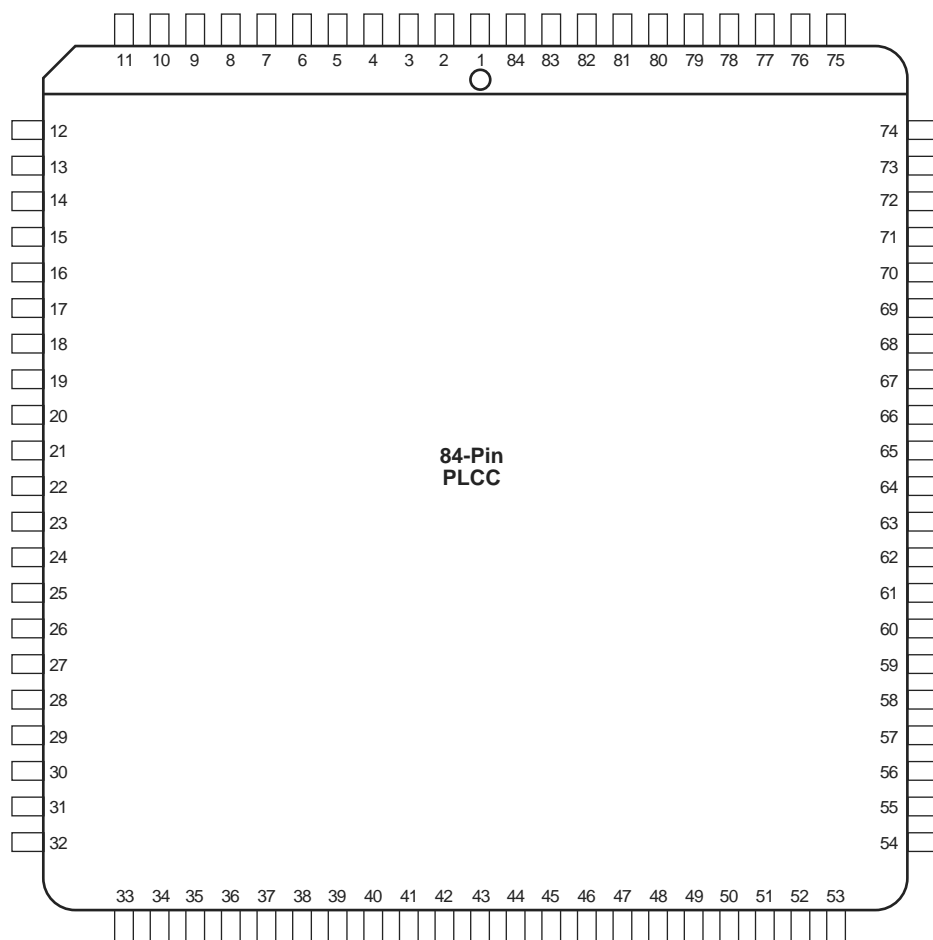
The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

### **SDI**                      **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

## 3 – Package Pin Assignments

### PL84

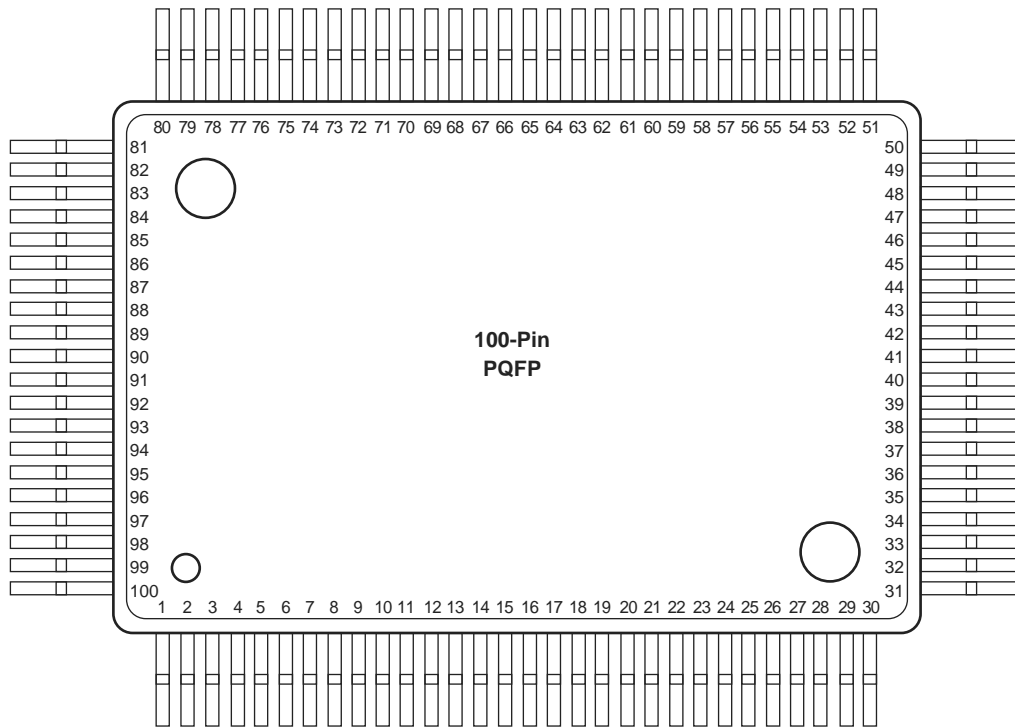


*Note: This is the top view of the package.*

#### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

## PQ100



*Note:* This is the top view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

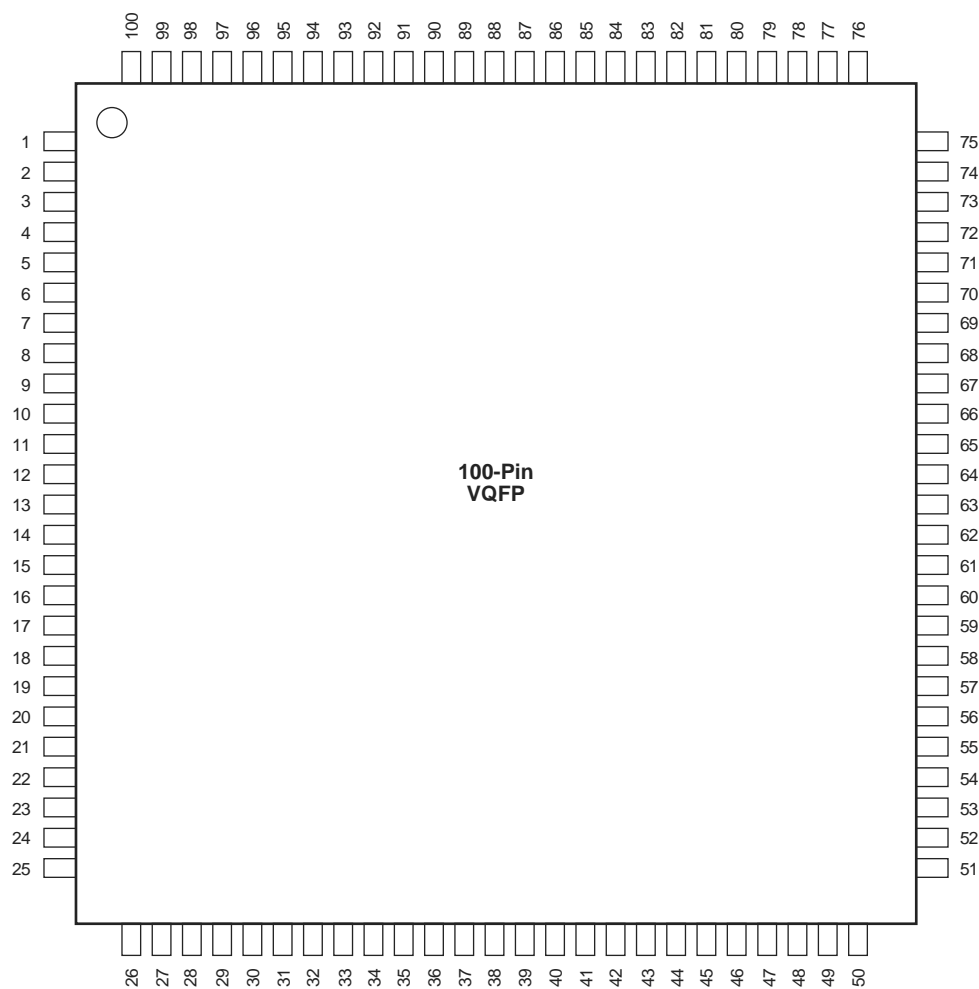
PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
1	GND	GND
2	SDI, I/O	SDI, I/O
11	MODE	MODE
12	VCC	VCC
25	VCC	VCC
26	GND	GND
27	VCC	VCC
28	GND	GND
40	VCC	VCC
41	VCC	VCC
52	GND	GND
53	NC	I/O
60	VCC	VCC
65	NC	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	VCC	VCC
79	GND	GND
80	VCC	VCC
82	HCLK, I/O	HCLK, I/O
98	VCC	VCC
102	NC	I/O
103	SDO	SDO
104	IOPCL, I/O	IOPCL, I/O
105	GND	GND
114	VCC	VCC

PQ208, RQ208		
Pin Number	A1460, A14V60 Function	A14100, A14V100 Function
115	VCC	VCC
116	NC	I/O
129	GND	GND
130	VCC	VCC
131	GND	GND
132	VCC	VCC
145	VCC	VCC
146	GND	GND
147	NC	I/O
148	VCC	VCC
156	IOCLK, I/O	IOCLK, I/O
157	GND	GND
158	NC	I/O
164	VCC	VCC
180	CLKA, I/O	CLKA, I/O
181	CLKB, I/O	CLKB, I/O
182	VCC	VCC
183	GND	GND
184	VCC	VCC
185	GND	GND
186	PRA, I/O	PRA, I/O
195	NC	I/O
201	VCC	VCC
205	NC	I/O
208	DCLK, I/O	DCLK, I/O

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## VQ100



*Note:* This is the top view.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>

CQ256	
Pin Number	A14100 Function
1	GND
2	SDI, I/O
11	MODE
28	VCC
29	GND
30	VCC
31	GND
46	VCC
59	GND
90	PRB, I/O
91	GND
92	VCC
93	GND
94	VCC
96	HCLK, I/O
110	GND
126	SDO
127	IOPCL, I/O
128	GND

CQ256	
Pin Number	A14100 Function
141	VCC
158	GND
159	VCC
160	GND
161	VCC
174	VCC
175	GND
176	GND
188	IOCLK, I/O
189	GND
219	CLKA, I/O
220	CLKB, I/O
221	VCC
222	GND
223	VCC
224	GND
225	PRA, I/O
240	GND
256	DCLK, I/O

**Notes:**

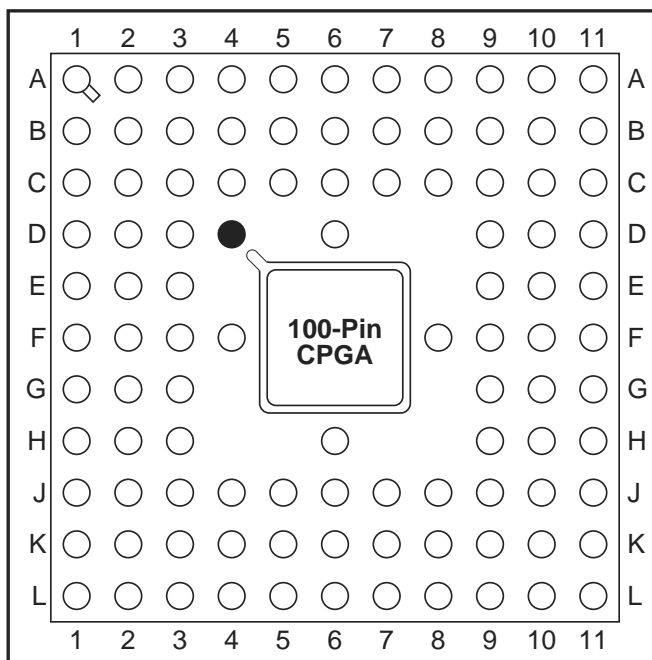
1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

BG313	
A14100, A14V100 Function	Location
CLKA or I/O	J13
CLKB or I/O	G13
DCLK or I/O	B2
GND	A1, A25, AD2, AE25, J21, L13, M12, M14, N11, N13, N15, P12, P14, R13
HCLK or I/O	T14
IOCLK or I/O	B24
IOPCL or I/O	AD24
MODE	G3
NC	A3, A13, A23, AA5, AA9, AA23, AB2, AB4, AB20, AC13, AC25, AD22, AE1, AE21, B14, C5, C25, D4, D24, E3, E21, F6, F10, F16, G1, G25, H18, H24, J1, J7, J25, K12, L15, L17, M6, N1, N5, N7, N21, N23, P20, R11, T6, T8, U9, U13, U21, V16, W7, Y20, Y24
PRA or I/O	H12
PRB or I/O	AD12
SDI or I/O	C1
SDO	AE23
VCC	AB18, AD6, AE13, C13, C19, E13, G9, H22, K8, K20, M16, N3, N9, N25, U5, W13, V2, V22, V24

*Notes:*

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

## PG100



● Orientation Pin

*Note: This is the top view.*

### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>



PG207	
A1460 Function	Location
CLKA or I/O	K1
CLKB or I/O	J3
DCLK or I/O	E4
GND	C14, D4, D5, D9, D14, J4, J14, P3, P4, P7, P9, P14, R15
HCLK or I/O	J15
IOCLK or I/O	P5
IOPCL or I/O	N14
MODE	D7
NC	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA or I/O	H1
PRB or I/O	K16
SDI or I/O	C3
SDO	P15
VCC	B2, B9, B16, D11, J2, J16, P12, S2, S9, S16, T5

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.

PG257	
A14100 Function	Location
CLKA or I/O	L4
CLKB or I/O	L5
DCLK or I/O	E4
GND	B16, C4, D4, D10, D16, E11, J5, K4, K16, L15, R4, T4, T10, T16, T17, X7
HCLK or I/O	J16
IOCLK or I/O	T5
IOPCL or I/O	R16
MODE	A5
NC	E5
PRA or I/O	J1
PRB or I/O	J17
SDI or I/O	B4
SDO	R17
VCC	C3, C10, C13, C17, K3, K17, V3, V7, V10, V17, X14

**Notes:**

1. All unlisted pin numbers are user I/Os.
2. NC denotes no connection.
3. MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage; otherwise it can be terminated directly to GND.



## 4 – Datasheet Information

### List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 3 (January 2012)	The description for SDO pins had earlier been removed from the datasheet and has now been included again, in the "Pin Descriptions" section (SAR 35820).	2-21
	SDO pin numbers had earlier been removed from package pin assignment tables in the datasheet, and have now been restored to the pin tables (SAR 35820).	3-1
Revision 2 (September 2011)	The ACT 3 datasheet was formatted newly in the style used for current datasheets. The same information is present (other than noted in the list of changes for this revision) but divided into chapters.	N/A
	The datasheet was revised to note in multiple places that speed grades –2 and –3 have been discontinued. The following device/package combinations have been discontinued for all speed grades and temperatures (SAR 33872): A1415 PG100 A1425 PG133 A1440 PG175 A1460 BG225 Refer to PDN 0104, PDN 0203, PDN 0604, and PDN 1004.	I and others
	The "Features" section was revised to state the clock-to-output time and on-chip performance for –1 speed grade as 9.0 ns and 186 MHz. The "General Description" section was revised in accordance (SAR 33872).	I
	The maximum performance values were updated in Table 1 • ACT 3 Family Product Information, and now reflect worst-case commercial for the –1 speed grade (SAR 33872).	I
	The "Product Plan" table was updated as follows to conform to current offerings (SAR 33872): The A1415A device is offered in PL84, PG100, and VQ100 packages for Military application. The A1440A device is offered in TQ176 and VQ100 packages for Industrial application.	III
	Table 1-1 • Chip-to-Chip Performance (worst-case commercial) was updated to include data for all speed grades instead of only –3 (SAR 33872).	1-2
	Figure 1-1 • Predictable Performance (worst-case commercial, –1 speed grade) was revised to reflect values for the –1 speed grade (SAR 33872).	1-1
	Figure 2-10 • Timing Model was updated to show data for the –1 speed grade instead of –3 (SAR 33872).	2-16
	Table 2-14 • Logic Module and Routing Delay by Fanout (ns); Worst-Case Commercial Conditions was updated to include data for all speed grades instead of only –3 (SAR 33872).	2-20
	Package names used in the "Package Pin Assignments" section and throughout the document were revised to match standards given in <i>Package Mechanical Drawings</i> (SAR 27395).	3-1



**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo CA 92656 USA  
Within the USA: +1 (949) 380-6100  
Sales: +1 (949) 380-6136  
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at [www.microsemi.com](http://www.microsemi.com).

© 2012 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.