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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8620t-i-pt

4.0 MEMORY ORGANIZATION

There are three memory blocks in PIC18FXX20 devices. They are:

- Program Memory
- Data RAM
- Data EEPROM

Data and program memory use separate busses, which allows for concurrent access of these blocks. Additional detailed information for Flash program memory and data EEPROM is provided in **Section 5.0 "Flash Program Memory"** and **Section 7.0 "Data EEPROM Memory"**, respectively.

In addition to on-chip Flash, the PIC18F8X20 devices are also capable of accessing external program memory through an external memory bus. Depending on the selected operating mode (discussed in **Section 4.1.1 "PIC18F8X20 Program Memory Modes"**), the controllers may access either internal or external program memory exclusively, or both internal and external memory in selected blocks. Additional information on the External Memory Interface is provided in **Section 6.0 "External Memory Interface"**.

4.1 Program Memory Organization

A 21-bit program counter is capable of addressing the 2-Mbyte program memory space. Accessing a location between the physically implemented memory and the 2-Mbyte address will cause a read of all '0's (a NOP instruction).

Devices in the PIC18FXX20 family can be divided into three groups, based on program memory size. The PIC18FX520 devices (PIC18F6520 and PIC18F8520) have 32 Kbytes of on-chip Flash memory, equivalent to 16,384 single-word instructions. The PIC18FX620 devices (PIC18F6620 and PIC18F8620) have 64 Kbytes of on-chip Flash memory, equivalent to 32,768 single-word instructions. Finally, the PIC18FX720 devices (PIC18F6720 and PIC18F8720) have 128 Kbytes of on-chip Flash memory, equivalent to 65,536 single-word instructions.

For all devices, the Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for all of the PIC18FXX20 devices are compared in Figure 4-1.

4.1.1 PIC18F8X20 PROGRAM MEMORY MODES

PIC18F8X20 devices differ significantly from their PIC18 predecessors in their utilization of program memory. In addition to available on-chip Flash program memory, these controllers can also address up to 2 Mbytes of external program memory through the External Memory Interface. There are four distinct operating modes available to the controllers:

- Microprocessor (MP)
- Microprocessor with Boot Block (MPBB)
- Extended Microcontroller (EMC)
- Microcontroller (MC)

The Program Memory mode is determined by setting the two Least Significant bits of the CONFIG3L configuration byte, as shown in Register 4-1. (See also **Section 23.1 "Configuration Bits"** for additional details on the device configuration bits.)

The Program Memory modes operate as follows:

- The **Microprocessor Mode** permits access only to external program memory; the contents of the on-chip Flash memory are ignored. The 21-bit program counter permits access to a 2-Mbyte linear program memory space.
- The **Microprocessor with Boot Block Mode** accesses on-chip Flash memory from addresses 000000h to 0007FFh for PIC18F8520 devices and from 000000h to 0001FFh for PIC18F8620 and PIC18F8720 devices. Above this, external program memory is accessed all the way up to the 2-Mbyte limit. Program execution automatically switches between the two memories, as required.
- The **Microcontroller Mode** accesses only on-chip Flash memory. Attempts to read above the physical limit of the on-chip Flash (7FFFh for the PIC18F8520, 0FFFFh for the PIC18F8620, 1FFFFh for the PIC18F8720) causes a read of all '0's (a NOP instruction). The Microcontroller mode is also the only operating mode available to PIC18F6X20 devices.
- The **Extended Microcontroller Mode** allows access to both internal and external program memories as a single block. The device can access its entire on-chip Flash memory; above this, the device accesses external program memory up to the 2-Mbyte program space limit. As with Boot Block mode, execution automatically switches between the two memories, as required.

In all modes, the microcontroller has complete access to data RAM and EEPROM.

Figure 4-2 compares the memory maps of the different Program Memory modes. The differences between on-chip and external memory access limitations are more fully explained in Table 4-1.

REGISTER 4-1: CONFIG3L CONFIGURATION BYTE

R/P-1	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
WAIT	—	—	—	—	—	PM1	PM0
bit 7							bit 0

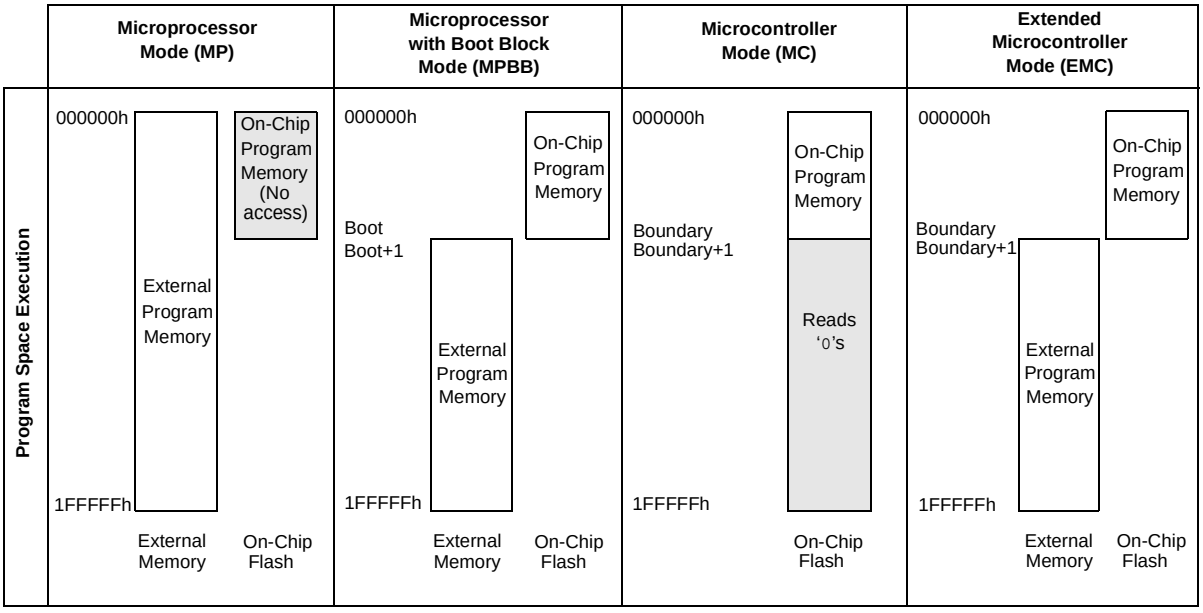
bit 7 **WAIT:** External Bus Data Wait Enable bit
1 = Wait selections unavailable, device will not wait
0 = Wait programmed by WAIT1 and WAIT0 bits of MEMCOM register (MEMCOM<5:4>)

bit 6-2 **Unimplemented:** Read as '0'

bit 1-0 **PM1:PM0:** Processor Data Memory Mode Select bits
11 = Microcontroller mode
10 = Microprocessor mode
01 = Microcontroller with Boot Block mode
00 = Extended Microcontroller mode

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
- n = Value after erase	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

FIGURE 4-2: MEMORY MAPS FOR PIC18F8X20 PROGRAM MEMORY MODES



Boundary Values for Microprocessor with Boot Block, Microcontroller and Extended Microcontroller modes(1)

Device	Boot	Boot+1	Boundary	Boundary+1	Available Memory Mode(s)
PIC18F6520	0007FFh	000800h	007FFFh	008000h	MC
PIC18F6620	0001FFh	000200h	00FFFFh	010000h	MC
PIC18F6720	0001FFh	000200h	01FFFFh	020000h	MC
PIC18F8520	0007FFh	000800h	007FFFh	008000h	MP, MPBB, MC, EMC
PIC18F8620	0001FFh	000200h	00FFFFh	010000h	MP, MPBB, MC, EMC
PIC18F8720	0001FFh	000200h	01FFFFh	020000h	MP, MPBB, MC, EMC

Note 1: PIC18F6X20 devices are included here for completeness, to show the boundaries of their Boot Blocks and program memory spaces.

TABLE 4-3: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
LATJ(3)	Read PORTJ Data Latch, Write PORTJ Data Latch								xxxx xxxx	35, 125
LATH(3)	Read PORTH Data Latch, Write PORTH Data Latch								xxxx xxxx	35, 122
LATG	—	—	—	Read PORTG Data Latch, Write PORTG Data Latch					---x xxxx	35, 120
LATF	Read PORTF Data Latch, Write PORTF Data Latch								xxxx xxxx	35, 117
LATE	Read PORTE Data Latch, Write PORTE Data Latch								xxxx xxxx	35, 114
LATD	Read PORTD Data Latch, Write PORTD Data Latch								xxxx xxxx	35, 111
LATC	Read PORTC Data Latch, Write PORTC Data Latch								xxxx xxxx	35, 109
LATB	Read PORTB Data Latch, Write PORTB Data Latch								xxxx xxxx	35, 106
LATA	—	LATA6(1)	Read PORTA Data Latch, Write PORTA Data Latch(1)						-xxx xxxx	35, 103
PORTJ(3)	Read PORTJ pins, Write PORTJ Data Latch								xxxx xxxx	36, 125
PORTH(3)	Read PORTH pins, Write PORTH Data Latch								xxxx xxxx	36, 122
PORTG	—	—	—	Read PORTG pins, Write PORTG Data Latch					---x xxxx	36, 120
PORTF	Read PORTF pins, Write PORTF Data Latch								xxxx xxxx	36, 117
PORTE	Read PORTE pins, Write PORTE Data Latch								xxxx xxxx	36, 114
PORTD	Read PORTD pins, Write PORTD Data Latch								xxxx xxxx	36, 111
PORTC	Read PORTC pins, Write PORTC Data Latch								xxxx xxxx	36, 109
PORTB	Read PORTB pins, Write PORTB Data Latch								xxxx xxxx	36, 106
PORTA	—	RA6(1)	Read PORTA pins, Write PORTA Data Latch(1)						-x0x 0000	36, 103
TMR4	Timer4 Register								0000 0000	36, 148
PR4	Timer4 Period Register								1111 1111	36, 148
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	36, 147
CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxx xxxx	36, 151, 152
CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxx xxxx	36, 151, 152
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	0000 0000	36, 149
CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxx xxxx	36, 151, 152
CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxx xxxx	36, 151, 152
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	0000 0000	36, 149
SPBRG2	USART2 Baud Rate Generator								0000 0000	36, 205
RCREG2	USART2 Receive Register								0000 0000	36, 206
TXREG2	USART2 Transmit Register								0000 0000	36, 204
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	36, 198
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	36, 199

Legend: x = unknown, u = unchanged, – = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO Oscillator modes only and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

3: These registers are unused on PIC18F6X20 devices; always maintain these clear.