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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.75K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf6620-i-pt

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TABLE 3-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator	Power-up	(2)	D	Wake-up from
Configuration	PWRTE = 0	PWRTE = 1	Brown-out	Sleep or Oscillator Switch
HS with PLL enabled ⁽¹⁾	72 ms + 1024 Tosc + 2ms	1024 Tosc + 2 ms	72 ms ⁽²⁾ + 1024 Tosc + 2 ms	1024 Tosc + 2 ms
HS, XT, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms ⁽²⁾ + 1024 Tosc	1024 Tosc
EC	EC 72 ms 1.5 μs		72 ms ⁽²⁾	1.5 μs ⁽³⁾
External RC	External RC 72 ms —		72 ms ⁽²⁾	—

Note 1: 2 ms is the nominal time required for the 4xPLL to lock.

2: 72 ms is the nominal power-up timer delay, if implemented.

3: 1.5 µs is the recovery time from Sleep. There is no recovery time from oscillator switch.

REGISTER 3-1:	RCON REGISTER BITS AND POSITIONS
---------------	----------------------------------

R/W-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IPEN	_	—	RI	TO	PD	POR	BOR
bit 7							bit 0

Note 1: Refer to Section 4.14 "RCON Register" for bit definitions.

TABLE 3-2:STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR
RCON REGISTER

Condition	Program Counter	RCON Register	RI	то	PD	POR	BOR	STKFUL	STKUNF
Power-on Reset	0000h	01 1100	1	1	1	0	0	u	u
MCLR Reset during normal operation	0000h	0u uuuu	u	u	u	u	u	u	u
Software Reset during normal operation	0000h	00 uuuu	0	u	u	u	u	u	u
Stack Full Reset during normal operation	0000h	0u uull	u	u	u	u	u	u	1
Stack Underflow Reset during normal operation	0000h	0u uull	u	u	u	u	u	1	u
MCLR Reset during Sleep	0000h	0u 10uu	u	1	0	u	u	u	u
WDT Reset	0000h	0u 01uu	1	0	1	u	u	u	u
WDT Wake-up	PC + 2	uu 00uu	u	0	0	u	u	u	u
Brown-out Reset	0000h	01 11u0	1	1	1	1	0	u	u
Interrupt wake-up from Sleep	PC + 2 ⁽¹⁾	uu 00uu	u	1	0	u	u	u	u

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (0x000008h or 0x000018h).



FIGURE 3-7:TIME-OUT SEQUENCE ON POR W/PLL ENABLED
(MCLR TIED TO VDD VIA 1 k Ω RESISTOR)



File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
CCPR3H	Capture/Cor	mpare/PWM R	egister 3 Higł	n Byte					XXXX XXXX	34, 151, 152
CCPR3L	Capture/Cor	mpare/PWM R	egister 3 Low	y Byte				_	XXXX XXXX	34, 151, 152
CCP3CON		_	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	00 0000	34, 149
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	34, 229
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	34, 223
TMR3H	Timer3 Regi	ster High Byte							xxxx xxxx	34, 143
TMR3L	Timer3 Regi	ster Low Byte	r	1				T	xxxx xxxx	34, 143
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	34, 143
PSPCON	IBF	OBF	IBOV	PSPMODE	_	—	_	—	0000	34, 129
SPBRG1	USART1 Ba	ud Rate Gene	rator						0000 0000	34, 205
RCREG1	USART1 Re	ceive Registe	r						0000 0000	34, 206
TXREG1	USART1 Tra	ansmit Registe	r						0000 0000	34, 204
TXSTA1	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	34, 198
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	34, 199
EEADRH	—	—	—	—	_	—	EE Adr Reg	gister High	00	34, 79
EEADR	Data EEPROM Address Register								0000 0000	34, 79
EEDATA	Data EEPRO	OM Data Regis	ster						0000 0000	34, 79
EECON2	Data EEPRO	OM Control Re	egister 2 (not a	a physical regi	ster)					34, 79
EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	34, 80
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	11 1111	35, 100
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	00 0000	35, 94
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	00 0000	35, 97
IPR2	—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	-1-1 1111	35, 99
PIR2	—	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-0 0000	35, 93
PIE2	—	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-0 0000	35, 96
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	35, 98
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	35, 92
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	35, 95
MEMCON ⁽³⁾	EBDIS	—	WAIT1	WAIT0	_	—	WM1	WM0	0-0000	35, 71
TRISJ ⁽³⁾	Data Direction	on Control Reg	gister for POR	TJ					1111 1111	35, 125
TRISH ⁽³⁾	Data Direction	on Control Reg	gister for POR	TH					1111 1111	35, 122
TRISG	—	—	—	Data Directio	n Control Reg	ister for PORT	G		1 1111	35, 120
TRISF	Data Direction	on Control Reg	gister for POR	TF					1111 1111	35, 117
TRISE	Data Direction	on Control Reg	gister for POR	TE					1111 1111	35, 114
TRISD	Data Direction	on Control Reg	gister for POR	TD					1111 1111	35, 111
TRISC	Data Direction	on Control Reg	gister for POR	TC					1111 1111	35, 109
TRISB	Data Direction	on Control Reg	gister for POR	TB					1111 1111	35, 106
TRISA	_	TRISA6 ⁽¹⁾	Data Directio	on Control Reg	ister for POR	ГА			-111 1111	35, 103

TABLE 4-3: REGISTER FILE SUMMARY (CONTINUED)

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO Oscillator modes only and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

3: These registers are unused on PIC18F6X20 devices; always maintain these clear.

Example 8-3 shows the sequence to do a 16 x 16 unsigned multiply. Equation 8-1 shows the algorithm that is used. The 32-bit result is stored in four registers, RES3:RES0.

EQUATION 8-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

RES3:RES0	=	ARG1H:ARG1L • ARG2H:ARG2L
	=	$(ARG1H \bullet ARG2H \bullet 2^{16}) +$
		$(ARG1H \bullet ARG2L \bullet 2^8) +$
		$(ARG1L \bullet ARG2H \bullet 2^8) +$
		$(ARG1L \bullet ARG2L)$

EXAMPLE 8-3: 16 x 16 UNSIGNED MULTIPLY ROUTINE

	MOVF	ARG1L, W	
	MULWF	ARG2L	; ARG1L * ARG2L ->
			; PRODH:PRODL
	MOVFF	PRODH, RES1	;
	MOVFF	PRODL, RESO	;
;			
	MOVF	ARG1H, W	
	MULWF	ARG2H	; ARG1H * ARG2H ->
			; PRODH:PRODL
	MOVFF	PRODH, RES3	;
	MOVFF	PRODL, RES2	;
;			
	MOVF	ARG1L, W	
	MULWF	ARG2H	; ARG1L * ARG2H ->
			; PRODH:PRODL
	MOVF	PRODL, W	;
	ADDWF	RES1, F	; Add cross
	MOVF	PRODH, W	; products
	ADDWFC	RES2, F	;
	CLRF	WREG	;
	ADDWFC	RES3, F	;
;			
	MOVF	ARG1H, W	;
	MULWF	ARG2L	; ARG1H * ARG2L ->
			; PRODH:PRODL
	MOVF	PRODL, W	;
	ADDWF	RES1, F	; Add cross
	MOVE	PRODH, W	; products
	ADDWFC	RESZ, F	;
	CLRF	WKEG	;
	ADDWFC	KES3, F	;

Example 8-4 shows the sequence to do a 16 x 16 signed multiply. Equation 8-2 shows the algorithm used. The 32-bit result is stored in four registers, RES3:RES0. To account for the sign bits of the arguments, each argument pairs' Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EQUATION 8-2: 16 x 16 SIGNED MULTIPLICATION

RES3:RI	ES0
=	A

0 ARG1H:ARG1L • ARG2H:ARG2L

=	$(ARG1H \bullet ARG2H \bullet 2^{16}) +$
	$(ARG1H \bullet ARG2L \bullet 2^8) +$
	$(ARG1L \bullet ARG2H \bullet 2^8) +$
	$(ARG1L \bullet ARG2L) +$
	$(-1 \bullet ARG2H < 7 > \bullet ARG1H: ARG1L \bullet 2^{16}) +$
	$(-1 \bullet ARG1H < 7 > \bullet ARG2H: ARG2L \bullet 2^{16})$

EXAMPLE 8-4: 16 x 16 SIGNED MULTIPLY ROUTINE

	MOVF	ARG1L, W	
	MULWF	ARG2L	; ARG1L * ARG2L ->
			; PRODH:PRODL
	MOVFF	PRODH, RES1	;
	MOVFF	PRODL, RESO	;
;			
	MOVF	ARG1H, W	
	MULWF	ARG2H	; ARG1H * ARG2H ->
			; PRODH:PRODL
	MOVFF	PRODH, RES3	;
	MOVFF	PRODL, RES2	;
;			
	MOVF	ARG1L, W	
	MULWF	ARG2H	; ARG1L * ARG2H ->
			; PRODH:PRODL
	MOVF	PRODL, W	;
	ADDWF	RES1, F	; Add cross
	MOVF	PRODH, W	; products
	ADDWFC	RES2, F	;
	CLRF	WREG	;
	ADDWFC	RES3, F	;
;			
	MOVF	ARG1H, W	;
	MULWF	ARG2L	; ARG1H * ARG2L ->
			; PRODH:PRODL
	MOVF	PRODL, W	;
	ADDWF	RES1, F	; Add cross
	MOVF	PRODH, W	; products
	ADDWFC	RES2, F	;
	CLRF	WREG	;
	ADDWFC	RES3, F	;
;			
	BTFSS	ARG2H, 7	; ARG2H:ARG2L neg?
	BRA	SIGN ARG1	; no, check ARG1
	MOVF	ARG1L, W	;
	SUBWF	RES2	;
	MOVF	ARG1H, W	;
	SUBWFB	RES3	
;			
SIG	N_ARG1		
	BTFSS	ARG1H, 7	; ARG1H:ARG1L neg?
	BRA	CONT_CODE	; no, done
	MOVF	ARG2L, W	;
	SUBWF	RES2	;
	MOVF	ARG2H, W	;
	SUBWFB	RES3	
;			
CON	T_CODE		
	:		

EGISTER 9-6: PIR3: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 3									
	U-0	U-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
			RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	
	bit 7							bit 0	
bit 7- 6	Unimplem	ented: Rea	d as '0'						
bit 5	RC2IF: US	ART2 Rece	ive Interrupt	t Flag bit					
	1 = The U 0 = The U	 1 = The USART2 receive buffer, RCREG, is full (cleared when RCREG is read) 0 = The USART2 receive buffer is empty 							
bit 4	TX2IF: US	ART2 Trans	mit Interrup	t Flag bit					
	 1 = The USART2 transmit buffer, TXREG, is empty (cleared when TXREG is written) 0 = The USART2 transmit buffer is full 								
bit 3	TMR4IF: T	MR3 Overfl	ow Interrupt	Flag bit					
	 1 = TMR4 register overflowed (must be cleared in software) 0 = TMR4 register did not overflow 								
bit 2-0	CCPxIF: C	CPx Interru	pt Flag bit (0	CCP Module	s 3, 4 and 5)			
	<u>Capture mode:</u> 1 = A TMR1 or TMR3 register capture occurred (must be cleared in software) 0 = No TMR1 or TMR3 register capture occurred								
	Compare mode: 1 = A TMR1 or TMR3 register compare match occurred (must be cleared in software) 0 = No TMR1 or TMR3 register compare match occurred								
<u>PWM mode:</u> Unused in this mode.									
	Legend:								
	R – Readable bit W – Writable bit II – Unimplemented bit read as '0'								

R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

10.0 I/O PORTS

Depending on the device selected, there are either seven or nine I/O ports available on PIC18FXX20 devices. Some of their pins are multiplexed with one or more alternate functions from the other peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch (LAT register) is useful for read-modifywrite operations on the value that the I/O pins are driving.

A simplified version of a generic I/O port and its operation is shown in Figure 10-1.

FIGURE 10-1: SIMPLIFIED BLOCK DIAGRAM OF PORT/LAT/ TRIS OPERATION



10.1 PORTA, TRISA and LATA Registers

PORTA is a 7-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register, read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open-drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

The RA6 pin is only enabled as a general I/O pin in ECIO and RCIO Oscillator modes.

The other PORTA pins are multiplexed with analog inputs and the analog VREF+ and VREF- inputs. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note:	On a Power-on Reset, RA5 and RA3:RA0							
	are configured as analog inputs and read							
	as '0'. RA6 and RA4 are configured as							
	digital inputs.							

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

CLRF	PORTA	; Initialize PORTA by
		; clearing output
		; data latches
CLRF	LATA	; Alternate method
		; to clear output
		; data latches
MOVLW	0x0F	; Configure A/D
MOVWF	ADCON1	; for digital inputs
MOVLW	0xCF	; Value used to
		; initialize data
		; direction
MOVWF	TRISA	; Set RA<3:0> as inputs
		; RA<5:4> as outputs
1		





I/O pins have diode protection to VDD and VSS.

SS Input

Note:

11.0 TIMER0 MODULE

The Timer0 module has the following features:

- Software selectable as an 8-bit or 16-bit timer/counter
- Readable and writable
- Dedicated 8-bit software programmable prescaler
- · Clock source selectable to be external or internal
- Interrupt-on-overflow from FFh to 00h in 8-bit mode and FFFFh to 0000h in 16-bit mode
- Edge select for external clock

Figure 11-1 shows a simplified block diagram of the Timer0 module in 8-bit mode and Figure 11-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

The T0CON register (Register 11-1) is a readable and writable register that controls all the aspects of Timer0, including the prescale selection.

REGISTER 11-1:	T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	TOCS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

- bit 7 TMR0ON: Timer0 On/Off Control bit
 - 1 = Enables Timer0
 - 0 = Stops Timer0
- bit 6 **T08BIT:** Timer0 8-bit/16-bit Control bit
 - 1 = Timer0 is configured as an 8-bit timer/counter
 - 0 = Timer0 is configured as a 16-bit timer/counter
- bit 5 **TOCS:** Timer0 Clock Source Select bit
 - 1 = Transition on TOCKI pin
 - 0 = Internal instruction cycle clock (CLKO)
- bit 4 TOSE: Timer0 Source Edge Select bit
 - 1 = Increment on high-to-low transition on T0CKI pin
 - 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA:** Timer0 Prescaler Assignment bit
 - 1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
 - 0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.
- bit 2-0 TOPS2:TOPS0: Timer0 Prescaler Select bits
 - 111 = 1:256 prescale value
 - 110 = 1:128 prescale value
 - 101 = 1:64 prescale value
 - 100 = 1:32 prescale value
 - 011 = 1:16 prescale value
 - 010 = 1:8 prescale value
 - 001 = 1:4 prescale value
 - 000 = 1:2 prescale value

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	oit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

16.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCPxCON) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte). All registers are both readable and writable.

16.1.1 CCP MODULES AND TIMER RESOURCES

The CCP modules utilize Timers 1, 2, 3 or 4, depending on the mode selected. Timer1 and Timer3 are available to modules in Capture or Compare modes, while Timer2 and Timer4 are available for modules in PWM mode.

TABLE 16-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3

The assignment of a particular timer to a module is determined by the Timer-to-CCP Enable bits in the T3CON register (Register 14-1). Depending on the configuration selected, up to four timers may be active at once, with modules in the same configuration (Capture/Compare or PWM) sharing timer resources. The possible configurations are shown in Figure 16-1.

FIGURE 16-1: CCP AND TIMER INTERCONNECT CONFIGURATIONS







T3CCP<2:1> = 10



T3CCP<2:1> = 11

Timer1 is used for all Capture and Compare operations for all CCP modules. Timer2 is used for PWM operations for all CCP modules. Modules may share either timer resource as a common time base.

Timer3 and Timer4 are not available.

Timer1 and Timer2 are used for Capture and Compare or PWM operations for CCP1 only (depending on selected mode).

All other modules use either Timer3 or Timer4. Modules may share either timer resource as a common time base, if they are in Capture/ Compare or PWM modes. Timer1 and Timer2 are used for Capture and Compare or PWM operations for CCP1 and CCP2 only (depending on the mode selected for each module). Both modules may use a timer as a common time base if they are both in Capture/Compare or PWM modes.

The other modules use either Timer3 or Timer4. Modules may share either timer resource as a common time base if they are in Capture/ Compare or PWM modes. Timer3 is used for all Capture and Compare operations for all CCP modules. Timer4 is used for PWM operations for all CCP modules. Modules may share either timer resource as a common time base.

Timer1 and Timer2 are not available.

17.4.7 BAUD RATE GENERATOR

In I²C Master mode, the Baud Rate Generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 17-17). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting. The BRG counts down to '0' and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TcY) on the Q2 and Q4 clocks. In I²C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 15-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

FIGURE 17-17: BAUD RATE GENERATOR BLOCK DIAGRAM



TABLE 17-3: I²C CLOCK RATE W/BRG

Fcy	Fcy*2	BRG VALUE	FscL (2 rollovers of BRG)
10 MHz	20 MHz	19h	400 kHz ⁽¹⁾
10 MHz	20 MHz	20h	312.5 kHz
10 MHz	20 MHz	3Fh	100 kHz
4 MHz	8 MHz	0Ah	400 kHz ⁽¹⁾
4 MHz	8 MHz	0Dh	308 kHz
4 MHz	8 MHz	28h	100 kHz
1 MHz	2 MHz	03h	333 kHz ⁽¹⁾
1 MHz	2 MHz	0Ah	100 kHz
1 MHz	2 MHz	00h	1 MHz ⁽¹⁾

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

18.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USARTs. It is a dedicated 8-bit Baud Rate Generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTAx<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 18-1 shows the formula for computation of the baud rate for different USART modes, which only apply in Master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRGx register can be calculated using the formula in Table 18-1. From this, the error in baud rate can be determined. Example 18-1 shows the calculation of the baud rate error for the following conditions:

- Fosc = 16 MHz
- Desired Baud Rate = 9600
- BRGH = 0
- SYNC = 0

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the equation in Example 18-1 can reduce the baud rate error in some cases.

Writing a new value to the SPBRGx register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

18.1.1 SAMPLING

The data on the RXx pin (either RC7/RX1/DT1 or RG2/ RX2/DT2) is sampled three times by a majority detect circuit to determine if a high or a low level is present at the pin.

EXAMPLE 18-1: CALCULATING BAUD RATE ERROR

Desired Baud Rate	= Fosc/(64 (X + 1))
Solving for X:	
X X X	= ((Fosc/Desired Baud Rate)/64) - 1 = ((16000000/9600)/64) - 1 = [25.042] = 25
Calculated Baud Rate	= 1600000/(64(25+1)) = 9615
Error	 <u>(Calculated Baud Rate – Desired Baud Rate)</u> Desired Baud Rate (9615 – 9600)/9600 0.16%

TABLE 18-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X + 1))	Baud Rate = Fosc/(16(X + 1))
1	(Synchronous) Baud Rate = FOSC/(4(X + 1))	N/A

Legend: X = value in SPBRGx (0 to 255)

TABLE 18-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TXSTAx	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRGx Baud Rate Generator Register							0000 0000	0000 0000		

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and Reset values are identical between modules.

	1			i			· · · · · ·			1			
BAUD	Fosc = 40 MHz			33 MHz			25 MHz				20 MHz		
RATE (Kbps)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-	
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-	
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-	
9.6	NA	-	-	9.60	-0.07	214	9.59	-0.15	162	9.62	+0.16	129	
19.2	19.23	+0.16	129	19.28	+0.39	106	19.30	+0.47	80	19.23	+0.16	64	
76.8	75.76	-1.36	32	76.39	-0.54	26	78.13	+1.73	19	78.13	+1.73	15	
96	96.15	+0.16	25	98.21	+2.31	20	97.66	+1.73	15	96.15	+0.16	12	
300	312.50	+4.17	7	294.64	-1.79	6	312.50	+4.17	4	312.50	+4.17	3	
500	500	0	4	515.63	+3.13	3	520.83	+4.17	2	416.67	-16.67	2	
HIGH	2500	-	0	2062.50	-	0	1562.50	-	0	1250	-	0	
LOW	9.77	-	255	8,06	-	255	6.10	-	255	4.88	-	255	

TABLE 18-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD	F	osc = 16 N	ИHz		10 MHz			7.15909 MHz			5.0688 MHz		
RATE (Kbps)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-	
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-	
2.4	NA	-	-	NA	-	-	2.41	+0.23	185	2.40	0	131	
9.6	9.62	+0.16	103	9.62	+0.16	64	9.52	-0.83	46	9.60	0	32	
19.2	19.23	+0.16	51	18.94	-1.36	32	19.45	+1.32	22	18.64	-2.94	16	
76.8	76.92	+0.16	12	78.13	+1.73	7	74.57	-2.90	5	79.20	+3.13	3	
96	100	+4.17	9	89.29	-6.99	6	89.49	-6.78	4	105.60	+10.00	2	
300	333.33	+11.11	2	312.50	+4.17	1	447.44	+49.15	0	316.80	+5.60	0	
500	500	0	1	625	+25.00	0	447.44	-10.51	0	NA	-	-	
HIGH	1000	-	0	625	-	0	447.44	-	0	316.80	-	0	
LOW	3.91	-	255	2.44	-	255	1.75	-	255	1.24	-	255	

BAUD	Fosc = 4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
RATE (Kbps)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	0.30	+0.16	207	0.29	-2.48	6
1.2	1.20	+0.16	207	1.20	+0.23	185	1.20	+0.16	51	1.02	-14.67	1
2.4	2.40	+0.16	103	2.41	+0.23	92	2.40	+0.16	25	2.05	-14.67	0
9.6	9.62	+0.16	25	9.73	+1.32	22	8.93	-6.99	6	NA	-	-
19.2	19.23	+0.16	12	18.64	-2.90	11	20.83	+8.51	2	NA	-	-
76.8	NA	-	-	74.57	-2.90	2	62.50	-18.62	0	NA	-	-
96	NA	-	-	111.86	+16.52	1	NA	-	-	NA	-	-
300	NA	-	-	223.72	-25.43	0	NA	-	-	NA	-	-
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-
HIGH	250	-	0	55.93	-	0	62.50	-	0	2.05	-	0
LOW	0.98	-	255	0.22	-	255	0.24	-	255	0.008	-	255

19.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 12 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 Tosc
- 4 Tosc
- 8 Tosc
- 16 Tosc
- 32 Tosc
- 64 Tosc
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 $\mu s.$

Table 19-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

19.3 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

- Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert as an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.
 - Analog levels on any pin defined as a digital input may cause the input buffer to consume current out of the device's specification limits.

TABLE 19-1: TAD VS. DEVICE OPERATING FREQUENCIES

AD Clock So	urce (TAD)	Maximum Device Frequency			
Operation	ADCS2:ADCS0	PIC18FXX20	PIC18LFXX20		
2 Tosc	000	1.25 MHz	666 kHz		
4 Tosc	100	2.50 MHz	1.33 MHz		
8 Tosc	001	5.00 MHz	2.67 MHz		
16 Tosc	101	10.0 MHz	5.33 MHz		
32 Tosc	010	20.0 MHz	10.67 MHz		
64 Tosc	110	40.0 MHz	21.33 MHz		
RC	x11	_	—		

19.4 A/D Conversions

Figure 19-3 shows the operation of the A/D converter after the GO bit has been set. Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2 TAD wait is required before the next acquisition is started. After this 2 TAD wait, acquisition on the selected channel is automatically started.

Note: The GO/DONE bit should NOT be set in the same instruction that turns on the A/D.

19.5 Use of the CCP2 Trigger

An A/D conversion can be started by the "special event trigger" of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/ DONE bit will be set, starting the A/D conversion and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH/ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the "special event trigger" sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

FIGURE 19-3: A/D CONVERSION TAD CYCLES

Tcy - Tad	TAD1	TAD2	TAD3	TAD4	TAD5	TAD6	TAD7	TAD8	TAD9	TAD10	TAD11		
↑ ↑ ↑	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	b0		
	Conver	sion sta	arts										
Holding	g capad	citor is	discon	nected	from a	inalog i	nput (t	ypically	/ 100 n	ıs)			
Set GO	bit			↓									
				Ne	xt Q4:	ADRE	SH/AD	RESL	is load	led, GC) bit is cl	cleared,	
						ADIF b	oit is se	et, hold	ing cap	cacitor	is conne	ected to analog inp	out.



FIGURE 21-1: VOLTAGE REFERENCE BLOCK DIAGRAM

21.2 Voltage Reference Accuracy/Error

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 21-1) keep CVREF from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the CVREF output changes with fluctuations in that source. The tested absolute accuracy of the voltage reference can be found in **Section 26.0 "Electrical Characteristics"**.

21.3 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

21.4 Effects of a Reset

A device Reset disables the voltage reference by clearing bit CVREN (CVRCON<7>). This Reset also disconnects the reference from the RA2 pin by clearing bit CVROE (CVRCON<6>) and selects the high-voltage range by clearing bit CVRR (CVRCON<5>). The VRSS value select bits, CVRCON<3:0>, are also cleared.

21.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RF5 pin if the TRISF<5> bit is set and the CVROE bit is set. Enabling the voltage reference output onto the RF5 pin, configured as a digital input, will increase current consumption. Connecting RF5 as a digital output with VRSS enabled will also increase current consumption.

The RF5 pin can be used as a simple D/A output with limited drive capability. Due to the limited current drive capability, a buffer must be used on the voltage reference output for external connections to VREF. Figure 21-2 shows an example buffering technique.

25.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

25.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

25.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions	
10	TosH2ckL	OSC1 \uparrow to CLKO \downarrow		—	75	200	ns	(Note 1)
11	TosH2ckH	OSC1 ↑ to CLKO ↑		—	75	200	ns	(Note 1)
12	ТскR	CLKO Rise Time		—	35	100	ns	(Note 1)
13	ТскF	CLKO Fall Time		—	35	100	ns	(Note 1)
14	TCKL2IOV	CLKO ↓ to Port Out Valid		—		0.5 TCY + 20	ns	(Note 1)
15	ТюV2скН	Port In Valid before CLKO 1	0.25 Tcy + 25		—	ns	(Note 1)	
16	TCKH2IOI	Port In Hold after CLKO ↑		0		—	ns	(Note 1)
17	TosH2IoV	OSC1 ↑ (Q1 cycle) to Port Out	_	50	150	ns		
18	TosH2iol	OSC1 ↑ (Q2 cycle) to Port	PIC18FXX20	100		—	ns	
18A		Input Invalid (I/O in hold time)	PIC18LFXX20	200		—	ns	VDD = 2.0V
19	TIOV20sH	Port Input Valid to OSC1 1 (I/C	in setup time)	0		—	ns	
20	TIOR	Port Output Rise Time	PIC18FXX20	—	10	25	ns	
20A			PIC18LFXX20	—	_	60	ns	VDD = 2.0V
21	TIOF	Port Output Fall Time	PIC18FXX20	—	10	25	ns	
21A			PIC18LFXX20	—		60	ns	VDD = 2.0V
22†	TINP	INT pin High or Low Time	Тсү		—	ns		
23†	Trbp	RB7:RB4 Change INT High or	Тсү	—	—	ns		
24†	TRCP	RC7:RC4 Change INT High or	Low Time	20		—	ns	

TABLE 26-8: CLKO AND I/O TIMING REQUIREMENTS

† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode, where CLKO output is 4 x Tosc.





Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
70	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK \downarrow or SCK \uparrow Input	Тсү		ns		
71	TscH	SCK Input High Time	Continuous	1.25 TCY + 30		ns	
71A		(Slave mode)	Single Byte	40		ns	(Note 1)
72	TscL	SCK Input Low Time	Continuous	1.25 TCY + 30		ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73	TDIV2SCH, TDIV2SCL	Setup Time of SDI Data Input to SC	100		ns		
73A	Тв2в	Last Clock Edge of Byte 1 to the 1st 0	1.5 Tcy + 40	_	ns	(Note 2)	
74	TscH2DIL, TscL2DIL	Hold Time of SDI Data Input to SCK	Edge	100		ns	
75	TDOR	SDO Data Output Rise Time	PIC18FXX20	—	25	ns	
			PIC18LFXX20	—	45	ns	VDD = 2.0V
76	TDOF	SDO Data Output Fall Time		—	25	ns	
78	TscR	SCK Output Rise Time	PIC18FXX20	—	25	ns	
		(Master mode)	PIC18LFXX20	—	45	ns	VDD = 2.0V
79	TscF	SCK Output Fall Time (Master mode	—	25	ns		
80	TscH2doV,	SDO Data Output Valid after SCK	PIC18FXX20	—	50	ns	
	TscL2doV	Edge	PIC18LFXX20	—	100	ns	VDD = 2.0V

TABLE 26-15.	EXAMPLE SPI MODE REQUIREMENTS	MASTER MODE CKE - 0	۱
IADLE 20-15.	EVAINIFLE SELINIODE KEROIKEINIEN 19	(WASTER WODE, CRE = 0)	,

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.





Param No.	Symbol	Characteristi	Min	Max	Units	Conditions	
71	TscH	SCK Input High Time	Continuous	1.25 TCY + 30		ns	
71A		(Slave mode)	Single Byte	40		ns	(Note 1)
72	TscL	SCK Input Low Time	Continuous	1.25 TCY + 30	—	ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73	TDIV2SCH, TDIV2SCL	Setup Time of SDI Data Input to S	100	_	ns		
73A	Тв2в	Last Clock Edge of Byte 1 to the 1st	1.5 Tcy + 40		ns	(Note 2)	
74	TscH2diL, TscL2diL	Hold Time of SDI Data Input to SC	100		ns		
75	TDOR	SDO Data Output Rise Time	PIC18FXX20	—	25	ns	
			PIC18LFXX20	—	45	ns	VDD = 2.0V
76	TDOF	SDO Data Output Fall Time		—	25	ns	
78	TscR	SCK Output Rise Time	PIC18FXX20	—	25	ns	
		(Master mode)	PIC18LFXX20	—	45	ns	VDD = 2.0V
79	TscF	SCK Output Fall Time (Master mo	de)	—	25	ns	
80	TscH2doV,	SDO Data Output Valid after SCK	PIC18FXX20	—	50	ns	
	TscL2doV	Edge	PIC18LFXX20	—	100	ns	VDD = 2.0V
81	TDOV2SCH, TDOV2SCL	SDO Data Output Setup to SCK E	DO Data Output Setup to SCK Edge			ns	

TABLE 26-16: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.





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