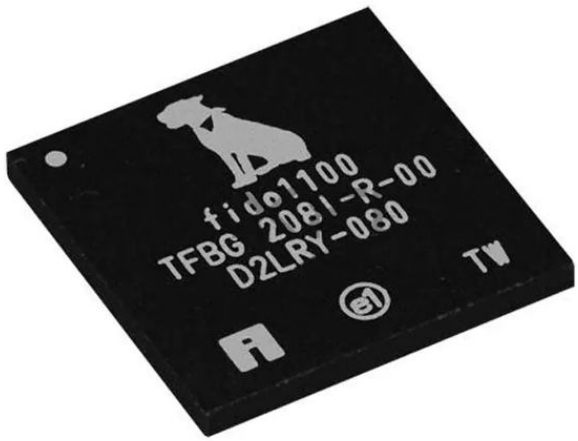

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	CPU32
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, EIA-232, Ethernet, GPIO, HDLC, I²C, SMBus, SPI
Peripherals	DMA, POR, WDT
Number of I/O	72
Program Memory Size	32KB (32K x 8)
Program Memory Type	RREM
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/fido1100bga208ir1

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2. Features

The fido1100 communication controller's features include:

- 32-bit Core CPU
- CISC architecture optimized for real time
- CPU32+ (Motorola® 68000) instruction-set compatible
- Five hardware contexts, each with its own register set and interrupt vector table
- An 8- or 16-bit external bus interface with programmable chip selects
- 24 Kbytes of high-speed internal user SRAM
- 32 Kbytes of high-speed internal user-mappable Relocatable Rapid Execution Memory (RREM)
- A Memory Protection Unit (MPU)
- An SDRAM controller
- Flat, contiguous memory space
- Non-aligned memory access support
- Dedicated Peripheral Management Unit (PMU)
- Four Universal I/O Controllers (UICs) capable of supporting the following protocols:
  - GPIO
  - 10/100 Ethernet with flexible MAC Address Filtering schemes
  - EIA-232
  - CAN
  - SPI
  - I^2C™ Bus
  - SMBus
  - HDLC
- Two channels of full-featured direct memory access (DMA) with deterministic arbitration
- Two Timer/Counter Units (TCU)
- A Watchdog timer, system timer, and context timers

- JTAG emulation and debug interface
- Available in a 208-pin PQFP, BGA 10- by 10-mm package, and BGA 15- by 15-mm package
- 3.3V operation with 5V-tolerant I/O
- Industrial temperature grade
- Software development supported by libraries and tools including UIC firmware for various interface protocols and formats, as well as a customized GNU tool set.

2.1 Core CPU

The fido1100 core is based on the CPU32 architecture, and is compatible with the CPU32 instruction set. The fido1100 incorporates five independent hardware contexts. While all contexts share the same Execution Unit, each of the five hardware contexts in the fido1100 has its own register set, execution priority and exception vector table. From an application's view, this unique feature of the fido1100 allows it to operate as five independent machines in one:

- 32-bit address and data paths on-chip
- 66-MHz operation
- Instruction execution from external memory or fast internal memory.
- Each hardware context has its own copy of:
  - Eight 32-bit User Data Registers (D0-D7)
  - Seven 32-bit Address Registers (A0-A6)
  - Two 32-bit Stack Pointers (A7 and A7')
  - One 32-bit Program Counter
  - One 16-bit Status Register (SR)
  - One 32-bit Vector Base Register (VBR)

2.2 JTAG

The fido1100 is fully compliant with the IEEE 1149.1 Test Access Port and Boundary-Scan architecture (see Table 2). The fido1100 architecture is equipped with the TAP (Test Access Port) interface, TAP controller, instruction register, instruction decoder, boundary-scan register, and by-pass register.

3. Libraries and Support Tools

- Full library support
- UIC libraries
- Embedded communication stacks
- TCP/IP
- GPIO sample programs
- Customized GNU tool set
- Eclipse IDE
- Sourcery G++ from Code Sourcery

4. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the fido1100 communication controller PQFP, BGA 10- by 10-mm package, and BGA 15- by 15-mm package is provided individually. Refer to sections, figures, and tables for information on the device of interest.

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
36	D12	Bidirectional	External Bus Interface data Bit [12]
37	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
38	D13	Bidirectional	External Bus Interface data Bit [13]
39	D14	Bidirectional	External Bus Interface data Bit [14]
40	D15	Bidirectional	External Bus Interface data Bit [15]
41	RDY_N	Input	External Bus Interface External Ready Indication
42	GND	Ground	Digital ground
43	MEMCLK	Output	Memory clock used by external memory
44	GND	Ground	Digital ground
45	BE0_N	Output	Byte enable 0, active low
46	BE1_N	Output	Byte enable 1, active low
47	OE_N	Output	Output enable, active low
48	VDDC	Power	Digital core supply voltage (+2.5VDC)
49	RW_N	Output	Read or write control (active low write)
50	BA_0	Output	Bank Enable 0
51	BA_1	Output	Bank Enable 1
52	CAS_N	Output	Column activate signal, active low
53	GND	Ground	Digital Ground
54	RAS_N	Output	Row activate signal, active low
55	CKE	Output	Clock enable to be used in conjunction with MEMCLK
56	HOLDREQ_N	Input	External Bus hold request, active low
57	HOLDGNT_N	Output	External Bus grant request, active low
58	RESET_N	Input	Reset input
59	RESET_OUT_N	Output	Reset output
60	GND	Ground	Digital ground
61	A0	Output	External Bus Interface address Bit [0]
62	A1	Output	External Bus Interface address Bit [1]
63	A2	Output	External Bus Interface address Bit [2]
64	A3	Output	External Bus Interface address Bit [3]
65	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
66	A4	Output	External Bus Interface address Bit [4]
67	A5	Output	External Bus Interface address Bit [5]
68	A6	Output	External Bus Interface address Bit [6]
69	A7	Output	External Bus Interface address Bit [7]
70	GND	Ground	Digital ground
71	A8	Output	External Bus Interface address Bit [8]
72	A9	Output	External Bus Interface address Bit [9]
73	A10	Output	External Bus Interface address Bit [10]
74	A11	Output	External Bus Interface address Bit [11]

4.2 BGA 10- by 10-mm Package

4.2.1 BGA 10- by 10-mm Pinout

The pinout for the fido1100™ communication controller BGA 10- by 10-mm package is as shown in Figure 4. The corresponding pinout is provided in Table 4.

Table 4. BGA 10- by 10-mm Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
B10	UIC3_6	Bidirectional	Universal I/O Controller 3 pin 6
C9	UIC3_7	Bidirectional	Universal I/O Controller 3 pin 7
A10	UIC3_8	Bidirectional	Universal I/O Controller 3 pin 8
C8	UIC3_9	Bidirectional	Universal I/O Controller 3 pin 9
B9	UIC3_10	Bidirectional	Universal I/O Controller 3 pin 10
A9	UIC3_11	Bidirectional	Universal I/O Controller 3 pin 11
C7	UIC3_12	Bidirectional	Universal I/O Controller 3 pin 12
B8	UIC3_13	Bidirectional	Universal I/O Controller 3 pin 13
A8	GND	Ground	Digital Ground
C6	UIC3_14	Bidirectional	Universal I/O Controller 3 pin 14
B7	UIC3_15	Bidirectional	Universal I/O Controller 3 pin 15
A7	UIC3_16	Bidirectional	Universal I/O Controller 3 pin 16
B6	UIC3_17	Bidirectional	Universal I/O Controller 3 pin 17
A6	T0IC0_T0OC0	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 0 or output compare 0
C5	T0IC1_T0OC1	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 1 or output compare 1
B5	T0IC2_T0OC2	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 2 or output compare 2
A5	T0IC3_T0OC3	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 3 or output compare 3
M8	GND	Ground	Digital ground
C4	T1IC0_T1OC0	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 0 or output compare 0
B4	T1IC1_T1OC1	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 1 or output compare 1
A4	T1IC2_T1OC2	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 2 or output compare 2
B3	T1IC3_T1OC3	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 3 or output compare 3
L7	VDDC	Power	Digital core supply voltage (+2.5VDC)
A3	T0IN	Input	Timer Counter Unit 0 external clock source
A2	T1IN	Input	Timer Counter Unit 1 external clock source
M9	GND	Ground	Digital Ground
J7	VDDC	Power	Digital core supply voltage (+2.5VDC)

4.3 BGA 15- by 15-mm Package

4.3.1 BGA 15- by 15-mm Pinout

The pinout for the fido1100™ communication controller BGA 15- by 15-mm package is as shown in Figure 6. The corresponding pinout is provided in Table 5.

Table 5. BGA 15- by 15-mm Package Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
T8	A11	Output	External Bus Interface address Bit [11]
D9	VDDC	Power	Digital core supply voltage (+2.5VDC)
U8	A12	Output	External Bus Interface address Bit [12]
U9	A13	Output	External Bus Interface address Bit [13]
T9	A14	Output	External Bus Interface address Bit [14]
R9	A15	Output	External Bus Interface address Bit [15]
H4	VDDC	Power	Digital core supply voltage (+2.5VDC)
U10	A16	Output	External Bus Interface address Bit [16]
T10	A17	Output	External Bus Interface address Bit [17]
R10	A18	Output	External Bus Interface address Bit [18]
U11	A19	Output	External Bus Interface address Bit [19]
G14	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
T11	A20	Output	External Bus Interface address Bit [20]
P11	A21	Output	External Bus Interface address Bit [21]
R11	A22	Output	External Bus Interface address Bit [22]
U12	A23	Output	External Bus Interface address Bit [23]
E4	GND	Ground	Digital ground
T12	A24	Output	External Bus Interface address Bit [24]
U13	A_25_RESET_DELAY	Internal Pull-up	Muxed pin, External Bus Interface address Bit [25] or POR counter bypass
P12	A_26_SIZE	Internal Pull-up	Muxed pin, External Bus Interface address Bit [26] or data bus size select (0 = 8-Bit, 1= 16=Bit)
R12	A27_CS7_N	Output	Muxed pin, External Bus Interface address Bit [27] or Chip select 7 (chip select active low)
T13	A28_CS6_N	Output	Muxed pin, External Bus Interface address Bit [28] or Chip select 6 (chip select active low)
R13	A29_CS5_N	Output	Muxed pin, External Bus Interface address Bit [29] or Chip select 5 (chip select active low)
U14	A30_CS4_N	Output	Muxed pin, External Bus Interface address Bit [30] or Chip select 4 (chip select active low)
T14	CS0_N	Output	Chip select 0 (chip select active low)
T15	CS1_N	Output	Chip select 1 (chip select active low)
R15	CS2_N	Output	Chip select 2 (chip select active low)
R14	CS3_N	Output	Chip select 3 (chip select active low)
U15	TDI	Input	JTAG data input
U16	TDO	Output	JTAG data output
T16	TCK	Input	JTAG clock input
U17	TMS	Input	JTAG control signal
K14	VDDC	Power	Digital core supply voltage (+2.5VDC)

4.3.3 BGA 15- by 15-mm Signal Routing

The 15- by15-mm BGA can be easily routed using economical and readily available PCB fabrication design rules. In order to route all signals from the fido1100 BGA, 2 layers in addition to power and ground are required, using 0.1mm trace/space technology. Since 0.1mm = 3.937mil, most PCB fabricators will consider this 4mil trace/space.

The PCB land pattern for the BGA should use 0.3mm round pads. Since the BGA pitch is 0.8mm, this leaves 0.5mm of space between pads. Using 0.1mm trace/space, 2 signals may be routed between each pair of pads (2 traces + 3spaces = 0.5mm). Figure 8 shows how this is accomplished.

Referring to Figure 8, signal layer 1 is shown in black, signal layer 2 is shown in red, and the vias are shown in blue. Signal layer 1 is the top side with the BGA pads, while signal layer 2 may be any other layer, but is typically the bottom side. All vias with no trace routed out from the BGA are power or ground.

Note that the innermost row of pads is all power and ground, except for 9 pads which are signals. Three of these signals are easily routed on signal layer 1, but 6 of them require the use of vias and signal layer 2. If all of the signals are not required for a given design, it may be possible to route all of the used signals on signal layer 1.

It may be beneficial to place more vias and to route more signals on layers other than signal layer 1. This could produce a better PCB layout, but care should be exercised to not include an excessive number of vias. The use of too many vias can lead to inadequate copper on the power/ground plane layers surrounding the center area of the BGA, resulting in relative isolation of the BGA power/ground via connections.

Note the open space between pads M17 and N17 (A1 is upper left corner). These signals are XTAL1 and XTAL0. It is best not to route other signals between these pads, especially if a crystal is used for the clock source.

The power connections to the inner ring of pads have 4 vias for +3.3V and 4 vias for +2.5V. The use of a single bypass capacitor for each via, and alternating 0.1uF and 0.01uF values on each supply, provide reasonable bypass capacitance for the fido1100. Using 8 capacitors in this manner allows the use of capacitors in the 0603 package for economical PCB assembly.

5. Electrical Characteristics

Tables 11, 12, 13, 14, and 15 show the absolute maximum ratings, ESD and latch-up characteristics, recommended operating conditions, DC characteristics, and input impedance, respectively.

Table 11. Absolute Maximum Ratings

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{DDC}	Digital core supply voltage	–	-0.3	–	3.05	V
V_{DDIO}	Digital I/O supply voltage	–	-0.3	–	5.5	V
V_{AIN}	Analog input voltage with respect to ground	–	-0.3	–	3.9	V
T_A	Ambient temperature	–	-40	–	+85	^oC
T_S	Storage temperature	–	-55	–	+150	^oC

Note: Operation of the fido1100 outside of maximum operating ratings may result in failure of the device.

Table 12. ESD and Latch-Up Characteristics

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{HBM}	Human body model	–	2000	–	–	V
V_{MM}	Machine model	–	200	–	–	V
I_{LATP}	Positive latch-up current	–	–	–	50	µA
I_{LATN}	Negative latch-up current	–	–	–	-50	µA

Table 13. Recommended Operating Conditions

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{DDC}	Digital core supply voltage	–	2.25	2.5	2.75	V
V_{DDIO}	Digital I/O supply voltage	–	3.0	3.3	3.6	V
f_{XTAL}	Crystal frequency	–	–	–	66	MHz
T_A	Ambient temperature	–	-40	–	+85	^oC
V_{DDA}	Analog supply voltage	–	3.0	3.3	3.6	V
V_{RH}	ADC reference voltage—high	–	–	3.0	–	V
V_{RL}	ADC reference voltage—low	–	–	0	–	V
C_L	Digital output load capacitance	See note	–	3.1	–	pF

Note: This parameter is guaranteed by design and not tested in production.

The following multiplexed signals are tri-stated during reset and should be pulled high if being used as chip selects or pulled low if being used as address lines (the fido1100 boots at address 0x00000000). If not being used, they can be pulled either high or low.

- A27_CS7_N
- A28_CS6_N
- A29_CS5_N
- A30_CS4_N

At Reset, the CS0_N signal defaults to low for external memory access, supporting the boot sequence from address 0x00000000.

7.3 Clock Signals

7.4 Typical Clock Source Implementations

The fido1100 can operate in one of two modes: (1) Normal or driven clock source input or (2) using an external crystal to set the operating frequency of the internal oscillator.

> *Note: VDDCLK and GNDCLK must be connected even when not using an external crystal.*

7.4.1 Normal or Driven Clock Source

System configuration—Drive external clock source into XTAL0 (see Figure 11). XTAL1 is left unconnected. XTAL0 is effectively a Schmitt trigger input. Target frequency should have a duty cycle of approximately 40% to 60%.

7.4.2 Using an External Crystal

- System Configuration (third overtone)—Crystal across XTAL0/XTAL1 (see Figure 12), 36 pF load caps to ground, 0.1-µF cap, and 0.33-µH inductor in series from XTAL1 to ground.

- System Configuration (fundamental tone)—Crystal across XTAL0/XTAL1 (see Figure 13) and 20-pF load caps to ground.

> *Note: Load capacitor and inductor values may be different based on crystal used. Please consult with your crystal supplier for more information.*

Third overtone configuration is recommended for 24- to 66-MHz operation and fundamental tone configuration is recommended for 1- to 24-MHz operation.

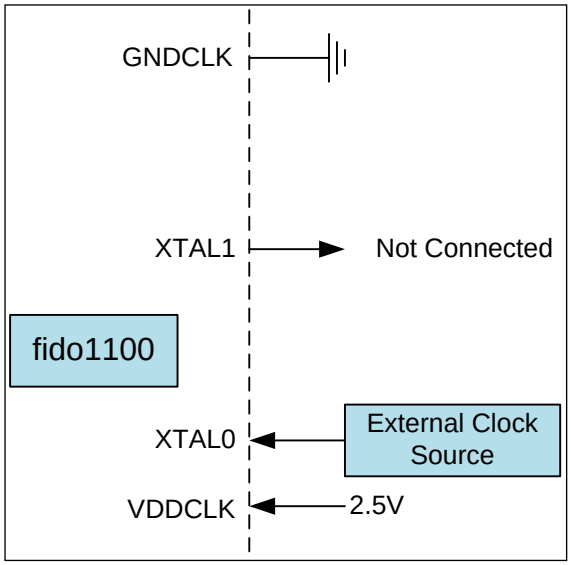

Figure 12. Driven Clock Source

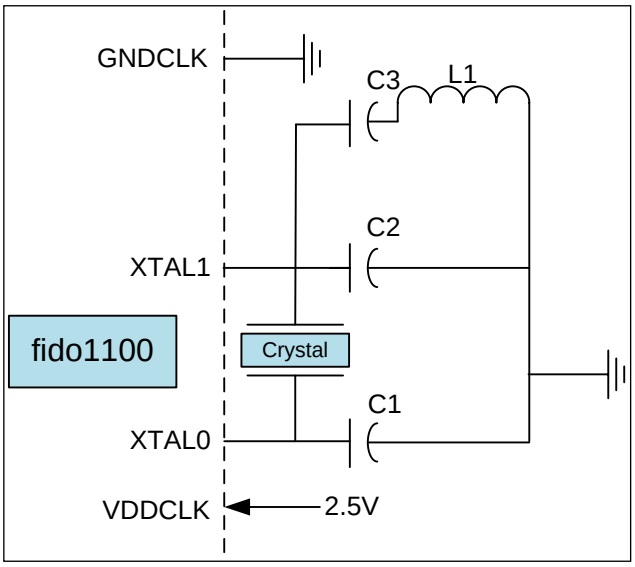

Figure 13. Crystal Oscillator Third Overtone Off-Chip Components

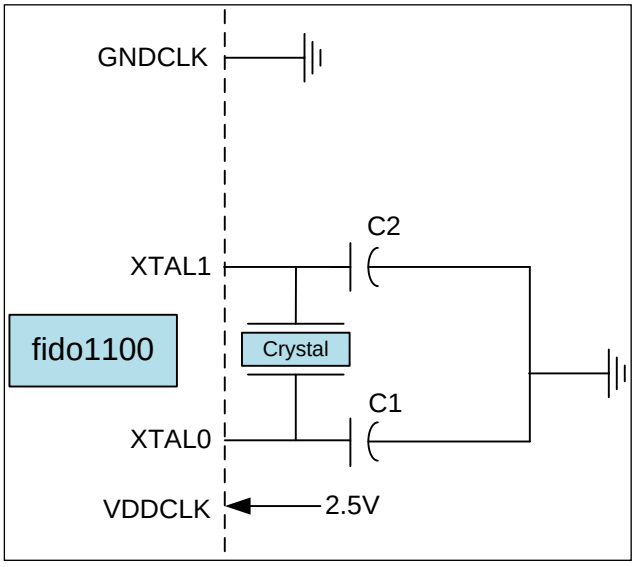

Figure 14. Crystal Oscillator Fundamental Overtone Off-Chip Components

8.3 External Bus Timing

Signals listed on the External Bus Timing diagrams are described below.

- TwWAIT
  - If RDY_ENABLE=0, specifies the width of the chip select active period for the non-burst-mode write cycle. The allowed range is 0–31, resulting in a wait time of 1–32 clocks.
  - If RDY_ENABLE=1, specifies the wait time before the RDY_N line is first sampled for the write cycle. This provides a max wait time of 484 nS at 66 MHz. Anything greater than this will require the external RDY_N line and external logic.

- TrWAIT
  - If RDY_ENABLE=0, specifies the width of the chip select active period for the non-burst-mode read cycle. The allowed range is 0–31, resulting in a wait time of 1–32 clocks.
  - If RDY_ENABLE=1, specifies the wait time before the RDY_N line is first sampled for the read cycle. This provides a max wait time of 484 nS at 66 MHz. Anything greater than this will require the external RDY_N line and external logic.

- The output-enable signal (OE_N) goes active (low) 0–3 clocks (TOE) after the chip select.
- The output-enable signal (OE_N) goes inactive (hi) coincident with the chip select. This is also when the read data is sampled.
- The write-enable signal (WE_N) goes active (low) 0–3 clocks (TWEF) after the chip select.
- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the cycle (CSn_N is removed).

9.1.4 External Bus Timing for 8-Bit/16-Bit Transfer (with RDY_N)

This timing is programmable via the External Bus Chip Select Control Register (see Figure 23).

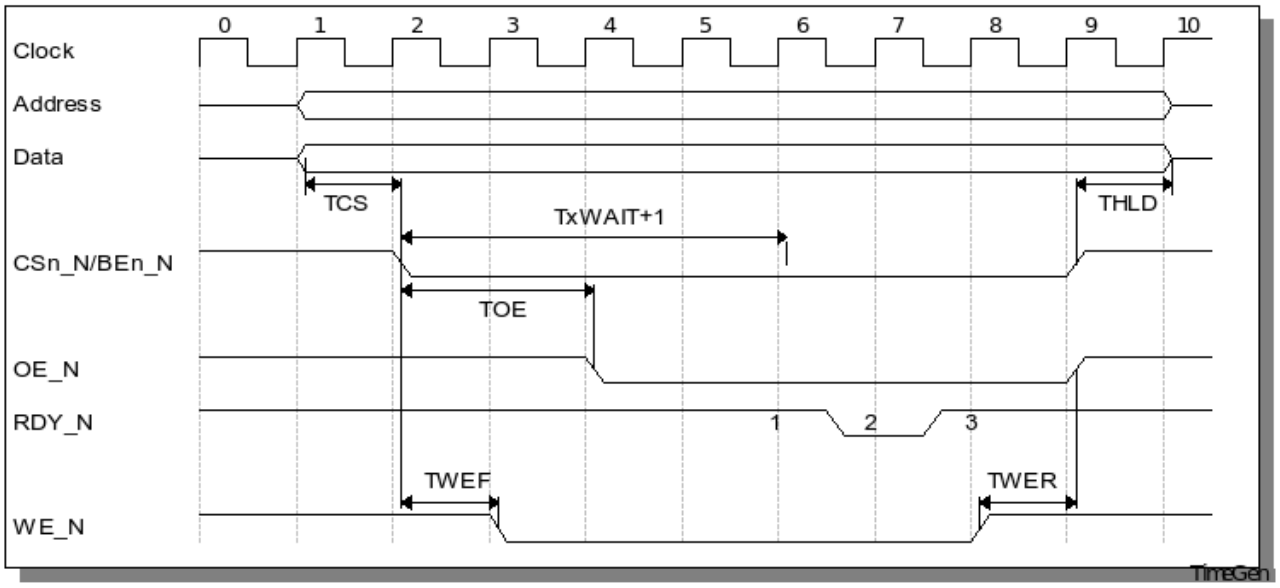

Figure 24. External Bus Timing for 8-Bit/16-Bit Transfer (with RDY_N)

- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The TxWAIT setting determines when first to start sampling the low active RDY_N line (labeled with an arrow marked “1” in the diagram).

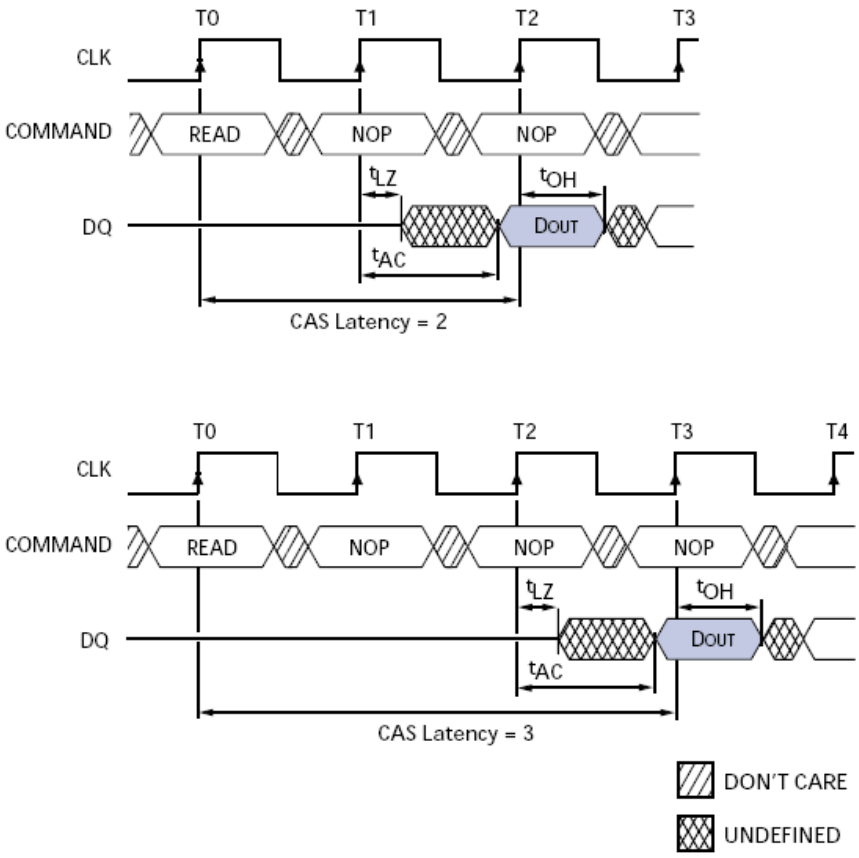

Figure 25. SDRAM CAS Timing

9.2.2 SDRAM Row Activation Timing

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 25). After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification. The tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 20ns with a 125-MHz clock (8-ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 26, which covers any case where $2 < \text{tRCD (MIN)/tCK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

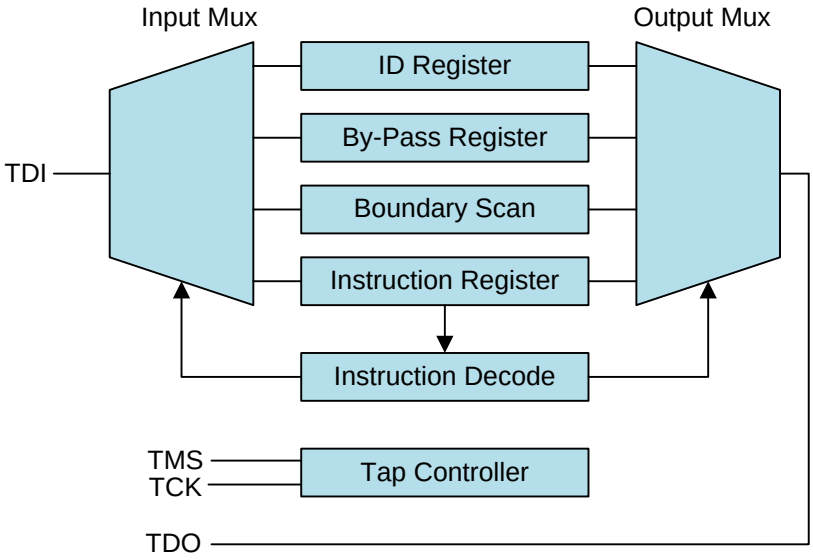

Figure 35. JTAG Port Register Interface

The timing of the JTAG signals is shown in Figure 35. The TDO pin remains in the high impedance state except during a shift-DR or shift-IR controller state. In the shift-DR and shift-IR controller states, TDO is updated on the falling edge of TCK. TMS and TDI are sampled on the rising edge of TCK.

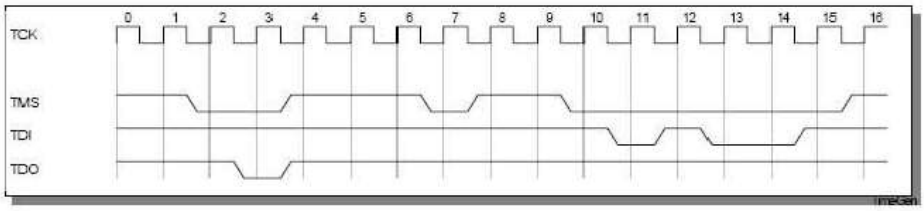

Figure 36. Timing of JTAG Signals

10.1 JTAG Scan Chain Debug Functionality

The JTAG port contains an 8-bit-wide instruction register. Instructions are transferred to this register during the shift-IR state of the TAP state machine and are decoded by entering the Update-IR state of the TAP. The JTAG controller executes the last decoded instruction until another new one is entered and decoded. The instructions and data are entered serially through the TDI pin, LSB first.

The JTAG Test Access Port (TAP) instruction shift register will support the debug scan chain commands shown in Table 23.

Table 23. Debug Scan Chain Commands Supported by the JTAG TAP

JTAG Instruction	Scan Chain Function	Scan Chain Length	Scan Chain Reference Number	Public or Private
00010000	READWRITEADDRCMD (Read/Write Memory/Registers Address and Command)	37 bits	1	Private
00010001	READDATA (Read Memory/Registers Data)	32 bits	2	Private
00010010	WRITEDATA (Write Memory/Registers Data)	32 bits	7	Private
00010011	READPC_ANDCONTEXT (Read Program Counter and Active context)	37 bits	4	Private
00010100	READWRITEDRBUGREG (Read/Write Debug Control Register)	15 bits	5	Private
11111110	IDCODE (Read Device ID Register)	32 bits	3	Public
11111000	EXTEST (IO Boundary Scan)	n bits (I/O Pins)	6	Public
11111010	SAMPLE/PRELOAD (Sample Boundary Scan chain on “Capture-DR” state, Load Boundary Scan chain on ‘Update-DR’ state)	N bits (I/O Pins)	6	Public
11111111	BYPASS (Use TDI/TDO Bypass Register)	1 bit	9	Public
00000111	RUNBIST (Run Built in Self Test)	16 bits	8	Public
00001111	ENABLEATPG (Enable ATPG Mode for Manufacturing Test)	N/A	N/A	Private

Notes:

1. The boundary-scan scan chain is selected via the EXETEST, SAMPLE, and PRELOAD instructions.
2. The SAMPLE and PRELOAD instructions have the SAME binary code. (They are identified as separate instructions in the JTAG Spec, but are allowed to have the same binary code for backwards compatibility with previous version of spec.)
3. Any undefined bit pattern that is shifted into the Instruction Register will perform the same function as the BYPASS instruction.
4. On Power-on Reset, or when the JTAG state machine enters the “Test Logic Reset” the instruction register will reset its value to operate as the IDCODE Instruction (per JTAG Spec).