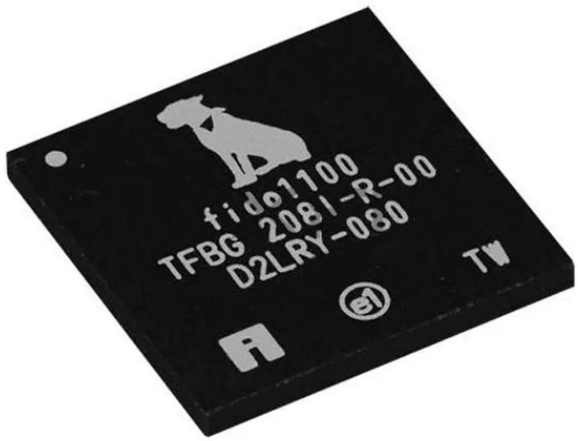

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CPU32
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, EIA-232, Ethernet, GPIO, HDLC, I²C, SMBus, SPI
Peripherals	DMA, POR, WDT
Number of I/O	72
Program Memory Size	32KB (32K x 8)
Program Memory Type	RREM
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/fido1100bgb208ir1

LIST OF TABLES

1. Overview

Innovasic Semiconductor's fido1100 is the first product in the fido™ family of real-time communication controllers. The fido communication controller architecture is uniquely optimized for solving memory bottlenecks, and is designed from the ground up for deterministic processing. Critical timing parameters, such as context switching and interrupt latency, are precisely predictable for real-time tasks. The fido1100 also incorporates the Universal I/O Controller (UIC™) that is configurable to support various communication protocols across multiple platforms. This flexibility relieves the designer of the task of searching product matrices to find the set of peripherals that most closely match the system interface needs. The Software Profiling and Integrated Debug EnviRonment (SPIDER™) has extensive real-time code debug capabilities without the burden of code instrumentation (see Table 1).

Figure 1 illustrates the top-level blocks of the fido1100 architecture.

Table 1. Key Features

Feature	Benefit
Programmable UIC	Provides the ability to customize peripherals to match user application. Single chip can solve multiple end-product demands. Reduces costs through optimized inventory management.
Five Hardware Contexts	Runs tight-control loops in separate contexts while RTOS manages high-level tasks in another context. Provides context isolation with robust time-and-space partitioning.
Low-Jitter Execution	Performs tasks at much lower clock rates (66MHz versus >200MHz), reducing power budget and simplifying board design.
SPIDER	Reduces system integration and debug time through in-system, "what-if" testing without code changes. Reduces firmware development time thus cutting costs. Up to 1Mbyte of trace buffer.
Long-Life-Cycle Support	Fulfills Innovasic's corporate policy of supporting products for the customer's entire life-cycle, eliminating product obsolescence concerns.

- JTAG emulation and debug interface
- Available in a 208-pin PQFP, BGA 10- by 10-mm package, and BGA 15- by 15-mm package
- 3.3V operation with 5V-tolerant I/O
- Industrial temperature grade
- Software development supported by libraries and tools including UIC firmware for various interface protocols and formats, as well as a customized GNU tool set.

2.1 Core CPU

The fido1100 core is based on the CPU32 architecture, and is compatible with the CPU32 instruction set. The fido1100 incorporates five independent hardware contexts. While all contexts share the same Execution Unit, each of the five hardware contexts in the fido1100 has its own register set, execution priority and exception vector table. From an application's view, this unique feature of the fido1100 allows it to operate as five independent machines in one:

- 32-bit address and data paths on-chip
- 66-MHz operation
- Instruction execution from external memory or fast internal memory.
- Each hardware context has its own copy of:
  - Eight 32-bit User Data Registers (D0-D7)
  - Seven 32-bit Address Registers (A0-A6)
  - Two 32-bit Stack Pointers (A7 and A7')
  - One 32-bit Program Counter
  - One 16-bit Status Register (SR)
  - One 32-bit Vector Base Register (VBR)

2.2 JTAG

The fido1100 is fully compliant with the IEEE 1149.1 Test Access Port and Boundary-Scan architecture (see Table 2). The fido1100 architecture is equipped with the TAP (Test Access Port) interface, TAP controller, instruction register, instruction decoder, boundary-scan register, and by-pass register.

The UIC is a very flexible hardware solution designed to support numerous interface requirements. When working in concert with the on-board Peripheral Management Unit (PMU) and on-board data buffers, the operation of the interfaces requires little core processor intervention. This allows the processor to use its bus bandwidth for more important functions than managing data traffic. The UIC design can support complex protocols such as Ethernet or GPIO functions.

- Four software-configurable UICs
- Each supports 10/100 Ethernet, CAN, UART, SPI, I^2C, HDLC, or GPIO functionality
- Software libraries are provided for various interface protocols and formats
- User-programmable integrated 256-location MAC address filter
- Dedicated PMU offloads main CPU bus traffic
- Large 1K × 32 transmit buffer and 2K × 32 receive buffers
- At a minimum, each UIC can support 1 Ethernet port (MII), 2 UARTs, or 18 GPIO
- CPU DMA—Two independent channels of DMA for data transfer

2.6 Internal Peripherals

The fido1100 incorporates the following set of internal peripherals:

2.6.1 Timer Counter Units (TCU)

- Two Timer Counter Units (TCU)—The fido1100 is equipped with two Timer Counter Units.
  - Four channels per timer; any channel can be either input capture or output compare.
  - Input captures can be either rising or falling edge.
  - External signal clocking can be rising edge, falling edge, or both edges of input signal.
  - Output compare can be assert high, assert low, or toggle mode.
  - Underflow, overflow, input-capture, or output-compare conditions can trigger an interrupt.
  - Timers can be programmed for auto-stop or auto-reload.
  - Timer can generate an internal interrupt to wake up the processor from sleep mode.
  - Timer periods in excess of 50 seconds are achievable.

3. Libraries and Support Tools

- Full library support
- UIC libraries
- Embedded communication stacks
- TCP/IP
- GPIO sample programs
- Customized GNU tool set
- Eclipse IDE
- Sourcery G++ from Code Sourcery

Table 3. PQFP Pin Listing

Pin	Signal Name	Type	Description
1	AN_7	Input	Analog-to-digital converter input channel 7
2	AN_6	Input	Analog-to-digital converter input channel 6
3	AN_5	Input	Analog-to-digital converter input channel 5
4	AN_4	Input	Analog-to-digital converter input channel 4
5	AN_3	Input	Analog-to-digital converter input channel 3
6	AN_2	Input	Analog-to-digital converter input channel 2
7	AN_1	Input	Analog-to-digital converter input channel 1
8	AN_0	Input	Analog-to-digital converter input channel 0
9	VRL	Input	Analog-to-digital converter low-input reference
10	VRH	Input	Analog-to-digital converter high-input reference
11	VDDA	Power	Analog supply voltage (+3.3VDC)
12	GNDA	Ground	Analog ground
13	INT0	Input	Interrupt_0
14	INT1	Input	Interrupt_1
15	INT2	Input	Interrupt_2
16	VDDC	Power	Digital core supply voltage (+2.5VDC)
17	INT3	Input	Interrupt_3
18	INT4_DMA0_ ACK	Bidirectional	Muxed pin, Interrupt_4 or DMA channel 0 acknowledge
19	INT5_DMA1_ ACK	Bidirectional	Muxed pin, Interrupt_5 or DMA channel 1 acknowledge
20	INT6_DMA0_ REQ	Input	Muxed pin, Interrupt_6 or DMA channel 0 request
21	INT7_DMA1_ REQ	Input	Muxed pin, Interrupt_7 or DMA channel 1 request
22	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
23	D0	Bidirectional	External Bus Interface data Bit [0]
24	D1	Bidirectional	External Bus Interface data Bit [1]
25	D2	Bidirectional	External Bus Interface data Bit [2]
26	D3	Bidirectional	External Bus Interface data Bit [3]
27	D4	Bidirectional	External Bus Interface data Bit [4]
28	D5	Bidirectional	External Bus Interface data Bit [5]
29	D6	Bidirectional	External Bus Interface data Bit [6]
30	D7	Bidirectional	External Bus Interface data Bit [7]
31	GND	Ground	Digital ground
32	D8	Bidirectional	External Bus Interface data Bit [8]
33	D9	Bidirectional	External Bus Interface data Bit [9]
34	D10	Bidirectional	External Bus Interface data Bit [10]
35	D11	Bidirectional	External Bus Interface data Bit [11]

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
75	VDDC	Power	Digital core supply voltage (+2.5VDC)
76	A12	Output	External Bus Interface address Bit [12]
77	A13	Output	External Bus Interface address Bit [13]
78	A14	Output	External Bus Interface address Bit [14]
79	A15	Output	External Bus Interface address Bit [15]
80	VDDC	Power	Digital core supply voltage (+2.5VDC)
81	A16	Output	External Bus Interface address Bit [16]
82	A17	Output	External Bus Interface address Bit [17]
83	A18	Output	External Bus Interface address Bit [18]
84	A19	Output	External Bus Interface address Bit [19]
85	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
86	A20	Output	External Bus Interface address Bit [20]
87	A21	Output	External Bus Interface address Bit [21]
88	A22	Output	External Bus Interface address Bit [22]
89	A23	Output	External Bus Interface address Bit [23]
90	GND	Ground	Digital ground
91	A24	Output	External Bus Interface address Bit [24]
92	A25_RESET_DELAY	Internal Pull-up	Muxed pin, External Bus Interface address Bit [25] or POR counter bypass
93	A26_SIZE	Internal Pull-up	Muxed pin, External Bus Interface address Bit [26] or data bus size select (0 = 8-Bit, 1= 16=Bit)
94	A27_CS7_N	Output	Muxed pin, External Bus Interface address Bit [27] or Chip select 7 (chip select active low)
95	A28_CS6_N	Output	Muxed pin, External Bus Interface address Bit [28] or Chip select 6 (chip select active low)
96	A29_CS5_N	Output	Muxed pin, External Bus Interface address Bit [29] or Chip select 5 (chip select active low)
97	A30_CS4_N	Output	Muxed pin, External Bus Interface address Bit [30] or Chip select 4 (chip select active low)
98	CS0_N	Output	Chip select 0 (chip select active low)
99	CS1_N	Output	Chip select 1 (chip select active low)
100	CS2_N	Output	Chip select 2 (chip select active low)
101	CS3_N	Output	Chip select 3 (chip select active low)
102	TDI	Input	JTAG data input
103	TDO	Output	JTAG data output
104	TCK	Input	JTAG clock input
105	TMS	Input	JTAG control signal
106	VDDC	Power	Digital core supply voltage (+2.5VDC)
107	UIC0_0	Bidirectional	Universal I/O Controller 0, pin 0
108	UIC0_1	Bidirectional	Universal I/O Controller 0, pin 1

Table 4. BGA 10- by 10-mm Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
B10	UIC3_6	Bidirectional	Universal I/O Controller 3 pin 6
C9	UIC3_7	Bidirectional	Universal I/O Controller 3 pin 7
A10	UIC3_8	Bidirectional	Universal I/O Controller 3 pin 8
C8	UIC3_9	Bidirectional	Universal I/O Controller 3 pin 9
B9	UIC3_10	Bidirectional	Universal I/O Controller 3 pin 10
A9	UIC3_11	Bidirectional	Universal I/O Controller 3 pin 11
C7	UIC3_12	Bidirectional	Universal I/O Controller 3 pin 12
B8	UIC3_13	Bidirectional	Universal I/O Controller 3 pin 13
A8	GND	Ground	Digital Ground
C6	UIC3_14	Bidirectional	Universal I/O Controller 3 pin 14
B7	UIC3_15	Bidirectional	Universal I/O Controller 3 pin 15
A7	UIC3_16	Bidirectional	Universal I/O Controller 3 pin 16
B6	UIC3_17	Bidirectional	Universal I/O Controller 3 pin 17
A6	T0IC0_T0OC0	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 0 or output compare 0
C5	T0IC1_T0OC1	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 1 or output compare 1
B5	T0IC2_T0OC2	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 2 or output compare 2
A5	T0IC3_T0OC3	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 3 or output compare 3
M8	GND	Ground	Digital ground
C4	T1IC0_T1OC0	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 0 or output compare 0
B4	T1IC1_T1OC1	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 1 or output compare 1
A4	T1IC2_T1OC2	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 2 or output compare 2
B3	T1IC3_T1OC3	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 3 or output compare 3
L7	VDDC	Power	Digital core supply voltage (+2.5VDC)
A3	T0IN	Input	Timer Counter Unit 0 external clock source
A2	T1IN	Input	Timer Counter Unit 1 external clock source
M9	GND	Ground	Digital Ground
J7	VDDC	Power	Digital core supply voltage (+2.5VDC)

Table 5. BGA 15- by 15-mm Package Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
P15	UIC0_0	Bidirectional	Universal I/O Controller 0, pin 0
T17	UIC0_1	Bidirectional	Universal I/O Controller 0, pin 1
R16	UIC0_2	Bidirectional	Universal I/O Controller 0, pin 2
R17	UIC0_3	Bidirectional	Universal I/O Controller 0, pin 3
E14	GND	Ground	Digital ground
P16	UIC0_4	Bidirectional	Universal I/O Controller 0, pin 4
N15	UIC0_5	Bidirectional	Universal I/O Controller 0, pin 5
P17	UIC0_6	Bidirectional	Universal I/O Controller 0, pin 6
N16	UIC0_7	Bidirectional	Universal I/O Controller 0, pin 7
M16	UIC0_8	Bidirectional	Universal I/O Controller 0, pin 8
M15	VDDCLK	Power supply	Power Supply for the Crystal Oscillator (+2.5VDC)
N17	XTAL0	Clock	Crystal input pin 0 (Osc. In)
M17	XTAL1	Clock	Crystal input/output pin 1 (Osc. Out)
M14	GNDCLK	Ground	Digital ground
L16	UIC0_9	Bidirectional	Universal I/O Controller 0, pin 9
L15	UIC0_10	Bidirectional	Universal I/O Controller 0, pin 10
L17	UIC0_11	Bidirectional	Universal I/O Controller 0, pin 11
K17	UIC0_12	Bidirectional	Universal I/O Controller 0, pin 12
K16	UIC0_13	Bidirectional	Universal I/O Controller 0, pin 13
K15	UIC0_14	Bidirectional	Universal I/O Controller 0, pin 14
J17	UIC0_15	Bidirectional	Universal I/O Controller 0, pin 15
J16	UIC0_16	Bidirectional	Universal I/O Controller 0, pin 16
J15	UIC0_17	Bidirectional	Universal I/O Controller 0, pin 17
N4	GND	Ground	Digital ground
H17	UIC1_0	Bidirectional	Universal I/O Controller 1, pin 0
H16	UIC1_1	Bidirectional	Universal I/O Controller 1, pin 1
G17	UIC1_2	Bidirectional	Universal I/O Controller 1, pin 2
H15	UIC1_3	Bidirectional	Universal I/O Controller 1, pin 3
J4	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
G16	UIC1_4	Bidirectional	Universal I/O Controller 1, pin 4
F17	UIC1_5	Bidirectional	Universal I/O Controller 1, pin 5
E17	UIC1_6	Bidirectional	Universal I/O Controller 1, pin 6
G15	UIC1_7	Bidirectional	Universal I/O Controller 1, pin 7
F16	UIC1_8	Bidirectional	Universal I/O Controller 1, pin 8
D17	UIC1_9	Bidirectional	Universal I/O Controller 1, pin 9
L14	VDDC	Power	Digital core supply voltage (+2.5VDC)
E16	UIC1_10	Bidirectional	Universal I/O Controller 1, pin 10
F15	UIC1_11	Bidirectional	Universal I/O Controller 1, pin 11

The following multiplexed signals are tri-stated during reset and should be pulled high if being used as chip selects or pulled low if being used as address lines (the fido1100 boots at address 0x00000000). If not being used, they can be pulled either high or low.

- A27_CS7_N
- A28_CS6_N
- A29_CS5_N
- A30_CS4_N

At Reset, the CS0_N signal defaults to low for external memory access, supporting the boot sequence from address 0x00000000.

7.3 Clock Signals

7.4 Typical Clock Source Implementations

The fido1100 can operate in one of two modes: (1) Normal or driven clock source input or (2) using an external crystal to set the operating frequency of the internal oscillator.

> *Note: VDDCLK and GNDCLK must be connected even when not using an external crystal.*

7.4.1 Normal or Driven Clock Source

System configuration—Drive external clock source into XTAL0 (see Figure 11). XTAL1 is left unconnected. XTAL0 is effectively a Schmitt trigger input. Target frequency should have a duty cycle of approximately 40% to 60%.

7.4.2 Using an External Crystal

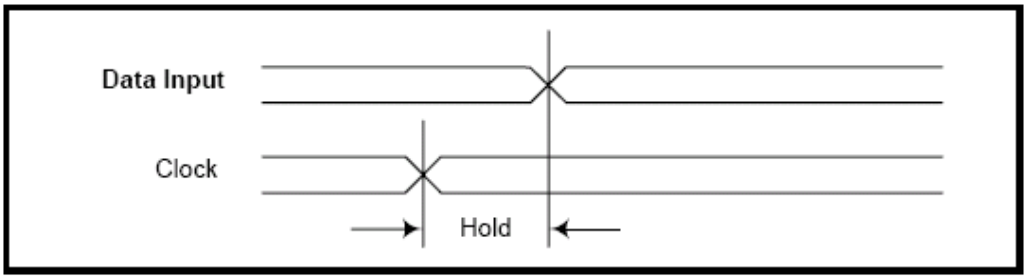
- System Configuration (third overtone)—Crystal across XTAL0/XTAL1 (see Figure 12), 36 pF load caps to ground, 0.1-µF cap, and 0.33-µH inductor in series from XTAL1 to ground.

- System Configuration (fundamental tone)—Crystal across XTAL0/XTAL1 (see Figure 13) and 20-pF load caps to ground.

> *Note: Load capacitor and inductor values may be different based on crystal used. Please consult with your crystal supplier for more information.*

Third overtone configuration is recommended for 24- to 66-MHz operation and fundamental tone configuration is recommended for 1- to 24-MHz operation.

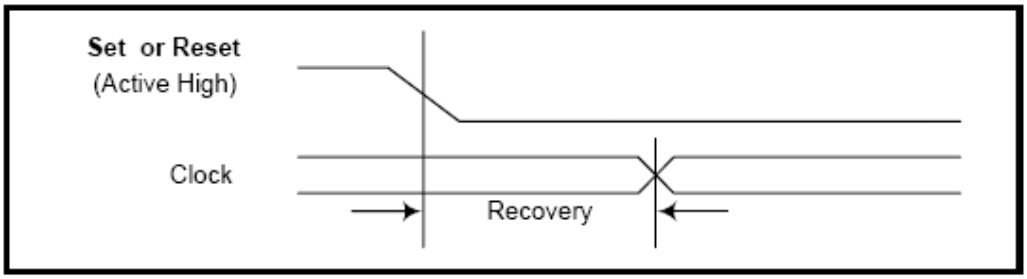
- Hold Time—The minimum time that input data must remain unchanged subsequent to an active clock transition (see Figure 16).



Hold = 2ns.

Figure 17. Hold Time

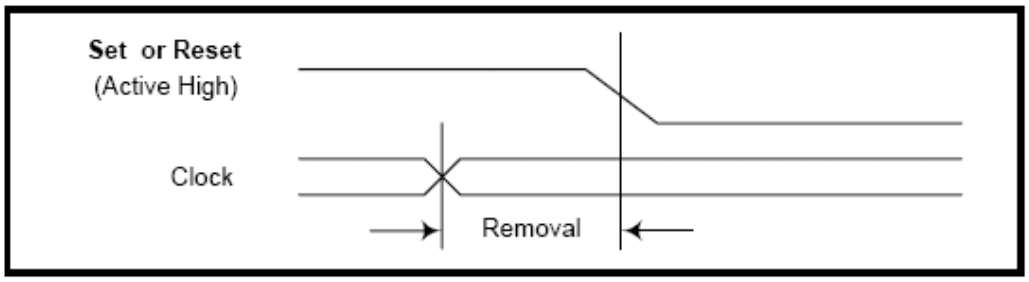
- Recovery Time—The minimum time that the Set or Reset input must remain unactivated prior to an active clock transition (see Figure 17).



Recovery = 3ns.

Figure 18. Recovery Time

- Removal Time—The minimum time that the Set or Reset input must remain activated subsequent to an active clock transition (see Figure 18).



Removal = 3ns.

Figure 19. Removal Time

- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the chip-select time.

9.1.3 External Bus Timing for 8-Bit/16-Bit Transfer (without RDY_N)

This timing is programmable via the External Bus Chip Select Control Register (see Figure 22).

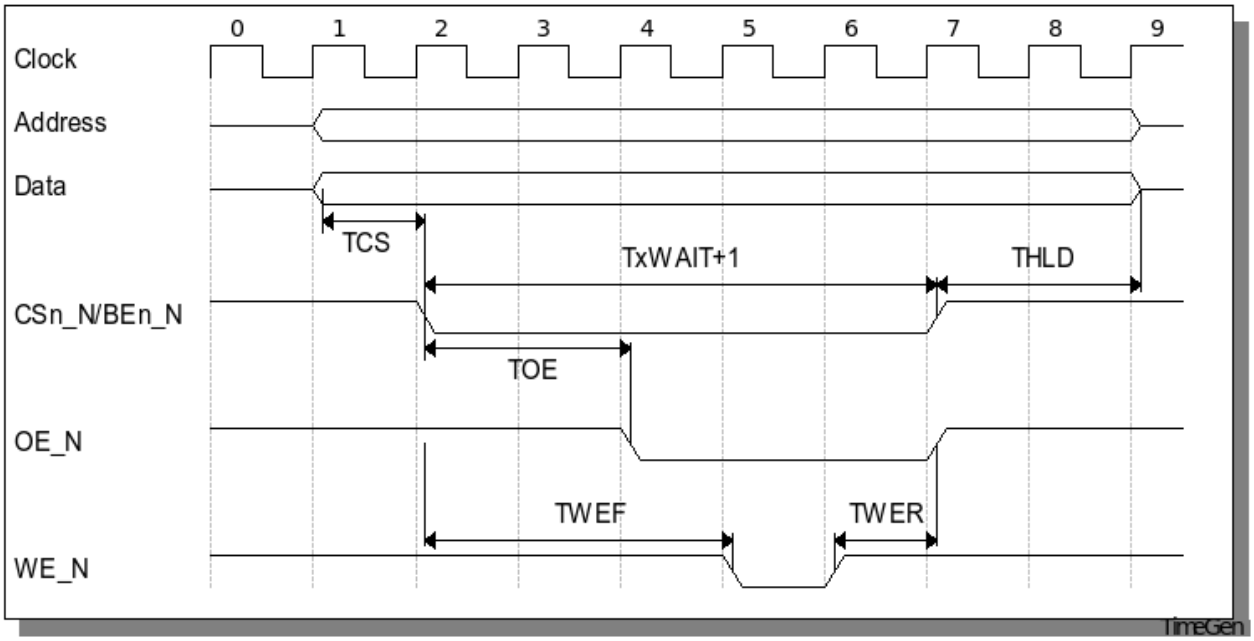


Figure 23. External Bus Timing for 8-Bit/16-Bit Transfer (without RDY_N)

- All timing is relative to the rising edge of the clock.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go active (low) 0–3 clocks (TCS) after the address bus is driven.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go inactive (hi) 0–7 clocks (THLD) before the address is changed.
- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.

- The output-enable signal (OE_N) goes active (low) 0–3 clocks (TOE) after the chip select.
- The output-enable signal (OE_N) goes inactive (hi) coincident with the chip select. This is also when the read data is sampled.
- The write-enable signal (WE_N) goes active (low) 0–3 clocks (TWEF) after the chip select.
- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the cycle (CSn_N is removed).

9.1.4 External Bus Timing for 8-Bit/16-Bit Transfer (with RDY_N)

This timing is programmable via the External Bus Chip Select Control Register (see Figure 23).

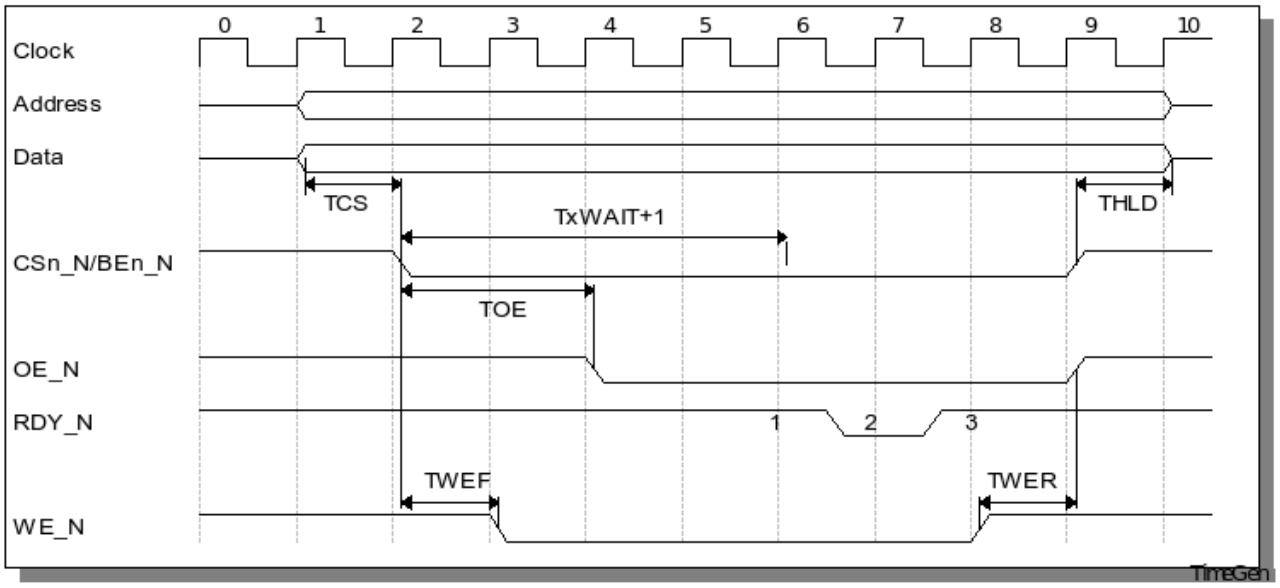


Figure 24. External Bus Timing for 8-Bit/16-Bit Transfer (with RDY_N)

- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The TxWAIT setting determines when first to start sampling the low active RDY_N line (labeled with an arrow marked “1” in the diagram).

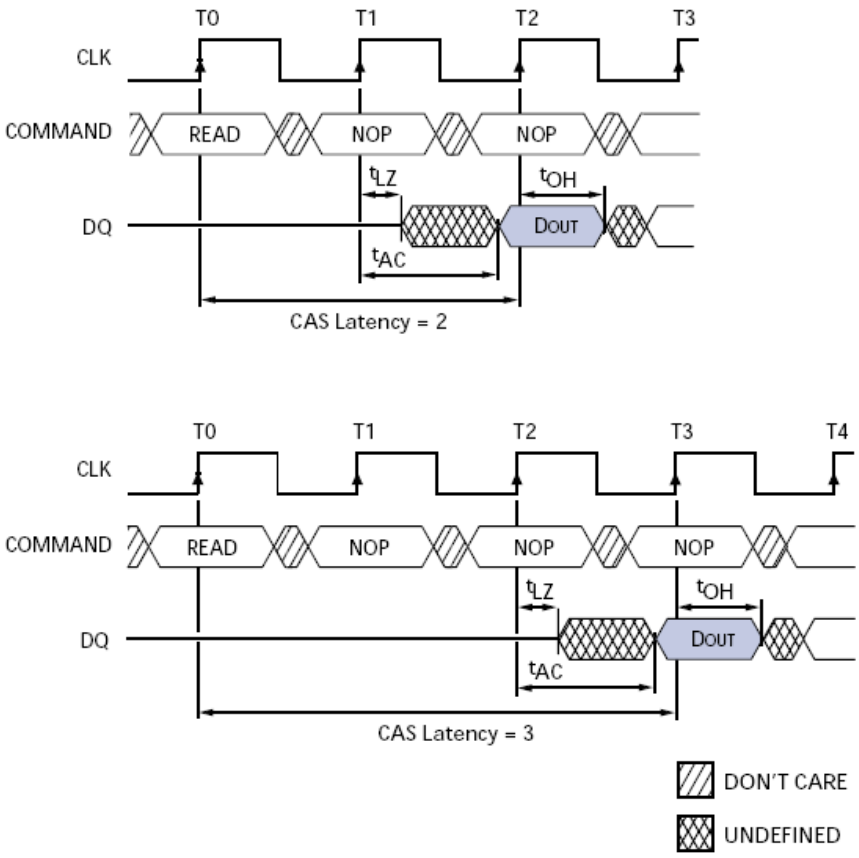


Figure 25. SDRAM CAS Timing

9.2.2 SDRAM Row Activation Timing

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 25). After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the tRCD specification. The tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 20ns with a 125-MHz clock (8-ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 26, which covers any case where $2 < \text{tRCD (MIN)/tCK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

9.2.3 SDRAM Read Operation Timing

READ bursts are initiated with a READ command.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled (see Figure 27).

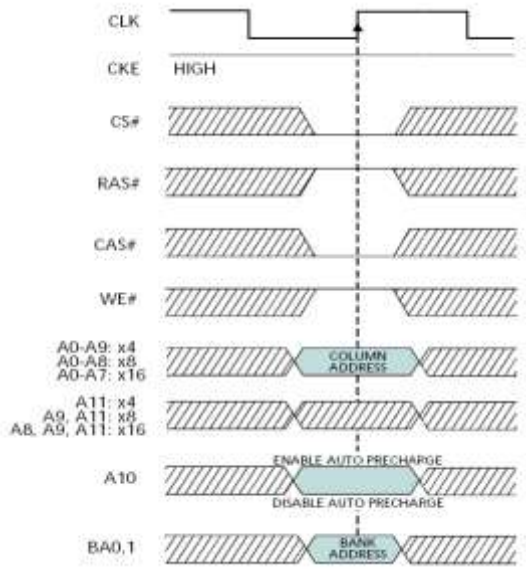


Figure 28. SDRAM Read Operation Timing

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go high, and full-page burst will continue until terminated. (At end of the page, it will wrap to column 0 and continue.)

9.2.4 SDRAM Read Burst Timing

Data from any READ burst may be truncated with subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a

10. JTAG

The TAP controller is a synchronous Finite State Machine and responds to changes in the TMS and TCK signals. States transition occurs on the rising edge of TCK. Values shown to the side of each state represent the state of TMS at the time of the rising edge of TCK (see Figure 33).

There are two paths through the state machine. The instruction path captures and loads the JTAG instructions into the instruction register. The data path captures and loads data into the other three registers. The TAP controller executes the last instruction decode until a new instruction is entered at the Update-IR state or until a reset is sent to the controller.

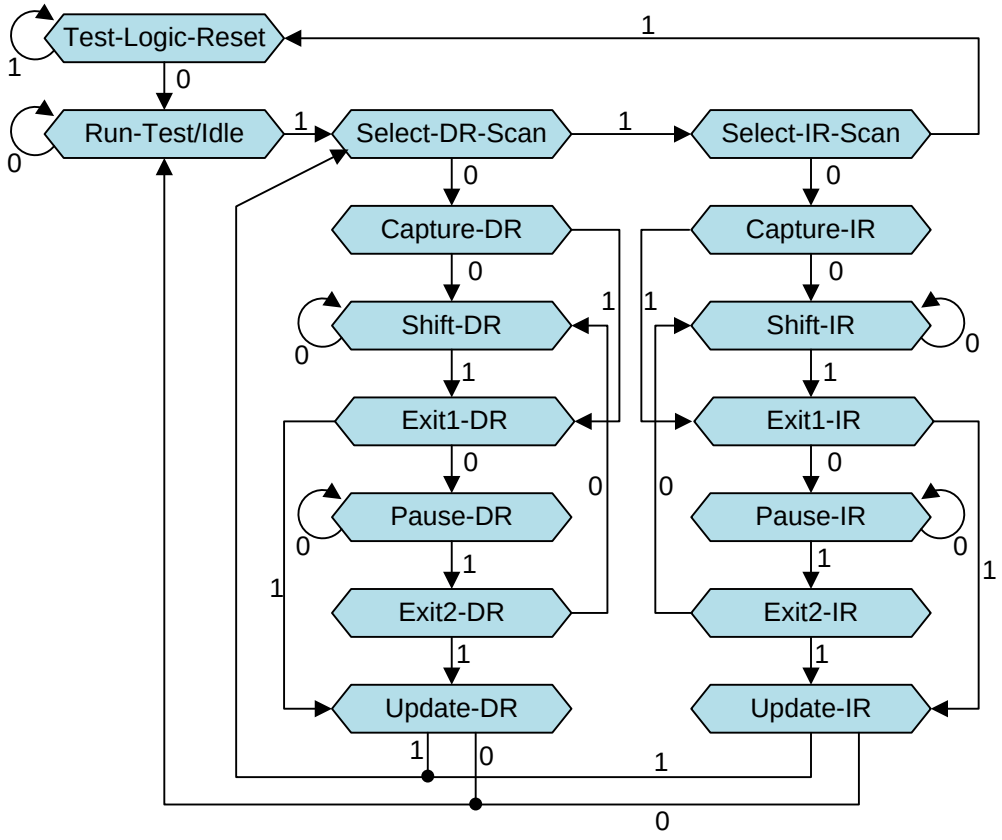


Figure 34. JTAG State Machine

The JTAG port has four Read/Write registers. An ID register, By-Pass Register, Boundary Scan, and Instruction Register (see Figure 34).

The TDO pin remains in the high impedance state except during a shift-DR or shift-IR controller state. In the shift-DR and shift-IR controller states, TDO is updated on the falling edge of TCK. TMS and TDI are sampled on the rising edge of TCK.

Table 23. Debug Scan Chain Commands Supported by the JTAG TAP

JTAG Instruction	Scan Chain Function	Scan Chain Length	Scan Chain Reference Number	Public or Private
00010000	READWRITEADDRCMD (Read/Write Memory/Registers Address and Command)	37 bits	1	Private
00010001	READDATA (Read Memory/Registers Data)	32 bits	2	Private
00010010	WRITEDATA (Write Memory/Registers Data)	32 bits	7	Private
00010011	READPC_ANDCONTEXT (Read Program Counter and Active context)	37 bits	4	Private
00010100	READWRITEDRBUGREG (Read/Write Debug Control Register)	15 bits	5	Private
11111110	IDCODE (Read Device ID Register)	32 bits	3	Public
11111000	EXTEST (IO Boundary Scan)	n bits (I/O Pins)	6	Public
11111010	SAMPLE/PRELOAD (Sample Boundary Scan chain on “Capture-DR” state, Load Boundary Scan chain on ‘Update-DR’ state)	N bits (I/O Pins)	6	Public
11111111	BYPASS (Use TDI/TDO Bypass Register)	1 bit	9	Public
00000111	RUNBIST (Run Built in Self Test)	16 bits	8	Public
00001111	ENABLEATPG (Enable ATPG Mode for Manufacturing Test)	N/A	N/A	Private

Notes:

1. The boundary-scan scan chain is selected via the EXETEST, SAMPLE, and PRELOAD instructions.
2. The SAMPLE and PRELOAD instructions have the SAME binary code. (They are identified as separate instructions in the JTAG Spec, but are allowed to have the same binary code for backwards compatibility with previous version of spec.)
3. Any undefined bit pattern that is shifted into the Instruction Register will perform the same function as the BYPASS instruction.
4. On Power-on Reset, or when the JTAG state machine enters the “Test Logic Reset” the instruction register will reset its value to operate as the IDCODE Instruction (per JTAG Spec).

12. Errata

This chapter addresses issues discovered by our internal testing organization that may affect the implementation of the fido1100. This information should be used in conjunction with *The fido1100 User Guide* and *The fido1100 Instruction Set Reference Guide* to circumvent problems during the design process and is not intended as a standalone design guide. Although fido1100-specific terms are clearly described, in the interest of conciseness, many terms already familiar to designers and developers are left undefined.

12.1 Summary

Table 25 presents a summary of errata.

Table 25. Summary of Errata

Errata No.	Problem	Ver. 1
1	ADC Start Register Bit 0 (START) does not self clear when non-scanning mode conversion for single channel or multi-channel is selected.	Exists
2	Fatal fault recovery sequence can be disturbed by interrupts.	Exists
3	The vectors are reversed when a trapx instruction is executed coincident with an interrupt to a higher priority context.	Exists
4	When using the RDY_N signal to insert wait states (chip select timing register RDY_ENABLE bit = 1), the Address bus timing is incorrect.	Exists
5	When using a JMP or JSR instruction in PC indirect with base displacement addressing mode in assembly code projects, the CPU does not execute the instruction correctly.	Exists

12.2 Detail

Errata No. 1

Problem: ADC Start Register Bit 0 (START) does not self clear when non-scanning mode conversion for single channel or multi-channel is selected.

Description:

- Scanning mode is controlled by ADC Control Register Bit 6 (SCAN).

- ADC Control Register Bit 4 (CD-Conversion Done) will correctly indicate that conversion(s) are done.
- An ADC interrupt will be issued if ADC interrupts are enabled. ADC interrupts are enabled by setting ADC Control Register Bit 3 (IRQ_En) to 1.
- ADC Data Available Register will correctly indicate which channels have updated results in their Data Registers.

Workaround: When using non-scanning mode conversions, enable the ADC between each commanded conversion (single channel or multi-channel):

- Clear ADC Control Register Bit 7 (EN) to 0.
- Set ADC Control Register Bit 7 (EN) to 1.
- Set ADC Start Register Bit 0 (START) to 1 to start the conversion process.
- ADC Conversion complete will be indicated by:
  - An ADC interrupt, if ADC Control Register Bit 3 (IRQ_En) is set to 1.
  - ADC Control Register Bit 4 (CD-Conversion Done) will set to indicate that conversion(s) are done.

Errata No. 2

Problem: Fatal fault recovery sequence can be disturbed by interrupts.

Description:

Context Fatal Faults can occur if a context's stack pointer becomes corrupted. It is a feature of the hardware to detect this "Fatal Fault" and allow a graceful recovery by directing an exception to the Master Context. This operation can be disturbed if, by chance, an interrupt is triggered during a bus cycle leading to a Fatal Fault. This problem occurs no matter which context the interrupt is directed to. It need not be the faulting context. Furthermore, since neither interrupt timing nor fatal faults are predictable, there is no way to guarantee this cannot happen. The effect of this error depends on the interrupt mode of the context to which the interrupt is directed. If the interrupted context is running in Fast Single Threaded mode, when an interrupt targeted to it occurs during a faulting bus cycle (caused by another context) the CPU will lock up after the faulting bus cycle completes. If the interrupted context is in Standard or Fast Vectored mode the CPU will not lock up but the normal fault handling process will be disrupted. The effect is:

- Both the interrupted and the faulting context will be set to Halted.
- The fatal fault exception will be directed to the interrupted context rather than the Master.

14. For Additional Information

Innovasic's fido1100 is the first product in the fido™ family of real-time communication controllers. The fido communication controller architecture is uniquely optimized for solving memory bottlenecks, and is designed from the ground up for deterministic processing. Critical timing parameters, such as context switching and interrupt latency, are precisely predictable for real-time tasks. The fido1100 also incorporates the Universal I/O Controller (UIC™) that is configurable to support various communication protocols across multiple platforms. This flexibility relieves the designer of the task of searching product matrices to find the set of peripherals that most closely match the system interface needs. The Software Profiling and Integrated Debug EnviRonment (SPIDER™) has extensive real-time code debug capabilities without the burden of code instrumentation.

The fido1100 User Guide and *The fido1100 Instruction Set Reference Guide* as well as other helpful tools and files are available. For example, the GDB debugger supports both profiling and tracing of executing code.

The Innovasic Support Team is continually planning and creating tools for your use. Visit http://www.innovasic.com for up-to-date documentation and software. Our goal is to provide timely, complete, accurate, useful, and easy-to-understand information. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

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