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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CPU32
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, EIA-232, Ethernet, GPIO, HDLC, I²C, SMBus, SPI
Peripherals	DMA, POR, WDT
Number of I/O	72
Program Memory Size	32KB (32K x 8)
Program Memory Type	RREM
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/fido1100pqf208ir1

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4. Packaging, Pin Descriptions, and Physical Dimensions

Information on the packages and pin descriptions for the fido1100 communication controller PQFP, BGA 10- by 10-mm package, and BGA 15- by 15-mm package is provided individually. Refer to sections, figures, and tables for information on the device of interest.

Table 3. PQFP Pin Listing

Pin	Signal Name	Type	Description
1	AN_7	Input	Analog-to-digital converter input channel 7
2	AN_6	Input	Analog-to-digital converter input channel 6
3	AN_5	Input	Analog-to-digital converter input channel 5
4	AN_4	Input	Analog-to-digital converter input channel 4
5	AN_3	Input	Analog-to-digital converter input channel 3
6	AN_2	Input	Analog-to-digital converter input channel 2
7	AN_1	Input	Analog-to-digital converter input channel 1
8	AN_0	Input	Analog-to-digital converter input channel 0
9	VRL	Input	Analog-to-digital converter low-input reference
10	VRH	Input	Analog-to-digital converter high-input reference
11	VDDA	Power	Analog supply voltage (+3.3VDC)
12	GNDA	Ground	Analog ground
13	INT0	Input	Interrupt_0
14	INT1	Input	Interrupt_1
15	INT2	Input	Interrupt_2
16	VDDC	Power	Digital core supply voltage (+2.5VDC)
17	INT3	Input	Interrupt_3
18	INT4_DMA0_ ACK	Bidirectional	Muxed pin, Interrupt_4 or DMA channel 0 acknowledge
19	INT5_DMA1_ ACK	Bidirectional	Muxed pin, Interrupt_5 or DMA channel 1 acknowledge
20	INT6_DMA0_ REQ	Input	Muxed pin, Interrupt_6 or DMA channel 0 request
21	INT7_DMA1_ REQ	Input	Muxed pin, Interrupt_7 or DMA channel 1 request
22	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
23	D0	Bidirectional	External Bus Interface data Bit [0]
24	D1	Bidirectional	External Bus Interface data Bit [1]
25	D2	Bidirectional	External Bus Interface data Bit [2]
26	D3	Bidirectional	External Bus Interface data Bit [3]
27	D4	Bidirectional	External Bus Interface data Bit [4]
28	D5	Bidirectional	External Bus Interface data Bit [5]
29	D6	Bidirectional	External Bus Interface data Bit [6]
30	D7	Bidirectional	External Bus Interface data Bit [7]
31	GND	Ground	Digital ground
32	D8	Bidirectional	External Bus Interface data Bit [8]
33	D9	Bidirectional	External Bus Interface data Bit [9]
34	D10	Bidirectional	External Bus Interface data Bit [10]
35	D11	Bidirectional	External Bus Interface data Bit [11]

Table 3. PQFP Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
36	D12	Bidirectional	External Bus Interface data Bit [12]
37	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
38	D13	Bidirectional	External Bus Interface data Bit [13]
39	D14	Bidirectional	External Bus Interface data Bit [14]
40	D15	Bidirectional	External Bus Interface data Bit [15]
41	RDY_N	Input	External Bus Interface External Ready Indication
42	GND	Ground	Digital ground
43	MEMCLK	Output	Memory clock used by external memory
44	GND	Ground	Digital ground
45	BE0_N	Output	Byte enable 0, active low
46	BE1_N	Output	Byte enable 1, active low
47	OE_N	Output	Output enable, active low
48	VDDC	Power	Digital core supply voltage (+2.5VDC)
49	RW_N	Output	Read or write control (active low write)
50	BA_0	Output	Bank Enable 0
51	BA_1	Output	Bank Enable 1
52	CAS_N	Output	Column activate signal, active low
53	GND	Ground	Digital Ground
54	RAS_N	Output	Row activate signal, active low
55	CKE	Output	Clock enable to be used in conjunction with MEMCLK
56	HOLDREQ_N	Input	External Bus hold request, active low
57	HOLDGNT_N	Output	External Bus grant request, active low
58	RESET_N	Input	Reset input
59	RESET_OUT_N	Output	Reset output
60	GND	Ground	Digital ground
61	A0	Output	External Bus Interface address Bit [0]
62	A1	Output	External Bus Interface address Bit [1]
63	A2	Output	External Bus Interface address Bit [2]
64	A3	Output	External Bus Interface address Bit [3]
65	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
66	A4	Output	External Bus Interface address Bit [4]
67	A5	Output	External Bus Interface address Bit [5]
68	A6	Output	External Bus Interface address Bit [6]
69	A7	Output	External Bus Interface address Bit [7]
70	GND	Ground	Digital ground
71	A8	Output	External Bus Interface address Bit [8]
72	A9	Output	External Bus Interface address Bit [9]
73	A10	Output	External Bus Interface address Bit [10]
74	A11	Output	External Bus Interface address Bit [11]

Table 4. BGA 10- by 10-mm Package Pin Listing

Pin	Signal Name	Type	Description
B1	AN_7	Input	Analog-to-digital converter input channel 7
B2	AN_6	Input	Analog-to-digital converter input channel 6
C1	AN_5	Input	Analog-to-digital converter input channel 5
C2	AN_4	Input	Analog-to-digital converter input channel 4
D1	AN_3	Input	Analog-to-digital converter input channel 3
C3	AN_2	Input	Analog-to-digital converter input channel 2
D2	AN_1	Input	Analog-to-digital converter input channel 1
E1	AN_0	Input	Analog-to-digital converter input channel 0
D3	VRL	Input	Analog-to-digital converter low-input reference
E2	VRH	Input	Analog-to-digital converter high-input reference
G7	VDDA	Power	Analog supply voltage (+3.3VDC)
H7	GNDA	Ground	Analog ground
F1	INT0	Input	Interrupt_0
E3	INT1	Input	Interrupt_1
F2	INT2	Input	Interrupt_2
G8	VDDC	Power	Digital core supply voltage (+2.5VDC)
G1	INT3	Input	Interrupt_3
F3	INT4_DMA0_ ACK	Bidirectional	Muxed pin, Interrupt_4 or DMA channel 0 acknowledge
H1	INT5_DMA1_ ACK	Bidirectional	Muxed pin, Interrupt_5 or DMA channel 1 acknowledge
G2	INT6_DMA0_ REQ	Input	Muxed pin, Interrupt_6 or DMA channel 0 request
G3	INT7_DMA1_ REQ	Input	Muxed pin, Interrupt_7 or DMA channel 1 request
G9	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
J1	D0	Bidirectional	External Bus Interface data Bit [0]
H2	D1	Bidirectional	External Bus Interface data Bit [1]
H3	D2	Bidirectional	External Bus Interface data Bit [2]
K1	D3	Bidirectional	External Bus Interface data Bit [3]
J2	D4	Bidirectional	External Bus Interface data Bit [4]
J3	D5	Bidirectional	External Bus Interface data Bit [5]
L1	D6	Bidirectional	External Bus Interface data Bit [6]
K2	D7	Bidirectional	External Bus Interface data Bit [7]
H8	GND	Ground	Digital ground
K3	D8	Bidirectional	External Bus Interface data Bit [8]
M1	D9	Bidirectional	External Bus Interface data Bit [9]
L2	D10	Bidirectional	External Bus Interface data Bit [10]
L3	D11	Bidirectional	External Bus Interface data Bit [11]

Table 4. BGA 10- by 10-mm Pin Listing *(Continued)*

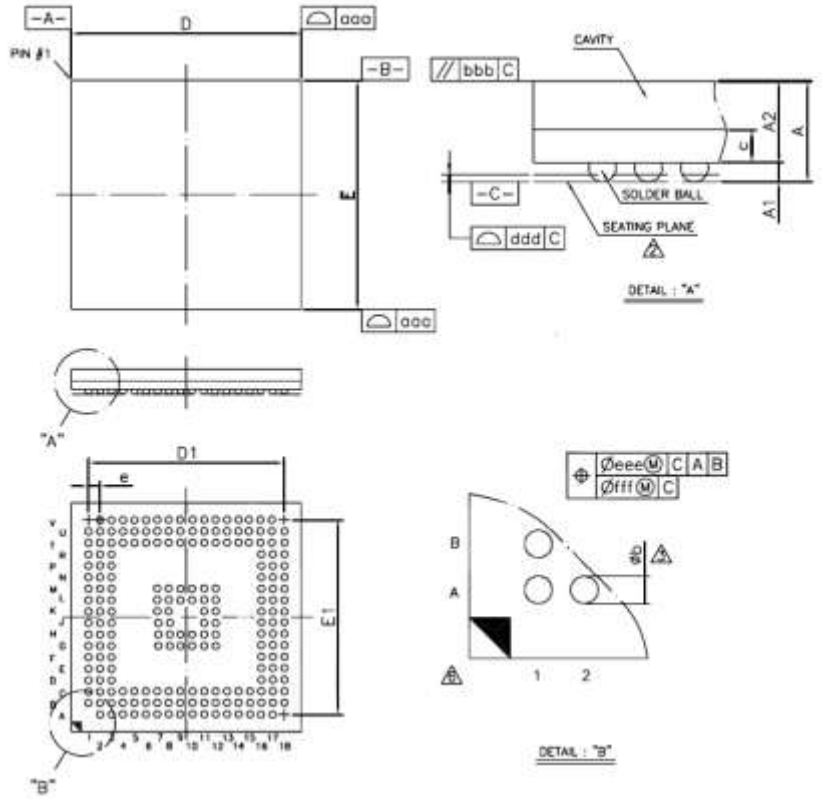
Pin	Signal Name	Type	Description
U18	UIC0_0	Bidirectional	Universal I/O Controller 0, pin 0
T17	UIC0_1	Bidirectional	Universal I/O Controller 0, pin 1
R16	UIC0_2	Bidirectional	Universal I/O Controller 0, pin 2
T18	UIC0_3	Bidirectional	Universal I/O Controller 0, pin 3
K8	GND	Ground	Digital ground
R17	UIC0_4	Bidirectional	Universal I/O Controller 0, pin 4
P16	UIC0_5	Bidirectional	Universal I/O Controller 0, pin 5
R18	UIC0_6	Bidirectional	Universal I/O Controller 0, pin 6
P17	UIC0_7	Bidirectional	Universal I/O Controller 0, pin 7
N16	UIC0_8	Bidirectional	Universal I/O Controller 0, pin 8
L12	VDDCLK	Power supply	Power Supply for the Crystal Oscillator (+2.5VDC)
P18	XTAL0	Clock	Crystal input pin 0 (Osc. In)
N18	XTAL1	Clock	Crystal input/output pin 1 (Osc. Out)
L11	GNDCLK	Ground	Digital ground
N17	UIC0_9	Bidirectional	Universal I/O Controller 0, pin 9
M17	UIC0_10	Bidirectional	Universal I/O Controller 0, pin 10
M18	UIC0_11	Bidirectional	Universal I/O Controller 0, pin 11
L16	UIC0_12	Bidirectional	Universal I/O Controller 0, pin 12
L17	UIC0_13	Bidirectional	Universal I/O Controller 0, pin 13
L18	UIC0_14	Bidirectional	Universal I/O Controller 0, pin 14
K16	UIC0_15	Bidirectional	Universal I/O Controller 0, pin 15
J16	UIC0_16	Bidirectional	Universal I/O Controller 0, pin 16
K18	UIC0_17	Bidirectional	Universal I/O Controller 0, pin 17
K11	GND	Ground	Digital ground
K17	UIC1_0	Bidirectional	Universal I/O Controller 1, pin 0
H16	UIC1_1	Bidirectional	Universal I/O Controller 1, pin 1
J18	UIC1_2	Bidirectional	Universal I/O Controller 1, pin 2
J17	UIC1_3	Bidirectional	Universal I/O Controller 1, pin 3
M7	VDDIO	Power	Digital I/O supply voltage (+3.3VDC)
G16	UIC1_4	Bidirectional	Universal I/O Controller 1, pin 4
H18	UIC1_5	Bidirectional	Universal I/O Controller 1, pin 5
H17	UIC1_6	Bidirectional	Universal I/O Controller 1, pin 6
F16	UIC1_7	Bidirectional	Universal I/O Controller 1, pin 7
G18	UIC1_8	Bidirectional	Universal I/O Controller 1, pin 8
G17	UIC1_9	Bidirectional	Universal I/O Controller 1, pin 9
M12	VDDC	Power	Digital core supply voltage (+2.5VDC)
E16	UIC1_10	Bidirectional	Universal I/O Controller 1, pin 10
F18	UIC1_11	Bidirectional	Universal I/O Controller 1, pin 11

Table 4. BGA 10- by 10-mm Pin Listing *(Continued)*

Pin	Signal Name	Type	Description
B10	UIC3_6	Bidirectional	Universal I/O Controller 3 pin 6
C9	UIC3_7	Bidirectional	Universal I/O Controller 3 pin 7
A10	UIC3_8	Bidirectional	Universal I/O Controller 3 pin 8
C8	UIC3_9	Bidirectional	Universal I/O Controller 3 pin 9
B9	UIC3_10	Bidirectional	Universal I/O Controller 3 pin 10
A9	UIC3_11	Bidirectional	Universal I/O Controller 3 pin 11
C7	UIC3_12	Bidirectional	Universal I/O Controller 3 pin 12
B8	UIC3_13	Bidirectional	Universal I/O Controller 3 pin 13
A8	GND	Ground	Digital Ground
C6	UIC3_14	Bidirectional	Universal I/O Controller 3 pin 14
B7	UIC3_15	Bidirectional	Universal I/O Controller 3 pin 15
A7	UIC3_16	Bidirectional	Universal I/O Controller 3 pin 16
B6	UIC3_17	Bidirectional	Universal I/O Controller 3 pin 17
A6	T0IC0_T0OC0	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 0 or output compare 0
C5	T0IC1_T0OC1	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 1 or output compare 1
B5	T0IC2_T0OC2	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 2 or output compare 2
A5	T0IC3_T0OC3	Bidirectional	Muxed pin, Timer Counter Unit 0 input capture 3 or output compare 3
M8	GND	Ground	Digital ground
C4	T1IC0_T1OC0	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 0 or output compare 0
B4	T1IC1_T1OC1	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 1 or output compare 1
A4	T1IC2_T1OC2	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 2 or output compare 2
B3	T1IC3_T1OC3	Bidirectional	Muxed pin, Timer Counter Unit 1 input capture 3 or output compare 3
L7	VDDC	Power	Digital core supply voltage (+2.5VDC)
A3	T0IN	Input	Timer Counter Unit 0 external clock source
A2	T1IN	Input	Timer Counter Unit 1 external clock source
M9	GND	Ground	Digital Ground
J7	VDDC	Power	Digital core supply voltage (+2.5VDC)

4.2.2 BGA 10- by 10-mm Physical Package Dimensions

The physical dimensions for the BGA 10- by 10-mm package are as shown in Figure 5.



Notes:

1. Controlling dimension: Millimeter.

2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.

4. There shall be a minimum clearance of 0.25mm between the edge of the solder ball and the body edge.

5. Special Characteristics C Class: bbb ddd.

6. The pattern of pin 1 fiducial is for reference only.

Legend:

Symbol	Dimension in mm			Dimension in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.4	0.013	0.014	0.016
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	–	8.50	–	–	0.335	–
E1	–	8.50	–	–	0.335	–
e	–	0.50	–	–	0.020	–
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	–	0.10	–	–	0.004	–
bbb	–	0.10	–	–	0.004	–
ddd	–	0.08	–	–	0.003	–
eee	–	0.15	–	–	0.006	–
fff	–	0.05	–	–	0.002	–
MD/ME	–	18/18	–	–	18/18	–

Figure 5. BGA 10- by 10-mm Physical Package Dimensions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	T1IC1_ T1OC1	T0IC2_ T0OC2	T0IC0_ T0OC0	UIC3_15	UIC3_13	UIC3_12	UIC3_9	UIC3_7	UIC3_4	UIC3_1	UIC3_0	UIC2_15	UIC2_13	UIC2_10	UIC2_7	UIC2_6	UIC1_17	A
B	AN_2	T1IC2_ T1OC2	T1IC0_ T1OC0	T0IC1_ T0OC1	UIC3_16	GND	UIC3_11	UIC3_8	UIC3_5	UIC3_2	UIC2_17	UIC2_14	UIC2_11	UIC2_8	UIC2_5	UIC2_0	UIC1_14	B
C	AN_0	AN_5	T0IN	T1IC3_ T1OC3	T0IC3_ T0OC3	UIC3_17	UIC3_14	UIC3_10	UIC3_6	UIC3_3	UIC2_16	UIC2_12	UIC2_9	UIC2_4	UIC2_1	UIC1_16	UIC1_12	C
D	VDDA	AN_1	AN_6	GND	GND	T1IN	VDDC	VDDC	VDDC	VDDIO	VDDIO	VDDIO	GND	GND	UIC2_2	UIC1_13	UIC1_9	D
E	GNDA	VRH	AN_3	GND										GND	UIC1_15	UIC1_10	UIC1_6	E
F	INT2	INT0	VRL	AN_7										UIC2_3	UIC1_11	UIC1_8	UIC1_5	F
G	INT4_ DMA0_ ACK	INT3	INT1	AN_4										VDDIO	UIC1_7	UIC1_4	UIC1_2	G
H	INT7_ DMA1_ REQ	INT6_ DMA0_ REQ	INT5_ DMA1_ ACK	VDDC										VDDIO	UIC1_3	UIC1_1	UIC1_0	H
J	D0	D1	D2	VDDIO										VDDIO	UIC0_17	UIC0_16	UIC0_15	J
K	D3	D4	D6	VDDIO										VDDC	UIC0_14	UIC0_13	UIC0_12	K
L	D5	D7	D11	OE_N										VDDC	UIC0_10	UIC0_9	UIC0_11	L
M	D8	D10	D15	CAS_N										GNDCLK	VDDCLK	UIC0_8	XTAL1	M
N	D9	D13	BE1_N	GND										GND	UIC0_5	UIC0_7	XTAL0	N
P	D12	RDY_N	BA_1	GND	GND	GND	RESET_N	VDDIO	VDDC	VDDC	A21	A26_SIZE	GND	GND	UIC0_0	UIC0_4	UIC0_6	P
R	D14	BE0_N	BA_0	RAS_N	HOLDGNT_N	A3	A6	A10	A15	A18	A22	A27_CS7_N	A29_CS5_N	CS3_N	CS2_N	UIC0_2	UIC0_3	R
T	GND	RW_N	CKE	RESET_ OUT_N	A2	A5	A8	A11	A14	A17	A20	A24	A28_CS6_N	CS0_N	CS1_N	TCK	UIC0_1	T
U	MEMCLK	HOLDREQ_N	A0	A1	A4	A7	A9	A12	A13	A16	A19	A23	A25_RESET_ DELAY	A30_CS4_N	TDI	TDO	TMS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

= Signals.
= Indicates power.
= Indicates ground.

Figure 6. BGA 15- by 15-mm Package Diagram

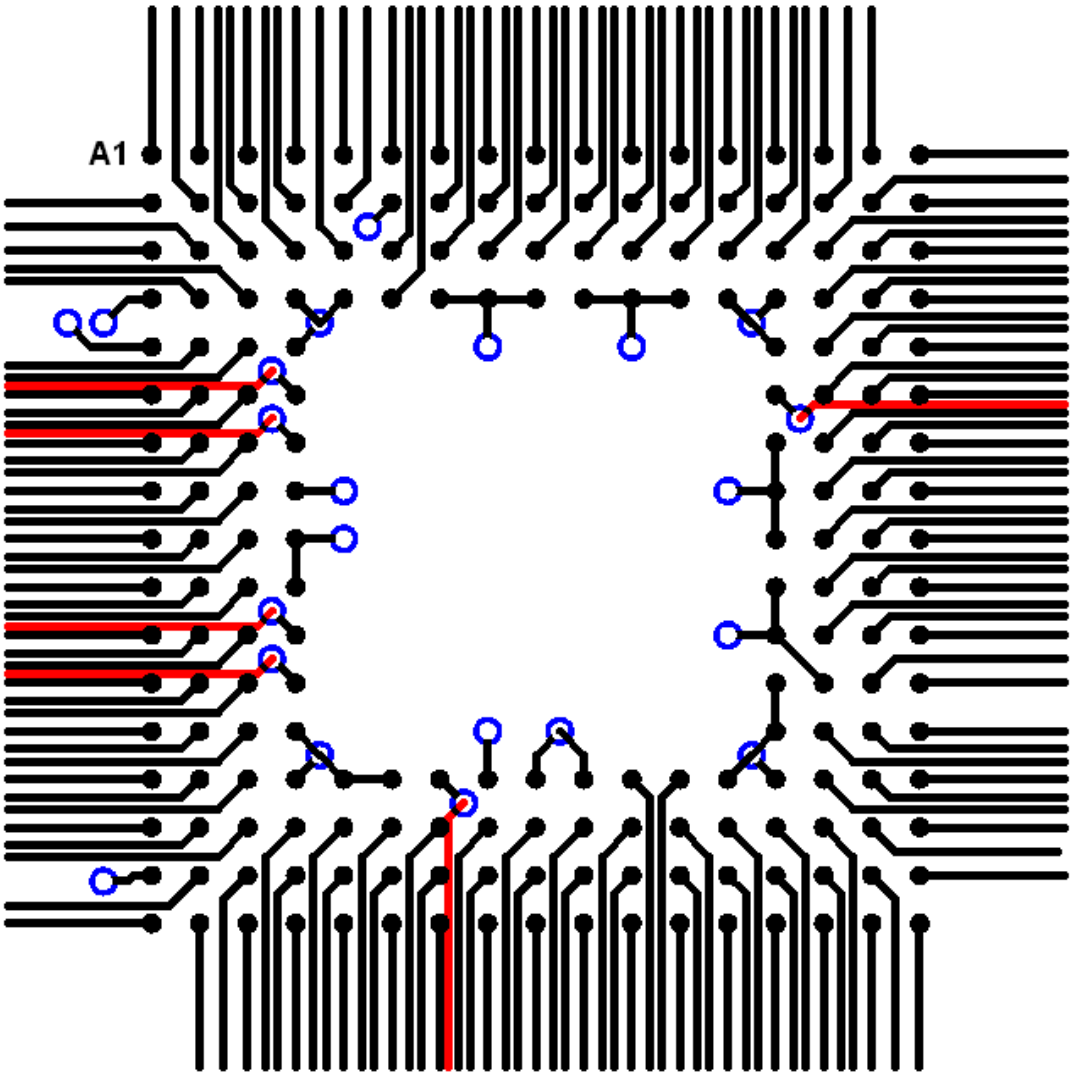


Figure 8. BGA 15- by 15-mm Signal Routing

Table 19. Analog-to-Digital Converter Characteristics

Symbol	Parameter Name	Conditions	Min	Typ	Max	Units
V_{INA}	Input voltage range	–	$0.1V_{DDA}$	-	$0.9V_{DDA}$	V
C_{INA}	Input capacitance	–	–	20	–	pF
Res	Resolution	–	–	10	–	Bits
INL	Integral non-linearity	–	–	± 2	–	Lsb
DNL	Differential non-linearity	guaranteed no missing codes	–	± 1	–	Lsb
SINAD	Signal to noise plus distortion	Fin = 10 KHz	–	54	–	dB
FSMPL	Sample clock frequency	–	0.5	–	2.6	MHz
P_D	Power dissipation	TA = 25ºC	–	5	–	mW
SMP	Sample rate	–	–	–	200	Ksps

Notes:
1. The ADC in the fido1100 uses its own VDD (VDDA) and GND (GNDA) connections along with VREF High (VRH) and VREF Low (VRL) signals.
2. VRH must be less than or equal to VDDA.
3. VRL must be greater than or equal to GNDA.
4. To ensure maximum conversion accuracy, VDDA, GNDA, VRH, and VRL should be as clean and free of noise as possible.

Table 20. Power Consumption

Conditions	Core Voltage 2.5 VDC		I/O Voltage 3.3 VDC		Total
	Current	Power	Current	Power	Power
Halted after a Reset	109.240 mA	273.100 mW	2.500 mA	8.25 mW	281.35 mW
Light Processing Load	214.000 mA	535.000 mW	7.700 mA	25.41 mW	560.41 mW
Heavy Processing Load	227.000 mA	567.500 mW	17.000 mA	56.1 mW	623.60 mW
Sleep Mode					320.90 mW
Stop Mode					302.91 mW
Low Power Stop Mode (LPSTOP)					8.68 mW

7. Reset

7.1 Overview

This section describes the reset signal considerations and the reset timing. The Power On Reset Register has a control bit to determine whether Major Reset or Minor Reset processing is performed after reset is asserted. The section below presents the hardware signal characteristics. See *The fido1100 User Guide* for more details on the Power On Reset Control Register.

7.2 Signal Considerations and Reset Timing

The fido1100 requires the RESET_N signal to be asserted LOW for a minimum of 100 µS after VDDIO and VDDC are at their nominal values and stable. The RESET_N signal must have a rise time of less than 100 nS. Table 21 presents the hardware signals involved or affected and should be considered when asserting reset.

Table 21. Hardware Signals Involved When Asserting Reset

Signal Name	Type	Description
RESET_N	Input	Reset input
RESET_OUT_N	Output	Reset output
A_25_RESET_DELAY	Muxed, Internal Pull-up	Muxed pin, External Bus Interface address Bit [25] or POR counter bypass
A_26_SIZE	Muxed, Internal Pull-up	Muxed pin, External Bus Interface address Bit [26] or data bus size select (0 = 8-bit, 1 = 16-bit)
A27_CS7_N	Muxed	Muxed pin, External Bus Interface address Bit [27] or Chip select 7 (chip select active low)
A28_CS6_N	Muxed	Muxed pin, External Bus Interface address Bit [28] or Chip select 6 (chip select active low)
A29_CS5_N	Muxed	Muxed pin, External Bus Interface address Bit [29] or Chip select 5 (chip select active low)
A30_CS4_N	Muxed	Muxed pin, External Bus Interface address Bit [30] or Chip select 4 (chip select active low)
CS0_N	Output	Chip select 0 (chip select active low)

When RESET_N is asserted, the following sequence occurs:

- The A25_Reset_Delay signal is sampled to determine the length of the reset clock delay
  - Low—reset clock delay → 100 µsecs
  - High—reset clock delay → 20 msecs

  Note: After this delay, the part performs major or minor reset processing and is released to run.
- The A_26_SIZE pin is sampled for the external bus interface size
  - Low—8-bit width
  - High—16-bit width

The following multiplexed signals are tri-stated during reset and should be pulled high if being used as chip selects or pulled low if being used as address lines (the fido1100 boots at address 0x00000000). If not being used, they can be pulled either high or low.

- A27_CS7_N
- A28_CS6_N
- A29_CS5_N
- A30_CS4_N

At Reset, the CS0_N signal defaults to low for external memory access, supporting the boot sequence from address 0x00000000.

7.3 Clock Signals

7.4 Typical Clock Source Implementations

The fido1100 can operate in one of two modes: (1) Normal or driven clock source input or (2) using an external crystal to set the operating frequency of the internal oscillator.

> *Note: VDDCLK and GNDCLK must be connected even when not using an external crystal.*

7.4.1 Normal or Driven Clock Source

System configuration—Drive external clock source into XTAL0 (see Figure 11). XTAL1 is left unconnected. XTAL0 is effectively a Schmitt trigger input. Target frequency should have a duty cycle of approximately 40% to 60%.

7.4.2 Using an External Crystal

- System Configuration (third overtone)—Crystal across XTAL0/XTAL1 (see Figure 12), 36 pF load caps to ground, 0.1-µF cap, and 0.33-µH inductor in series from XTAL1 to ground.

- System Configuration (fundamental tone)—Crystal across XTAL0/XTAL1 (see Figure 13) and 20-pF load caps to ground.

> *Note: Load capacitor and inductor values may be different based on crystal used. Please consult with your crystal supplier for more information.*

Third overtone configuration is recommended for 24- to 66-MHz operation and fundamental tone configuration is recommended for 1- to 24-MHz operation.

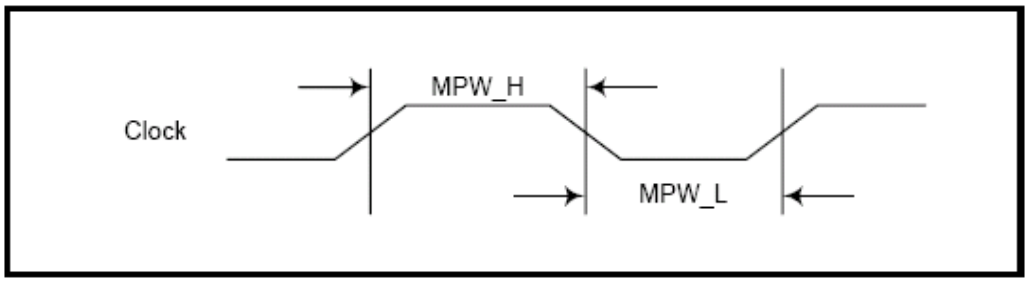
8.3 External Bus Timing

Signals listed on the External Bus Timing diagrams are described below.

- TwWAIT
  - If RDY_ENABLE=0, specifies the width of the chip select active period for the non-burst-mode write cycle. The allowed range is 0–31, resulting in a wait time of 1–32 clocks.
  - If RDY_ENABLE=1, specifies the wait time before the RDY_N line is first sampled for the write cycle. This provides a max wait time of 484 nS at 66 MHz. Anything greater than this will require the external RDY_N line and external logic.

- TrWAIT
  - If RDY_ENABLE=0, specifies the width of the chip select active period for the non-burst-mode read cycle. The allowed range is 0–31, resulting in a wait time of 1–32 clocks.
  - If RDY_ENABLE=1, specifies the wait time before the RDY_N line is first sampled for the read cycle. This provides a max wait time of 484 nS at 66 MHz. Anything greater than this will require the external RDY_N line and external logic.

- Minimum Pulse Width—The minimum length of time between the leading and trailing edges of a pulse (see Figure 19).



Timings are based on a 66-MHz clock yielding 15-ns cycles.
MPW_H = 7ns.
MPW_L = 7ns.

Figure 20. Minimum Pulse Width

- THLD—Specifies the time between when the CSn_N and BEn_N signals go inactive (hi) and the address is removed, 0–7 clocks.
- TCS—Specifies the time between when the address bus is driven and the CSn_N and BEn_N signals go active (low), 0–3 clocks.
- TOE—Specifies the time between when the CSn_N and BEn_N signals go active (low) and the OE signal goes active (low), 0–3 clocks.
- TWEF—Specifies the time between when the CSn_N and BEn_N signals go active (low) and the WE_N signal goes active (low), 0–3 clocks.
- TWER—Specifies the time between when the WE_N signal goes inactive (hi) and the CSn_N and BEn_N signals go inactive (hi), 0–3 clocks.

9.1.1 External Bus Timing for a 32-Bit Transfer (without RDY_N)

This timing is programmable via the External Bus Chip Select Timing Register (see Figure 20).

- All timing is relative to the rising edge of the clock.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go active (low) 0–3 clocks (TCS) after the address bus is driven.
- The chip-select, output-enable, and byte-enable signals (CSn_N, BEn_N, and OE_N) go inactive (hi) 0–7 clocks (THLD) before the address is removed (on the last cycle).

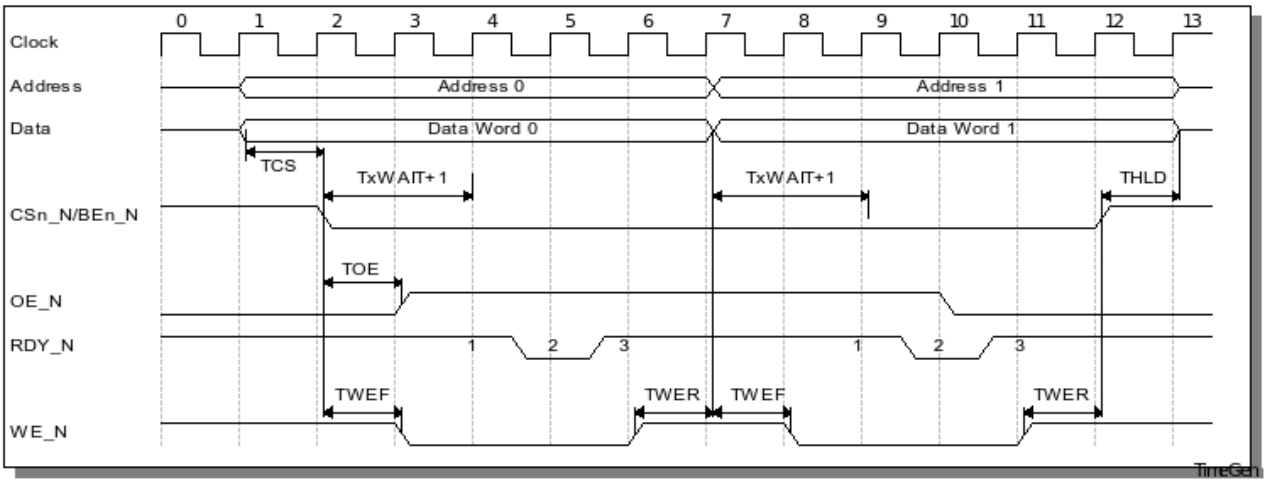


Figure 22. External Bus Timing for a 32-Bit Transfer (with RDY_N)

- The TxWAIT setting determines when first to start sampling the low active RDY_N line (labeled with an arrow marked "1" in the diagram).
- In the case of a write transfer after the low active RDY_N line is first sampled low (labeled with an arrow marked "2" in the diagram), the write cycle will complete on the next rising edge of the clock as shown (labeled with an arrow marked "3" in the diagram).
- In the case of a read transfer once the low active RDY_N line is first sampled low (labeled with an arrow marked "2" in the diagram), the read data will be sampled on the second rising edge of the clock.
- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- If the RDY_N line never goes low, the cycle will end (as a bus error) after a timeout of TxWAIT + 256 clocks.
- If the RDY_N line is unused (tied low via an internal pull down) or goes low immediately, the cycle will be controlled by TxWAIT as described above.
- In the case of a write transfer, the write-enable signal (WE_N) goes active (low) 0–3 clocks after the CS_N goes low.

- The write-enable signal (WE_N) goes inactive (hi) 0–3 clocks (TWER) before the end of the chip-select time.

9.1.3 External Bus Timing for 8-Bit/16-Bit Transfer (without RDY_N)

This timing is programmable via the External Bus Chip Select Control Register (see Figure 22).

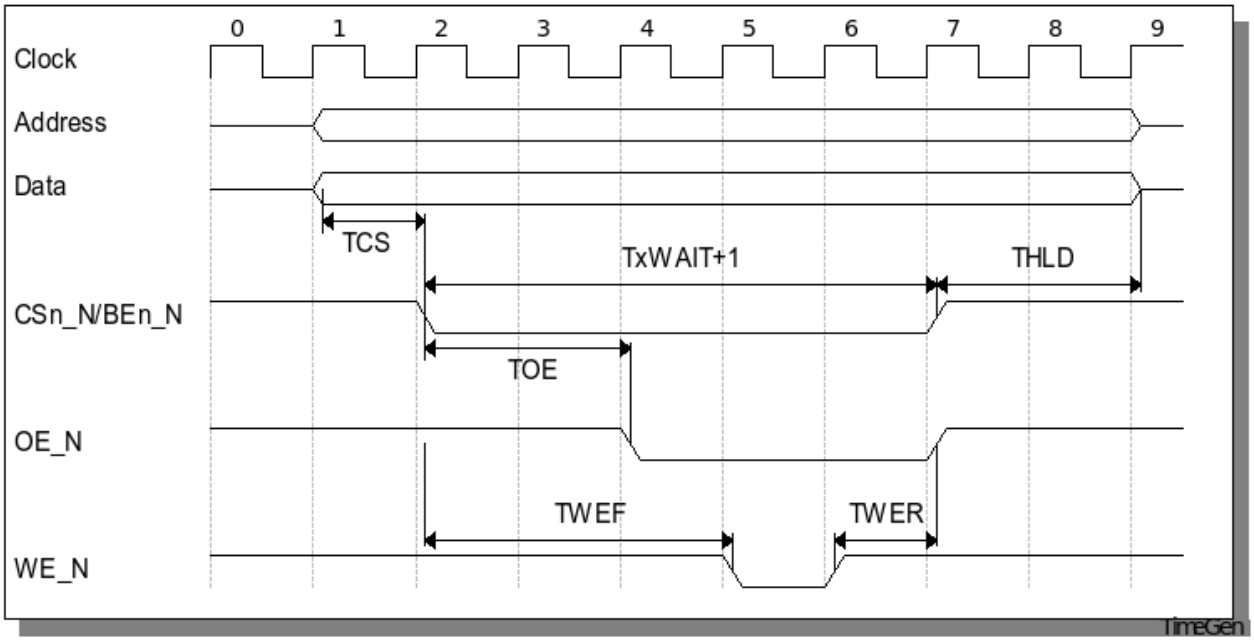


Figure 23. External Bus Timing for 8-Bit/16-Bit Transfer (without RDY_N)

- All timing is relative to the rising edge of the clock.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go active (low) 0–3 clocks (TCS) after the address bus is driven.
- The chip-select and byte-enable signals (CSn_N and BEn_N) go inactive (hi) 0–7 clocks (THLD) before the address is changed.
- The write-cycle timing is controlled by TwWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.
- The read-cycle timing is controlled by TrWAIT setting (shown as TxWAIT in the diagram), 1–16 clocks.

- ADC Control Register Bit 4 (CD-Conversion Done) will correctly indicate that conversion(s) are done.
- An ADC interrupt will be issued if ADC interrupts are enabled. ADC interrupts are enabled by setting ADC Control Register Bit 3 (IRQ_En) to 1.
- ADC Data Available Register will correctly indicate which channels have updated results in their Data Registers.

Workaround: When using non-scanning mode conversions, enable the ADC between each commanded conversion (single channel or multi-channel):

- Clear ADC Control Register Bit 7 (EN) to 0.
- Set ADC Control Register Bit 7 (EN) to 1.
- Set ADC Start Register Bit 0 (START) to 1 to start the conversion process.
- ADC Conversion complete will be indicated by:
  - An ADC interrupt, if ADC Control Register Bit 3 (IRQ_En) is set to 1.
  - ADC Control Register Bit 4 (CD-Conversion Done) will set to indicate that conversion(s) are done.

Errata No. 2

Problem: Fatal fault recovery sequence can be disturbed by interrupts.

Description:

Context Fatal Faults can occur if a context's stack pointer becomes corrupted. It is a feature of the hardware to detect this "Fatal Fault" and allow a graceful recovery by directing an exception to the Master Context. This operation can be disturbed if, by chance, an interrupt is triggered during a bus cycle leading to a Fatal Fault. This problem occurs no matter which context the interrupt is directed to. It need not be the faulting context. Furthermore, since neither interrupt timing nor fatal faults are predictable, there is no way to guarantee this cannot happen. The effect of this error depends on the interrupt mode of the context to which the interrupt is directed. If the interrupted context is running in Fast Single Threaded mode, when an interrupt targeted to it occurs during a faulting bus cycle (caused by another context) the CPU will lock up after the faulting bus cycle completes. If the interrupted context is in Standard or Fast Vectored mode the CPU will not lock up but the normal fault handling process will be disrupted. The effect is:

- Both the interrupted and the faulting context will be set to Halted.
- The fatal fault exception will be directed to the interrupted context rather than the Master.

13. Revision History

Table 26 presents the sequence of revisions to document IA211080807.

Table 26. Revision History

Date	Revision	Description	Page(s)
August 8, 2007	00	First edition released.	NA
September 11, 2008	01	Reformatted to meet publication standards. Technical data updated. Errata added.	NA
October 9, 2008	02	Changed “RESET” to “RESET_N” and “RESET_OUT” to “RESET_OUT_N” in text, figures, and tables.	17, 19, 26, 28, 35, 37, 50, 51
		In Table 5, changed pin numbers in data row 14 from “F3” to “G3”and in data row 19 from “G3” to “H3.”	36
		In Table 5, changed pin numbers in data row 11 from “M14” to “M15” and in data row 14 from “M15” to “M14.”	39
		Deleted last row of Table 5 (duplicate).	40
		In Table 7, changed numbers in data row 1 from “M14” to “M15” and in data row 2 from “M15” to “M14.”	43
		In Table 10, changed numbers in data rows 13, 14, 15, and 16 to “B6,” “P13,” “P14,” and “–,” from “P5,” “B6,” “P13,” and “P14,” respectively, for column labeled “BGA 15 x 15.”	44
		Added 2 new sentences at beginning of Section 7.2, “Signal Considerations and Reset Timing.”	50
		Changed “CLKVDD” to “VDDCLK” and “CLKGND” to “GNDCLK” in note and Figures 11, 12, and 13.	52, 53
		Updated errata chapter to reflect errata for Version 01.	76 through 87
October 10, 2008	03	To conform to publication standards, removed illustration from cover. Changed Table 24, “Part Numbers by Package Types,” to reflect Version 01 part numbers.	1, 75
March 12, 2009	04	Revised ordering information – package information; Added Errata 2.	75 - 78
July 28, 2009	05	Revised description of when bus cycle terminates in a Read cycle; Added two errata.	61, 64, 76, 78, 79
November 20, 2009	06	Updated LPSTOP power consumption.	49
April 15, 2010	07	Added BGA signal routing guidance.	43, 44
April 25, 2012	08	Added Errata 5	81