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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.15V ~ 3.6V
Data Converters	A/D 10x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f26j53t-i-ss

TABLE 1-4: PIC18F4XJ53 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	44-QFN	44-TQFP			
					PORTB (continued)
RB4/CCP4/PMA1/KBI0/SCK1/SCL1/RP7	14(3)	14(3)			
RB4			I/O	TTL/DIG	Digital I/O.
CCP4(2)			I/O	ST/DIG	Capture/Compare/PWM input/output.
PMA1(2)			I/O	ST/TTL/DIG	Parallel Master Port address.
KBI0			I	TTL	Interrupt-on-change pin.
SCK1			I/O	ST/DIG	Synchronous serial clock input/output.
SCL1			I/O	I^2C	I^2C clock input/output.
RP7			I/O	ST/DIG	Remappable Peripheral Pin 7 input/output.
RB5/CCP5/PMA0/KBI1/SDI1/SDA1/RP8	15(3)	15(3)			
RB5			I/O	TTL/DIG	Digital I/O.
CCP5			I/O	ST/DIG	Capture/Compare/PWM input/output.
PMA0(2)			I/O	ST/TTL/DIG	Parallel Master Port address.
KBI1			I	TTL	Interrupt-on-change pin.
SDI1			I	ST	SPI data input.
SDA1			I/O	I^2C	I^2C data input/output.
RP8			I/O	ST/DIG	Remappable Peripheral Pin 8 input/output.
RB6/CCP6/KBI2/PGC/RP9	16(3)	16(3)			
RB6			I/O	TTL/DIG	Digital I/O.
CCP6			I/O	ST/DIG	Capture/Compare/PWM input/output.
KBI2			I	TTL	Interrupt-on-change pin.
PGC			I	ST	ICSP™ clock input.
RP9			I/O	ST/DIG	Remappable Peripheral Pin 9 input/output.
RB7/CCP7/KBI3/PGD/RP10	17(3)	17(3)			
RB7			I/O	TTL/DIG	Digital I/O.
CCP7			I/O	ST/DIG	Capture/Compare/PWM input/output.
KBI3			I	TTL	Interrupt-on-change pin.
PGD			I/O	ST/DIG	In-Circuit Debugger and ICSP programming data pin.
RP10			I/O	ST/DIG	Remappable Peripheral Pin 10 input/output.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); DIG = Digital output; I^2C = Open-Drain, I^2C specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

2: Available only on 44-pin devices (PIC18F46J53, PIC18F47J53, PIC18LF46J53 and PIC18LF47J53).

3: 5.5V tolerant.

TABLE 4-1: LOW-POWER MODES

Mode	DSCONH<7>	OSCCON<7,1:0>		Module Clocking		Available Clock and Oscillator Source
	DSEN(1)	IDLEN(1)	SCS<1:0>	CPU	Peripherals	
Sleep	0	0	N/A	Off	Off	Timer1 oscillator and/or RTCC may optionally be enabled
Deep Sleep(3)	1	0	N/A	Powered off(2)	Powered off	RTCC can run uninterrupted using the Timer1 or internal low-power RC oscillator
PRI_RUN	0	N/A	00	Clocked	Clocked	The normal, full-power execution mode; primary clock source (defined by FOSC<2:0>)
SEC_RUN	0	N/A	01	Clocked	Clocked	Secondary – Timer1 oscillator
RC_RUN	0	N/A	11	Clocked	Clocked	Postscaled internal clock
PRI_IDLE	0	1	00	Off	Clocked	Primary clock source (defined by FOSC<2:0>)
SEC_IDLE	0	1	01	Off	Clocked	Secondary – Timer1 oscillator
RC_IDLE	0	1	11	Off	Clocked	Postscaled internal clock

Note 1: IDLEN and DSEN reflect their values when the SLEEP instruction is executed.

2: Deep Sleep turns off the internal core voltage regulator to power down core logic. See **Section 4.6 "Deep Sleep Mode"** for more information.

3: Deep Sleep mode is only available on "F" devices, not "LF" devices.

4.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Two bits indicate the current clock source and its status: OSTS (OSCCON<3>) and SOSCRUN (OSCCON2<6>). In general, only one of these bits will be set in a given power-managed mode. When the OSTS bit is set, the primary clock would be providing the device clock. When the SOSCRUN bit is set, the Timer1 oscillator would be providing the clock. If neither of these bits is set, INTRC would be clocking the device.

Note:	Executing a SLEEP instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep or Deep Sleep mode, or one of the Idle modes, depending on the setting of the IDLEN bit.

4.1.4 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the SLEEP instruction is determined by the setting of the IDLEN and DSEN bits at the time the instruction is executed. If another SLEEP instruction is executed, the device will enter the power-managed mode specified by IDLEN and DSEN at that time. If IDLEN or DSEN have changed, the device will enter the new power-managed mode specified by the new setting.

4.4 Idle Modes

The Idle modes allow the controller's CPU to be selectively shut down while the peripherals continue to operate. Selecting a particular Idle mode allows users to further manage power consumption.

If the IDLEN bit is set to '1' when a SLEEP instruction is executed, the peripherals will be clocked from the clock source selected using the SCS<1:0> bits; however, the CPU will not be clocked. The clock source status bits are not affected. Setting IDLEN and executing a SLEEP instruction provides a quick method of switching from a given Run mode to its corresponding Idle mode.

If the WDT is selected, the INTRC source will continue to operate. If the Timer1 oscillator is enabled, it will also continue to run.

Since the CPU is not executing instructions, the only exits from any of the Idle modes are by interrupt, WDT time-out or a Reset. When a wake event occurs, CPU execution is delayed by an interval of TCSD (parameter 38, Table 31-14) while it becomes ready to execute code. When the CPU begins executing code, it resumes with the same clock source for the current Idle mode. For example, when waking from RC_IDLE mode, the internal oscillator block will clock the CPU and peripherals (in other words, RC_RUN mode). The IDLEN and SCS bits are not affected by the wake-up.

While in any Idle or Sleep mode, a WDT time-out will result in a WDT wake-up to the Run mode currently specified by the SCS<1:0> bits.

4.4.1 PRI_IDLE MODE

This mode is unique among the three low-power Idle modes, in that it does not disable the primary device clock. For timing-sensitive applications, this allows for the fastest resumption of device operation with its more accurate primary clock source, since the clock source does not have to "warm up" or transition from another oscillator.

PRI_IDLE mode is entered from PRI_RUN mode by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then set the SCS bits to '00' and execute SLEEP. Although the CPU is disabled, the peripherals continue to be clocked from the primary clock source specified by the FOSC<1:0> Configuration bits. The OSTS bit remains set (see Figure 4-7).

When a wake event occurs, the CPU is clocked from the primary clock source. A delay of interval, TCSD, is required between the wake event and when code execution starts. This is required to allow the CPU to become ready to execute instructions. After the wake-up, the OSTS bit remains set. The IDLEN and SCS bits are not affected by the wake-up (see Figure 4-8).

4.4.2 SEC_IDLE MODE

In SEC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the Timer1 oscillator. This mode is entered from SEC_RUN by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then set SCS<1:0> to '01' and execute SLEEP. When the clock source is switched to the Timer1 oscillator, the primary oscillator is shut down, the OSTS bit is cleared and the SOSCRUN bit is set.

When a wake event occurs, the peripherals continue to be clocked from the Timer1 oscillator. After an interval of TCSD following the wake event, the CPU begins executing code being clocked by the Timer1 oscillator. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run (see Figure 4-8).

Note:	The Timer1 oscillator should already be running prior to entering SEC_IDLE mode. If the T1OSCEN bit is not set when the SLEEP instruction is executed, the SLEEP instruction will be ignored and entry to SEC_IDLE mode will not occur. If the Timer1 oscillator is enabled, but not yet running, peripheral clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset, Wake From Deep Sleep	MCLR Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
PSTR1CON	PIC18F2XJ53	PIC18F4XJ53	00-0 0001	00-0 0001	uu-u uuuu
ECCP1AS	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
ECCP1DEL	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
CCPR1H	PIC18F2XJ53	PIC18F4XJ53	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1L	PIC18F2XJ53	PIC18F4XJ53	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
PSTR2CON	PIC18F2XJ53	PIC18F4XJ53	00-0 0001	00-0 0001	uu-u uuuu
ECCP2AS	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
ECCP2DEL	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
CCPR2H	PIC18F2XJ53	PIC18F4XJ53	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2L	PIC18F2XJ53	PIC18F4XJ53	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
CTMUCONH	PIC18F2XJ53	PIC18F4XJ53	0-00 000-	0-00 000-	u-uu uuu-
CTMUCONL	PIC18F2XJ53	PIC18F4XJ53	0000 00xx	0000 00xx	uuuu uuuu
CTMUICON	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
SPBRG1	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
RCREG1	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
TXREG1	PIC18F2XJ53	PIC18F4XJ53	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA1	PIC18F2XJ53	PIC18F4XJ53	0000 0010	0000 0010	uuuu uuuu
RCSTA1	PIC18F2XJ53	PIC18F4XJ53	0000 000x	0000 000x	uuuu uuuu
SPBRG2	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
RCREG2	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
TXREG2	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
TXSTA2	PIC18F2XJ53	PIC18F4XJ53	0000 0010	0000 0010	uuuu uuuu
EECON2	PIC18F2XJ53	PIC18F4XJ53	---- ----	---- ----	---- ----
EECON1	PIC18F2XJ53	PIC18F4XJ53	--00 x00-	--00 u00-	--00 u00-
IPR3	PIC18F2XJ53	PIC18F4XJ53	1111 1111	1111 1111	uuuu uuuu
PIR3	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu(3)
PIE3	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu
IPR2	PIC18F2XJ53	PIC18F4XJ53	1111 1111	1111 1111	uuuu uuuu
PIR2	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu(3)
PIE2	PIC18F2XJ53	PIC18F4XJ53	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

5: Not implemented for PIC18F2XJ53 devices.

6: Not implemented for "LF" devices.

TABLE 6-3: NON-ACCESS BANK SPECIAL FUNCTION REGISTER MAP

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
F5Fh	PMCONH	F3Fh	RTCCFG	F1Fh	PR6	EFFh	RPINR24	EDFh	—	EBFh	PPSCON
F5Eh	PMCONL	F3Eh	RTCCAL	F1Eh	T6CON	EFEh	RPINR23	EDEh	—	EBEh	—
F5Dh	PMMODEH	F3Dh	REFOCON	F1Dh	TMR8	EFDh	RPINR22	EDDh	—	EBDh	—
F5Ch	PMMODEL	F3Ch	PADCFG1	F1Ch	PR8	EFCh	RPINR21	EDCh	—	EBCh	PMDIS3
F5Bh	PMDOUT2H	F3Bh	RTCVALH	F1Bh	T8CON	EFBh	—	EDBh	—	EBBh	PMDIS2
F5Ah	PMDOUT2L	F3Ah	RTCVALL	F1Ah	PSTR3CON	EFAh	—	EDAh	—	EBAh	PMDIS1
F59h	PMDIN2H	F39h	UCFG	F19h	ECCP3AS	EF9h	—	ED9h	—	EB9h	PMDIS0
F58h	PMDIN2L	F38h	UADDR	F18h	ECCP3DEL	EF8h	RPINR17	ED8h	RPOR24	EB8h	ADCTRIG
F57h	PMEH	F37h	UEIE	F17h	CCPR3H	EF7h	RPINR16	ED7h	RPOR23	EB7h	—
F56h	PMEL	F36h	UIE	F16h	CCPR3L	EF6h	—	ED6h	RPOR22	EB6h	—
F55h	PMSTATH	F35h	UEP15	F15h	CCP3CON	EF5h	—	ED5h	RPOR21	EB5h	—
F54h	PMSTATL	F34h	UEP14	F14h	CCPR4H	EF4h	RPINR14	ED4h	RPOR20	EB4h	—
F53h	CVRCON	F33h	UEP13	F13h	CCPR4L	EF3h	RPINR13	ED3h	RPOR19	EB3h	—
F52h	CCPTMRS0	F32h	UEP12	F12h	CCP4CON	EF2h	RPINR12	ED2h	RPOR18	EB2h	—
F51h	CCPTMRS1	F31h	UEP11	F11h	CCPR5H	EF1h	—	ED1h	RPOR17	EB1h	—
F50h	CCPTMRS2	F30h	UEP10	F10h	CCPR5L	EF0h	—	ED0h	—	EB0h	—
F4Fh	DSGPR1	F2Fh	UEP9	F0Fh	CCP5CON	EEFh	—	ECFh	—		
F4Eh	DSGPR0	F2Eh	UEP8	F0Eh	CCPR6H	EEEh	—	ECEh	—		
F4Dh	DSCONH	F2Dh	UEP7	F0Dh	CCPR6L	EEDh	—	ECDh	RPOR13		
F4Ch	DSCONL	F2Ch	UEP6	F0Ch	CCP6CON	EECh	—	ECCh	RPOR12		
F4Bh	DSWAKEH	F2Bh	UEP5	F0Bh	CCPR7H	EEBh	—	ECBh	RPOR11		
F4Ah	DSWAKEL	F2Ah	UEP4	F0Ah	CCPR7L	EEAh	RPINR9	ECAh	RPOR10		
F49h	ANCON1	F29h	UEP3	F09h	CCP7CON	EE9h	RPINR8	EC9h	RPOR9		
F48h	ANCON0	F28h	UEP2	F08h	CCPR8H	EE8h	RPINR7	EC8h	RPOR8		
F47h	ALRMCFG	F27h	UEP1	F07h	CCPR8L	EE7h	RPINR15	EC7h	RPOR7		
F46h	ALRMRPT	F26h	UEP0	F06h	CCP8CON	EE6h	RPINR6	EC6h	RPOR6		
F45h	ALRMVALH	F25h	CM3CON	F05h	CCPR9H	EE5h	—	EC5h	RPOR5		
F44h	ALRMVALL	F24h	TMR5H	F04h	CCPR9L	EE4h	RPINR4	EC4h	RPOR4		
F43h	—	F23h	TMR5L	F03h	CCP9CON	EE3h	RPINR3	EC3h	RPOR3		
F42h	ODCON1	F22h	T5CON	F02h	CCPR10H	EE2h	RPINR2	EC2h	RPOR2		
F41h	ODCON2	F21h	T5GCON	F01h	CCPR10L	EE1h	RPINR1	EC1h	RPOR1		
F40h	ODCON3	F20h	TMR6	F00h	CCP10CON	EE0h	—	EC0h	RPOR0		

TABLE 6-4: REGISTER FILE SUMMARY (PIC18F47J53 FAMILY) (CONTINUED)

Addr.	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
F7Fh	SPBRGH1	EUSART1 Baud Rate Generator High Byte								0000 0000
F7Eh	BAUDCON1	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	0100 0-00
F7Dh	SPBRGH2	EUSART2 Baud Rate Generator High Byte								0000 0000
F7Ch	BAUDCON2	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	0100 0-00
F7Bh	TMR3H	Timer3 Register High Byte								xxxx xxxx
F7Ah	TMR3L	Timer3 Register Low Byte								xxxx xxxx
F79h	T3CON	TMR3CS1	TMR3CS0	T3CKPS1	T3CKPS0	T3OSCEN	$\overline{\text{T3SYNC}}$	RD16	TMR3ON	0000 0000
F78h	TMR4	Timer4 Register								0000 0000
F77h	PR4	Timer4 Period Register								1111 1111
F76h	T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000
F75h	SSP2BUF	MSSP2 Receive Buffer/Transmit Register								xxxx xxxx
F74h	SSP2ADD	MSSP2 Address Register (I^2C Slave Mode). MSSP2 Baud Rate Reload Register (I^2C Master Mode).								---- ----
F74h	SSP2MSK	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	0000 0000
F73h	SSP2STAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	1111 1111
F72h	SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000
F71h	SSP2CON2	GCEN	ACKSTAT	ACKDT ADMSK5	ACKEN ADMSK4	RCEN ADMSK3	PEN ADMSK2	RSEN ADMSK1	SEN	0000 0000
F70h	CMSTAT	—	—	—	—	—	COUT3	COUT2	COUT1	---- -111
F6Fh	PMADDRH/ PMDOUT1H(1)	—	CS1	Parallel Master Port Address High Byte						-000 0000
		Parallel Port Out Data High Byte (Buffer 1)								0000 0000
F6Eh	PMADDRL/ PMDOUT1L(1)	Parallel Master Port Address Low Byte/ Parallel Port Out Data Low Byte (Buffer 1)								0000 0000
F6Dh	PMDIN1H(1)	Parallel Port In Data High Byte (Buffer 1)								0000 0000
F6Ch	PMDIN1L(1)	Parallel Port In Data Low Byte (Buffer 1)								0000 0000
F6Bh	TXADDRL	SPI DMA Transmit Data Pointer Low Byte								xxxx xxxx
F6Ah	TXADDRH	—	—	—	—	SPI DMA Transmit Data Pointer High Byte				---- xxxx
F69h	RXADDRL	SPI DMA Receive Data Pointer Low Byte								xxxx xxxx
F68h	RXADDRH	—	—	—	—	SPI DMA Receive Data Pointer High Byte				---- xxxx
F67h	DMABCL	SPI DMA Byte Count Low Byte								xxxx xxxx
F66h	DMABCH	—	—	—	—	—	—	SPI DMA Byte Count High Byte		---- --xx
F65h	UCON(1)	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	-0x0 000-
F64h	USTAT	—	ENDP3	ENDP2	ENDP1	ENDP0	DIR	PPBI	—	-xxx xxx-
F63h	UEIR	BTSEF	—	—	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0--0 0000
F62h	UIR	—	SOFIF	STALLIF	IDLEIF	TRNIF	ACTVIF	UERRIF	URSTIF	-000 0000
F61h	UFRMH	—	—	—	—	—	FRM10	FRM9	FRM8	---- -xxx
F60h	UFRML	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0	xxxx xxxx
F5Fh	PMCONH(1)	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	0-00 0000
F5Eh	PMCONL(1)	CSF1	CSF0	ALP	—	CS1P	BEP	WRSP	RDSP	000- 0000
F5Dh	PMMODEH(1)	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	0000 0000
F5Ch	PMMODEL(1)	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	0000 0000
F5Bh	PMDOUT2H(1)	Parallel Port Out Data High Byte (Buffer 2)								0000 0000
F5Ah	PMDOUT2L(1)	Parallel Port Out Data Low Byte (Buffer 2)								0000 0000
F59h	PMDIN2H(1)	Parallel Port In Data High Byte (Buffer 2)								0000 0000
F58h	PMDIN2L(1)	Parallel Port In Data Low Byte (Buffer 2)								0000 0000
F57h	PMEH(1)	PTEN15	PTEN14	PTEN13	PTEN12	PTEN11	PTEN10	PTEN9	PTEN8	0000 0000
F56h	PMEL(1)	PTEN7	PTEN6	PTEN5	PTEN4	PTEN3	PTEN2	PTEN1	PTEN0	0000 0000
F55h	PMSTATH(1)	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	00-- 0000
F54h	PMSTATL(1)	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	10-- 1111

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify

Note 1: Implemented only for 44-pin devices (PIC18F46J53, PIC18F47J53, PIC18LF46J53 and PIC18LF47J53).

2: Implemented only for 28-pin devices (PIC18F26J53, PIC18F27J53, PIC18LF26J53 and PIC18LF27J53).

3: Implemented only for devices with 128 Kbyte of program memory (PIC18F27J53, PIC18F47J53, PIC18LF27J53 and PIC18LF47J53).

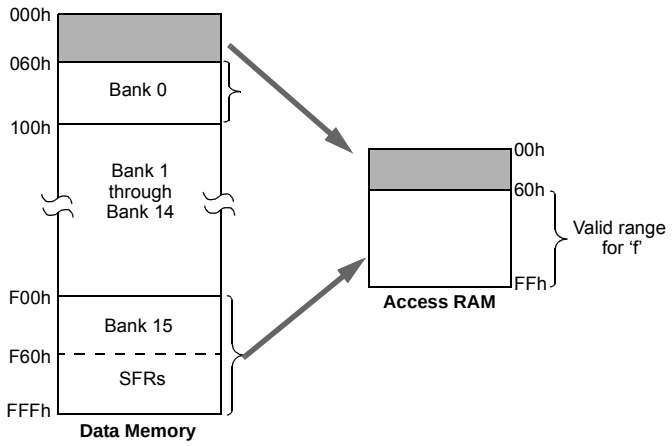
FIGURE 6-9: COMPARING ADDRESSING OPTIONS FOR BIT-ORIENTED AND BYTE-ORIENTED INSTRUCTIONS (EXTENDED INSTRUCTION SET ENABLED)

EXAMPLE INSTRUCTION: `ADDWF, f, d, a` (Opcode: `0010 01da ffff ffff`)

When a = 0 and f ≥ 60h:

The instruction executes in Direct Forced mode. 'f' is interpreted as a location in the Access RAM between 060h and FFFh. This is the same as locations, F60h to FFFh (Bank 15), of data memory.

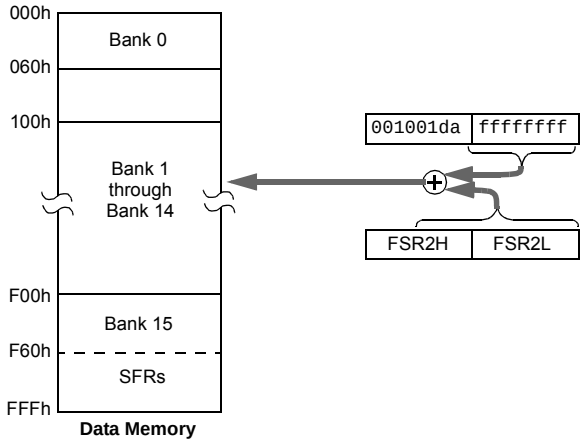
Locations below 060h are not available in this addressing mode.



When a = 0 and f ≤ 5Fh:

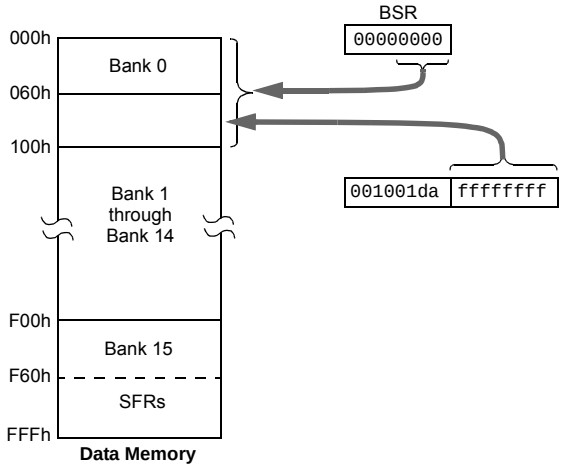
The instruction executes in Indexed Literal Offset mode. 'f' is interpreted as an offset to the address value in FSR2. The two are added together to obtain the address of the target register for the instruction. The address can be anywhere in the data memory space.

Note that in this mode, the correct syntax is:
`ADDWF [k], d`
where 'k' is the same as 'f'.



When a = 1 (all values of f):

The instruction executes in Direct mode (also known as Direct Long mode). 'f' is interpreted as a location in one of the 16 banks of the data memory space. The bank is designated by the Bank Select Register (BSR). The address can be in any implemented bank in the data memory space.



REGISTER 10-42: RPOR21: PERIPHERAL PIN SELECT OUTPUT REGISTER 21 (BANKED ED5h)(1)

U-0	U-0	U-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0
—	—	—	RP21R4	RP21R3	RP21R2	RP21R1	RP21R0
bit 7							bit 0

Legend:	R/$\overline{W}$ = Readable bit, Writable bit if IOLOCK = 0		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP21R<4:0>:** Peripheral Output Function is Assigned to RP21 Output Pin bits
(see Table 10-14 for peripheral function numbers)

Note 1: RP21 pins are not available on 28-pin devices.

REGISTER 10-43: RPOR22: PERIPHERAL PIN SELECT OUTPUT REGISTER 22 (BANKED ED6h)(1)

U-0	U-0	U-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0
—	—	—	RP22R4	RP22R3	RP22R2	RP22R1	RP22R0
bit 7							bit 0

Legend:	R/$\overline{W}$ = Readable bit, Writable bit if IOLOCK = 0		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP22R<4:0>:** Peripheral Output Function is Assigned to RP22 Output Pin bits
(see Table 10-14 for peripheral function numbers)

Note 1: RP22 pins are not available on 28-pin devices.

REGISTER 10-44: RPOR23: PERIPHERAL PIN SELECT OUTPUT REGISTER 23 (BANKED ED7h)(1)

U-0	U-0	U-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0
—	—	—	RP23R4	RP23R3	RP23R2	RP23R1	RP23R0
bit 7							bit 0

Legend:	R/$\overline{W}$ = Readable bit, Writable bit if IOLOCK = 0		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RP23R<4:0>:** Peripheral Output Function is Assigned to RP23 Output Pin bits
(see Table 10-14 for peripheral function numbers)

Note 1: RP23 pins are not available on 28-pin devices.

REGISTER 15-3: OSCCON2: OSCILLATOR CONTROL REGISTER 2 (ACCESS F87h)

U-0	R-0(2)	U-0	R/W-1	R/W-0(2)	R/W-1	U-0	U-0
—	SOSCRUN	—	SOSCDRV	SOSCGO(3)	PRISD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **SOSCRUN:** SOSC Run Status bit
1 = System clock comes from secondary SOSC
0 = System clock comes from an oscillator other than SOSC

bit 5 **Unimplemented:** Read as '0'

bit 4 **SOSCDRV:** SOSC Drive Control bit
1 = T1OSC/SOSC circuit oscillator drive circuit selected by Configuration bits, CONFIG2L<4:3>
0 = Low-power T1OSC/SOSC circuit is selected

bit 3 **SOSCGO:** Oscillator Start Control bit
1 = Turns on the oscillator, even if no peripherals are requesting it.
0 = Oscillator is shut off unless peripherals are requesting it

bit 2 **PRISD:** Primary Oscillator Drive Circuit shutdown
1 = Oscillator drive circuit on
0 = Oscillator drive circuit off (zero power)

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Reset value is '0' when Two-Speed Start-up is enabled and '1' if disabled.
2: Default output frequency of INTOSC on Reset (4 MHz).
3: When the SOSC is selected to run from a digital clock input, rather than an external crystal, this bit has no effect.

15.5.4 TIMER3/5 GATE SINGLE PULSE MODE

When Timer3/5 Gate Single Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer3/5 Gate Single Pulse mode is first enabled by setting the TxGSPM bit (TxGCON<4>). Next, the TxGGO/$\overline{\text{TxDONE}}$ bit (TxGCON<3>) must be set.

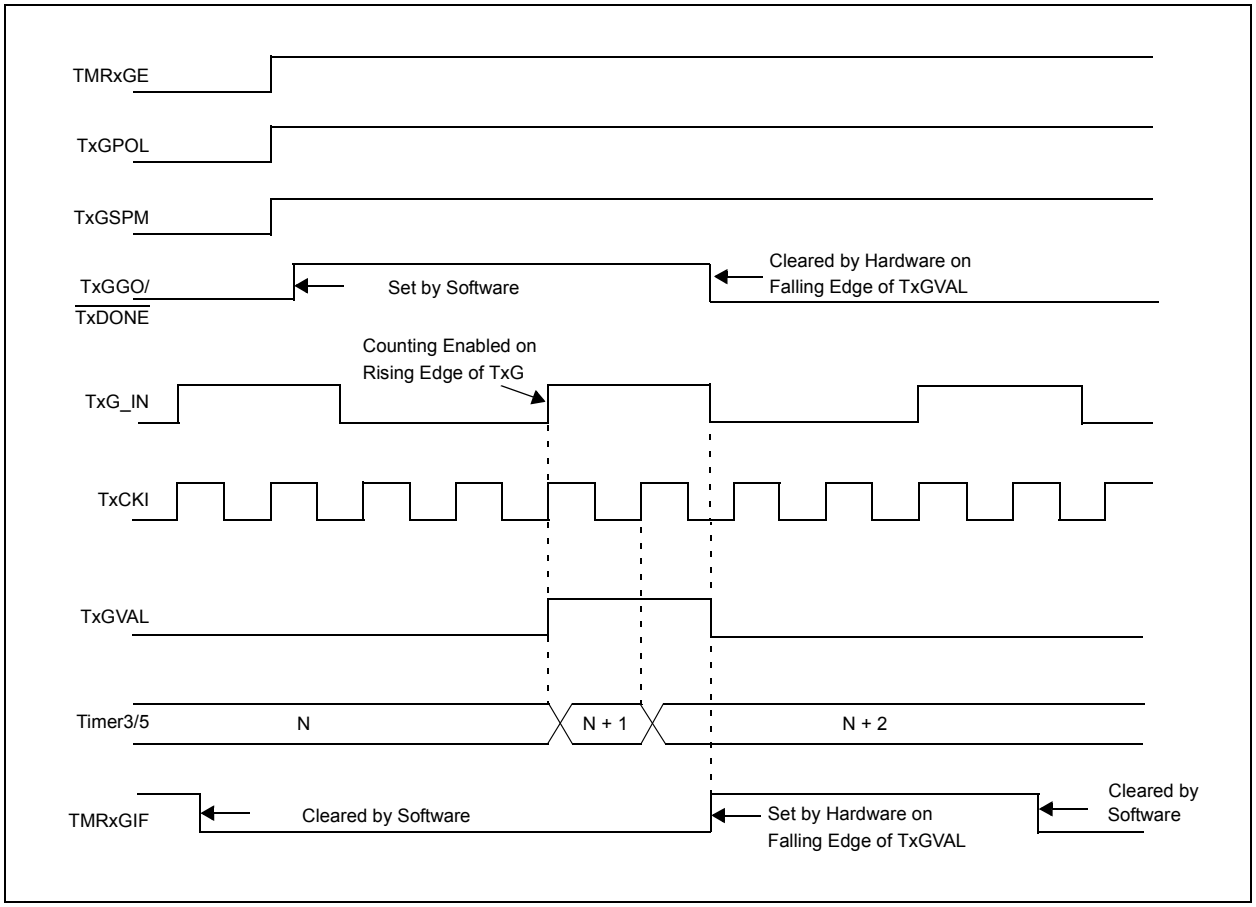
The Timer3/5 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the TxGGO/$\overline{\text{TxDONE}}$ bit will automatically be cleared.

No other gate events will be allowed to increment Timer3/5 until the TxGGO/$\overline{\text{TxDONE}}$ bit is once again set in software.

Clearing the TxGSPM bit will also clear the TxGGO/$\overline{\text{TxDONE}}$ bit. (For timing details, see Figure 15-4.)

Simultaneously, enabling the Toggle mode and the Single Pulse mode will permit both sections to work together. This allows the cycle times on the Timer3/5 gate source to be measured. (For timing details, see Figure 15-5.)

FIGURE 15-4: TIMER3/5 GATE SINGLE PULSE MODE



17.1.2 RTCVALH AND RTCVALL REGISTER MAPPINGS

REGISTER 17-6: RESERVED REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 17-7: YEAR: YEAR VALUE REGISTER(1)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to the YEAR register is only allowed when RTCWREN = 1.

REGISTER 17-8: MONTH: MONTH VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 3-0 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 20-3: DMACON1: DMA CONTROL REGISTER 1 (ACCESS F88h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSCON1	SSCON0	TXINC	RXINC	DUPLEX1	DUPLEX0	DLYINTEN	DMAEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SSCON<1:0>:** $\overline{\text{SSDMA}}$ Output Control bits (Master modes only)
11 = $\overline{\text{SSDMA}}$ is asserted for the duration of 4 bytes; DLYINTEN is always reset low
01 = $\overline{\text{SSDMA}}$ is asserted for the duration of 2 bytes; DLYINTEN is always reset low
10 = $\overline{\text{SSDMA}}$ is asserted for the duration of 1 byte; DLYINTEN is always reset low
00 = $\overline{\text{SSDMA}}$ is not controlled by the DMA module; DLYINTEN bit is software programmable

bit 5 **TXINC:** Transmit Address Increment Enable bit
Allows the transmit address to increment as the transfer progresses.
1 = The transmit address is to be incremented from the initial value of TXADDR<11:0>
0 = The transmit address is always set to the initial value of TXADDR<11:0>

bit 4 **RXINC:** Receive Address Increment Enable bit
Allows the receive address to increment as the transfer progresses.
1 = The received address is to be incremented from the initial value of RXADDR<11:0>
0 = The received address is always set to the initial value of RXADDR<11:0>

bit 3-2 **DUPLEX<1:0>:** Transmit/Receive Operating Mode Select bits
10 = SPI DMA operates in Full-Duplex mode, data is simultaneously transmitted and received
01 = DMA operates in Half-Duplex mode, data is transmitted only
00 = DMA operates in Half-Duplex mode, data is received only

bit 1 **DLYINTEN:** Delay Interrupt Enable bit
Enables the interrupt to be invoked after the number of T_{CY} cycles specified in DLYCYC<2:0> has elapsed from the latest completed transfer.
1 = The interrupt is enabled, SSCON<1:0> must be set to '00'
0 = The interrupt is disabled

bit 0 **DMAEN:** DMA Operation Start/Stop bit
This bit is set by the users' software to start the DMA operation. It is reset back to zero by the DMA engine when the DMA operation is completed or aborted.
1 = DMA is in session
0 = DMA is not in session

REGISTER 20-6: SSPxCON1: MSSPx CONTROL REGISTER 1 (I^2C MODE) (1, ACCESS FC6h; 2, F73h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN(1)	CKP	SSPM3(2)	SSPM2(2)	SSPM1(2)	SSPM0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL:** Write Collision Detect bit

In Master Transmit mode:
1 = A write to the SSPxBUF register was attempted while the I^2C conditions were not valid for a transmission to be started (must be cleared in software)
0 = No collision

In Slave Transmit mode:
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

In Receive mode (Master or Slave modes):
This is a "don't care" bit.

bit 6 **SSPOV:** Receive Overflow Indicator bit

In Receive mode:
1 = A byte is received while the SSPxBUF register is still holding the previous byte (must be cleared in software)
0 = No overflow

In Transmit mode:
This is a "don't care" bit in Transmit mode.

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(1)
1 = Enables the serial port and configures the SDAx and SCLx pins as the serial port pins
0 = Disables the serial port and configures these pins as I/O port pins

bit 4 **CKP:** SCKx Release Control bit

In Slave mode:
1 = Releases clock
0 = Holds clock low (clock stretch); used to ensure data setup time

In Master mode:
Unused in this mode.

bit 3-0 **SSPM<3:0>:** Master Synchronous Serial Port Mode Select bits(2)
1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I^2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1011 = I^2C Firmware Controlled Master mode (slave Idle)
1001 = Load the SSPxMSK register at the SSPxADD SFR address(3,4)
1000 = I^2C Master mode, clock = FOSC/(4 * (SSPxADD + 1))
0111 = I^2C Slave mode, 10-bit address
0110 = I^2C Slave mode, 7-bit address

Note 1: When enabled, the SDAx and SCLx pins must be configured as inputs.
2: Bit combinations not specifically listed here are either reserved or implemented in SPI mode only.
3: When SSPM<3:0> = 1001, any reads or writes to the SSPxADD SFR address actually accesses the SSPxMSK register.
4: This mode is only available when 7-Bit Address Masking mode is selected (MSSPMSK Configuration bit is '1').

FIGURE 20-29: BUS COLLISION DURING START CONDITION (SCLx = 0)

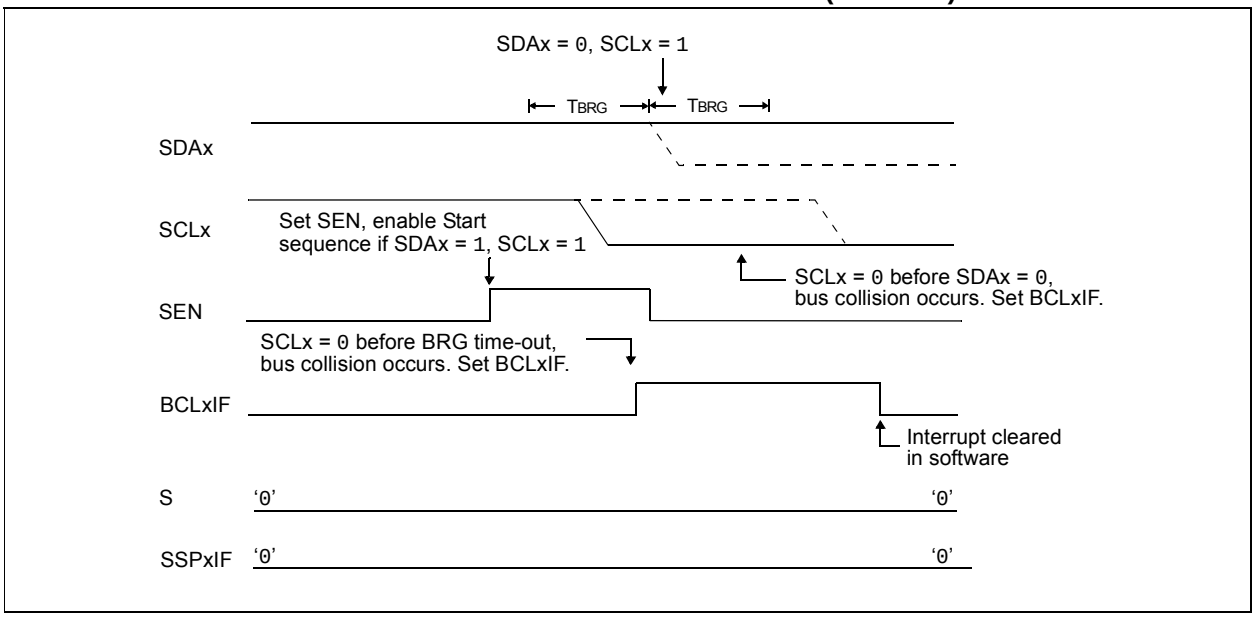
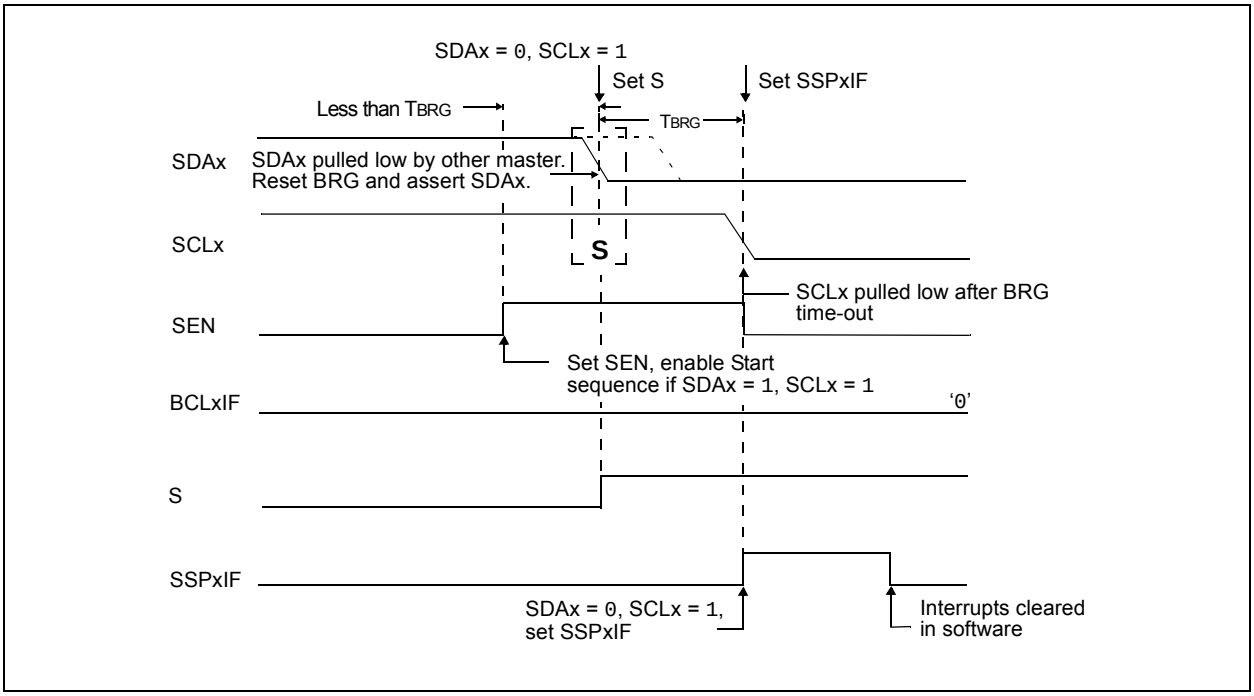


FIGURE 20-30: BRG RESET DUE TO SDAx ARBITRATION DURING START CONDITION



23.6 USB Power Modes

Many USB applications will likely have several different sets of power requirements and configuration. The most common power modes encountered are Bus Power Only, Self-Power Only and Dual Power with Self-Power Dominance. The most common cases are presented here. Also provided is a means of estimating the current consumption of the USB transceiver.

23.6.1 BUS POWER ONLY

In Bus Power Only mode, all power for the application is drawn from the USB (Figure 23-9). This is effectively the simplest power method for the device.

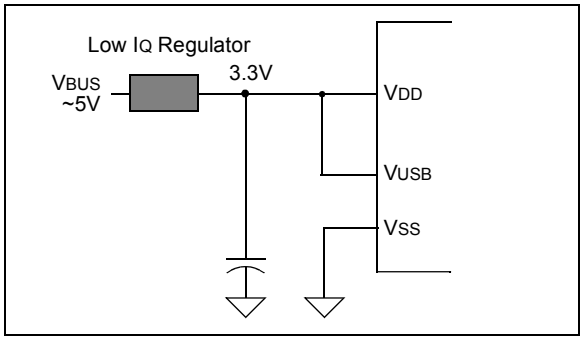
In order to meet the inrush current requirements of the USB 2.0 Specification, the total effective capacitance appearing across VBUS and ground must be no more than 10 µF. If not, some kind of inrush timing is required. For more details, see Section 7.2.4 of the USB 2.0 Specification.

According to the USB 2.0 Specification, all USB devices must also support a Low-Power Suspend mode. In the USB Suspend mode, devices must consume no more than 2.5 mA from the 5V VBUS line of the USB cable.

The host signals the USB device to enter the Suspend mode by stopping all USB traffic to that device for more than 3 ms. This condition will cause the IDLEIF bit in the UIR register to become set.

During the USB Suspend mode, the D+ or D- pull-up resistor must remain active, which will consume some of the allowed suspend current: 2.5 mA budget.

FIGURE 23-9: BUS POWER ONLY



23.6.2 SELF-POWER ONLY

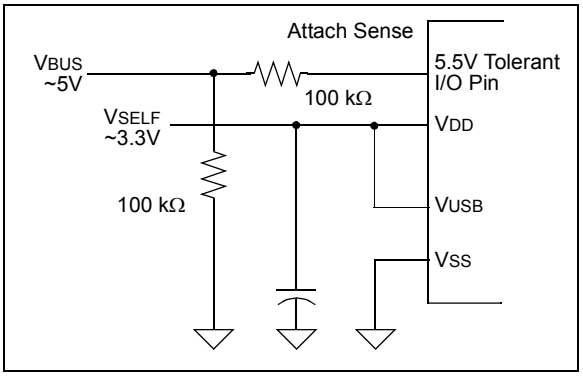
In Self-Power Only mode, the USB application provides its own power, with very little power being pulled from the USB. See Figure 23-10 for an example.

Note that an attach indication is added to indicate when the USB has been connected and the host is actively powering VBUS.

In order to meet compliance specifications, the USB module (and the D+ or D- pull-up resistor) should not be enabled until the host actively drives VBUS high. One of the 5.5V tolerant I/O pins may be used for this purpose.

The application should never source any current onto the 5V VBUS pin of the USB cable.

FIGURE 23-10: SELF-POWER ONLY

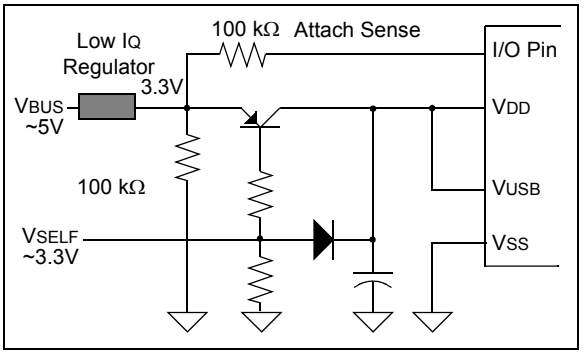


23.6.3 DUAL POWER WITH SELF-POWER DOMINANCE

Some applications may require a dual power option. This allows the application to use internal power primarily, but switch to power from the USB when no internal power is available. See Figure 23-11 for a simple Dual Power with Self-Power Dominance mode example, which automatically switches between Self-Power Only and USB Bus Power Only modes.

Dual power devices must also meet all of the special requirements for inrush current and Suspend mode current, and must not enable the USB module until VBUS is driven high. See **Section 23.6.1 "Bus Power Only"** and **Section 23.6.2 "Self-Power Only"** for descriptions of those requirements. Additionally, dual power devices must never source current onto the 5V VBUS pin of the USB cable.

FIGURE 23-11: DUAL POWER EXAMPLE



Note:	Users should keep in mind the limits for devices drawing power from the USB. According to USB Specification 2.0, this cannot exceed 100 mA per low-power device or 500 mA per high-power device.

REGISTER 28-11: WDTCON: WATCHDOG TIMER CONTROL REGISTER (ACCESS FC0h)

R/W-1	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
REGSLP	LVDSTAT(2)	ULPLVL	VBGOE	DS(2)	ULPEN	ULPSINK	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **REGSLP:** Voltage Regulator Low-Power Operation Enable bit
1 = On-chip regulator enters low-power operation when device enters Sleep mode
0 = On-chip regulator is active even in Sleep mode

bit 6 **LVDSTAT:** Low-Voltage Detect Status bit(2)
1 = V_{DDCORE} > 2.45V nominal
0 = V_{DDCORE} < 2.45V nominal

bit 5 **ULPLVL:** Ultra Low-Power Wake-up Output bit (not valid unless ULPEN = 1)
1 = Voltage on RA0 > ~0.5V
0 = Voltage on RA0 < ~0.5V

bit 4 **VBGOE**: Band Gap Reference Voltage (VBG) Output Enable bit
1 = Band gap reference output is enabled on pin RA1
0 = Band gap reference output is disabled

bit 3 **DS:** Deep Sleep Wake-up Status bit (used in conjunction with RCON, POR and BOR bits to determine Reset source)(2)
1 = If the last exit from Reset was caused by a normal wake-up from Deep Sleep
0 = If the last exit from Reset was not due to a wake-up from Deep Sleep

bit 2 **ULPEN:** Ultra Low-Power Wake-up Module Enable bit
1 = Ultra low-power wake-up module is enabled; ULPLVL bit indicates the comparator output
0 = Ultra low-power wake-up module is disabled

bit 1 **ULPSINK:** Ultra Low-Power Wake-up Current Sink Enable bit
1 = Ultra low-power wake-up current sink is enabled (if ULPEN = 1)
0 = Ultra low-power wake-up current sink is disabled

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit(1)
1 = Watchdog Timer is on
0 = Watchdog Timer is off

Note 1: This bit has no effect if the Configuration bit, WDTEN, is enabled.
2: Not available on devices where the on-chip voltage regulator is disabled ("LF" devices).

TABLE 28-3: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCON	IPEN	—	$\overline{CM}$	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
WDTCON	REGSLP	LVDSTAT	ULPLVL	VBGOE	DS	ULPEN	ULPSINK	SWDTEN

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Watchdog Timer.

GOTO **Unconditional Branch**

Syntax: GOTO k

Operands: $0 \le k \le 1048575$

Operation: $k \rightarrow PC<20:1>$

Status Affected: None

Encoding:

1st word (k<7:0>)	1110	1111	k_7kkk	$kkkk_0$
2nd word(k<19:8>)	1111	$k_{19}kkk$	kkkk	$kkkk_8$

Description: GOTO allows an unconditional branch anywhere within entire 2-Mbyte memory range. The 20-bit value 'k' is loaded into PC<20:1>. GOTO is always a 2-cycle instruction.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	No operation	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: GOTO THERE

After Instruction
PC = Address (THERE)

INCF **Increment f**

Syntax: INCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest

Status Affected: C, DC, N, OV, Z

Encoding:

0010	10da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: INCF CNT, 1, 0

Before Instruction
CNT = FFh
Z = 0
C = ?
DC = ?
After Instruction
CNT = 00h
Z = 1
C = 1
DC = 1

SUBWFB **Subtract W from f with Borrow**

Syntax: SUBWFB f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) – (W) – ($\overline{C}$) → dest

Status Affected: N, OV, C, DC, Z

Encoding:

0101	10da	ffff	ffff

Description: Subtract W and the Carry flag (borrow) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1:
```
SUBWFB  REG, 1, 0
Before Instruction
    REG  =  19h    (0001 1001)
    W    =  0Dh    (0000 1101)
    C    =  1
After Instruction
    REG  =  0Ch    (0000 1011)
    W    =  0Dh    (0000 1101)
    C    =  1
    Z    =  0
    N    =  0      ; result is positive
```

Example 2:
```
SUBWFB  REG, 0, 0
Before Instruction
    REG  =  1Bh    (0001 1011)
    W    =  1Ah    (0001 1010)
    C    =  0
After Instruction
    REG  =  1Bh    (0001 1011)
    W    =  00h
    C    =  1
    Z    =  1      ; result is zero
    N    =  0
```

Example 3:
```
SUBWFB  REG, 1, 0
Before Instruction
    REG  =  03h    (0000 0011)
    W    =  0Eh    (0000 1101)
    C    =  1
After Instruction
    REG  =  F5h    (1111 0100)
                   ; [2's comp]
    W    =  0Eh    (0000 1101)
    C    =  0
    Z    =  0
    N    =  1      ; result is negative
```

SWAPF **Swap f**

Syntax: SWAPF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f<3:0>) → dest<7:4>,
(f<7:4>) → dest<3:0>

Status Affected: None

Encoding:

0011	10da	ffff	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in register 'f' (default).

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example:
```
SWAPF   REG, 1, 0
Before Instruction
    REG  =  53h
After Instruction
    REG  =  35h
```

TABLE 31-7: USB MODULE SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D313	VUSB	USB Voltage	3.0	—	3.6	V	Voltage on VUSB pin must be in this range for proper USB operation
D314	IIL	Input Leakage on D+ or D-	—	—	±0.2	μA	VSS ≤ VPIN ≤ VUSB
D315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	For VUSB range
D316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	For VUSB range
D318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
D319	VCM	Differential Common Mode Range	0.8	—	2.5	V	
D320	ZOUT	Driver Output Impedance(1)	28	—	44	Ω	
D321	VOL	Voltage Output Low	0.0	—	0.3	V	1.5 kΩ load connected to 3.6V
D322	VOH	Voltage Output High	2.8	—	3.6	V	1.5 kΩ load connected to ground

Note 1: The D+ and D- signal lines have built-in impedance matching resistors. No external resistors, capacitors or magnetic components are necessary on the D+/D- signal paths between the PIC18F47J53 family device and a USB cable.

TABLE 31-27: MSSPx I²C BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			400 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	µs	
101	TLOW	Clock Low Time	100 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			400 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	µs	
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	µs	
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	µs	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	TBD	—	ns	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	TBD	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			400 kHz mode	2(TOSC)(BRG + 1)	—	µs	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	µs	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(1)	—	—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	TBD	—	µs	
D102	CB	Bus Capacitive Loading		—	400	pF	

Legend: TBD = To Be Determined

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

2: A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but parameter #107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, parameter #102 + parameter #107 = 1000 + 250 = 1250 ns (for 100 kHz mode), before the SCLx line is released.