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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.15V ~ 3.6V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f46j53t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-4: PIC18F4XJ53 PINOUT I/O DESCRIPTIONS (CONTINUED)

	Pin Number			Duffer	
Pin Name	44- QFN	44- TQFP	Ріп Туре	Buffer Type	Description
					PORTA is a bidirectional I/O port.
RA0/AN0/C1INA/ULPWU/PMA6/ RP0	19	19			
RAO			I/O	TTL/DIG	Digital I/O.
				Analog	Analog Input 0.
				Analog	Liltra low-power wake-up input
PMA6			I/O	ST/TTL/	Parallel Master Port digital I/O.
				DIG	
RP0			I/O	ST/DIG	Remappable Peripheral Pin 0 input/output.
RA1/AN1/C2INA/VBG/PMA7/RP1	20	20			
RA1			I/O	TTL/DIG	Digital I/O.
AN1			0	Analog	Analog Input 1.
C2INA				Analog	Comparator 2 Input A.
				Analog	Band Gap Reference Voltage (VBG) output.
			1/0	DIG	r araller Master i Ort digital 1/O.
RP1			I/O	ST/DIG	Remappable Peripheral Pin 1 input/output.
RA2/AN2/C2INB/C1IND/C3INB/	21	21			
VREF-/CVREF	- ·				
RA2			I/O	TTL/DIG	Digital I/O.
AN2			Ι	Analog	Analog Input 2.
C2INB				Analog	Comparator 2 Input B.
				Analog	Comparator 1 Input D.
VPEE-				Analog	A/D reference voltage (low) input
CVREF			i	Analog	Comparator reference voltage output.
	22	22		Ű	
RA3	~~	~~	I/O	TTL/DIG	Digital I/O.
AN3			I	Analog	Analog Input 3.
C1INB			Ι	Analog	Comparator 1 Input B.
VREF+			I	Analog	A/D reference voltage (high) input.
RA5/AN4/C1INC/SS1/HLVDIN/ RCV/RP2	24	24			
RA5			I/O	TTL/DIG	Digital I/O.
AN4			Ι	Analog	Analog Input 4.
C1INC				Analog	SPI slave select input.
				11L Angleg	Comparator 1 Input C.
RCV				TTI	External USB transceiver RCV input
RP2			I/O	ST/DIG	Remappable Peripheral Pin 2 input/output.
RA6 ⁽¹⁾					See the OSC2/CLKO/RA6 nin
RA7 ⁽¹⁾					See the OSC1/CLKI/RA7 pin.
Legend: TTL = TTL compatible in	nput		<u>.</u>		CMOS = CMOS compatible input or output
SI = Schmitt Trigger in	put wit	n CMO	Sievel	S	Analog = Analog Input
P = Power					OD = Open-Drain (no P diode to V)
DIG = Digital output					I^2C = Open-Drain, I^2C specific
Note 1: RA7 and RA6 will be disa	abled if	fOSC1	and O	SC2 are	used for the clock function.

2: Available only on 44-pin devices (PIC18F46J53, PIC18F47J53, PIC18LF46J53 and PIC18LF47J53).

3: 5.5V tolerant.

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 3.0 "Oscillator Configurations"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-4. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins and other signals in close proximity to the oscillator are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate website (www.microchip.com):

- AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC[™] and PICmicro[®] Devices
- AN849, Basic PICmicro[®] Oscillator Design
- AN943, Practical PICmicro[®] Oscillator Analysis and Design
- AN949, Making Your Oscillator Work

2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 k Ω to 10 k Ω resistor to Vss on unused pins and drive the output to logic low.

FIGURE 2-4: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT





FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



FIGURE 5-5: SLOW RISE TIME (MCLR TIED TO VDD, VDD RISE > TPWRT)



9.1 INTCON Registers

The INTCON registers are readable and writable registers, which contain various enable, priority and flag bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global interrupt enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 9-1: INTCON: INTERRUPT CONTROL REGISTER (ACCESS FF2h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INTOIF	RBIF ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	GIE/GIEH: Global Interrupt Enable bit
	When IPEN = 0:
	1 = Enables all unmasked interrupts
	0 = Disables all interrupts
	When IPEN = 1:
	1 = Enables all high-priority interrupts
bit 6	PEIE/GIEL: Peripheral Interrupt Enable bit
	$\frac{\text{When IPEN = 0}}{\text{IPEN = 0}}$
	1 = Enables all unmasked peripheral interrupts
	<u>$vviieiriPEN = 1$.</u> 1 = Enables all low-priority peripheral interrupts
	0 = Disables all low-priority peripheral interrupts
bit 5	TMR0IE: TMR0 Overflow Interrupt Enable bit
	1 = Enables the TMR0 overflow interrupt
	0 = Disables the TMR0 overflow interrupt
bit 4	INTOIE: INTO External Interrupt Enable bit
	1 = Enables the INT0 external interrupt
	0 = Disables the INT0 external interrupt
bit 3	RBIE: RB Port Change Interrupt Enable bit
	1 = Enables the RB port change interrupt
	0 = Disables the RB port change interrupt
bit 2	TMR0IF: TMR0 Overflow Interrupt Flag bit
	1 = The TMR0 register has overflowed (must be cleared in software)
	0 = The TMR0 register did not overflow
bit 1	INTOIF: INTO External Interrupt Flag bit
	1 = The INT0 external interrupt occurred (must be cleared in software)
	0 = The INT0 external interrupt did not occur
bit 0	RBIF: RB Port Change Interrupt Flag bit ⁽¹⁾
	1 = At least one of the RB<7:4> pins changed state (must be cleared in software)
	0 = None of the RB<7:4> pins have changed state

Note 1: A mismatch condition will continue to set this bit. Reading PORTB and waiting 1 Tcy will end the mismatch condition and allow the bit to be cleared.

10.7.6 PERIPHERAL PIN SELECT REGISTERS

The PIC18F47J53 family of devices implements a total of 37 registers for remappable peripheral configuration of 44-pin devices. The 28-pin devices have 31 registers for remappable peripheral configuration.

Note: Input and output register values can only be changed if IOLOCK (PPSCON<0>) = 0. See Example 10-7 for a specific command sequence.

REGISTER 10-5: PPSCON: PERIPHERAL PIN SELECT INPUT REGISTER 0 (BANKED PPSCON)⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—		—	—	—	—	IOLOCK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 Unimplemented: Read as '0'

- bit 0 IOLOCK: I/O Lock Enable bit
 - 1 = I/O lock is active, RPORx and RPINRx registers are write-protected
 0 = I/O lock is not active, pin configurations can be changed

Note 1: Register values can only be changed if IOLOCK (PPSCON<0>) = 0.

REGISTER 10-6: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1 (BANKED EE1h)

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INTR1R4	INTR1R3	INTR1R2	INTR1R1	INTR1R0
bit 7							bit 0

Legend:	R/W = Readable bit, Writab	le bit if IOLOCK = 0	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: Read as '0'

bit 4-0 **INTR1R<4:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits

REGISTER 10-7: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2 (BANKED EE2h)

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	INTR2R4	INTR2R3	INTR2R2	INTR2R1	INTR2R0
bit 7							bit 0

Legend:	R/\overline{W} = Readable bit, Writable bit if IOLOCK = 0		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: Read as '0'

bit 4-0 INTR2R<4:0>: Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits

11.2 Slave Port Modes

The primary mode of operation for the module is configured using the MODE<1:0> bits in the PMMODEH register. The setting affects whether the module acts as a slave or a master, and it determines the usage of the control pins.

11.2.1 LEGACY MODE (PSP)

In Legacy mode (PMMODEH<1:0> = 00 and PMPEN = 1), the module is configured as a Parallel Slave Port (PSP) with the associated enabled module

pins dedicated to the module. In this mode, an external device, such as another microcontroller or microprocessor, can asynchronously read and write data using the 8-bit data bus (PMD<7:0>), the read (PMRD), write (PMWR) and chip select (PMCS1) inputs. It acts as a slave on the bus and responds to the read/write-control signals.

Figure 11-2 displays the connection of the PSP. When chip select is active and a write strobe occurs (PMCSx = 1 and PMWR = 1), the data from PMD<7:0> is captured into the PMDIN1L register.

FIGURE 11-2: LEGACY PARALLEL SLAVE PORT EXAMPLE



12.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable. Its value is set by the PSA and T0PS<2:0> bits (T0CON<3:0>), which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When it is assigned, prescale values from 1:2 through 1:256, in power-of-2 increments, are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF TMR0, MOVWF TMR0, BSF TMR0, etc.) clear the prescaler count.

Note:	Writing to TMR0 when the prescaler is
	assigned to Timer0 will clear the prescaler
	count but will not change the prescaler
	assignment.

12.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed "on-the-fly" during program execution.

12.4 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit (INTCON<5>). Before re-enabling the interrupt, the TMR0IF bit must be cleared in software by the Interrupt Service Routine (ISR).

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

TABLE 12-1:	REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TMR0L	Timer0 Register Low Byte								
TMR0H	Timer0 Register High Byte								
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	
TOCON	TMR0ON	T08BIT	TOCS	T0SE	PSA	T0PS2	T0PS1	T0PS0	
			T ⁱ o						

Legend: Shaded cells are not used by Timer0.

20.4 SPI DMA MODULE

The SPI DMA module contains control logic to allow the MSSP2 module to perform SPI direct memory access transfers. This enables the module to quickly transmit or receive large amounts of data with relatively little CPU intervention. When the SPI DMA module is used, MSSP2 can directly read and write to general purpose SRAM. When the SPI DMA module is not enabled, MSSP2 functions normally, but without DMA capability.

The SPI DMA module is composed of control logic, a Destination Receive Address Pointer, a Transmit Source Address Pointer, an interrupt manager and a Byte Count register for setting the size of each DMA transfer. The DMA module may be used with all SPI Master and Slave modes, and supports both half-duplex and full-duplex transfers.

20.4.1 I/O PIN CONSIDERATIONS

When enabled, the SPI DMA module uses the MSSP2 module. All SPI input and output signals, related to MSSP2, are routed through the Peripheral Pin Select module. The appropriate initialization procedure, as described in **Section 20.4.6** "**Using the SPI DMA Module**", will need to be followed prior to using the SPI DMA module. The output pins assigned to the SDO2 and SCK2 functions can optionally be configured as open-drain outputs, such as for level shifting operations mentioned in the same section.

20.4.2 RAM TO RAM COPY OPERATIONS

Although the SPI DMA module is primarily intended to be used for SPI communication purposes, the module can also be used to perform RAM to RAM copy operations. To do this, configure the module for Full-Duplex Master mode operation, but assign the SDO2 output and SDI2 input functions onto the same RPn pin in the PPS module. Also assign SCK2 out and SCK2 in onto the same RPn pin (a different pin than used for SDO2 and SDI2). This will allow the module to operate in Loopback mode, providing RAM copy capability.

20.4.3 IDLE AND SLEEP CONSIDERATIONS

The SPI DMA module remains fully functional when the microcontroller is in Idle mode.

During normal Sleep, the SPI DMA module is not functional and should not be used. To avoid corrupting a transfer, user firmware should be careful to make certain that pending DMA operations are complete by polling the DMAEN bit in the DMACON1 register prior to putting the microcontroller into Sleep.

In SPI Slave modes, the MSSP2 module is capable of transmitting and/or receiving one byte of data while in Sleep mode. This allows the SSP2IF flag in the PIR3 register to be used as a wake-up source. When the DMAEN bit is cleared, the SPI DMA module is effectively disabled, and the MSSP2 module functions normally, but without DMA capabilities. If the DMAEN bit is clear prior to entering Sleep, it is still possible to use the SSP2IF as a wake-up source without any data loss.

Neither MSSP2 nor the SPI DMA module will provide any functionality in Deep Sleep. Upon exiting from Deep Sleep, all of the I/O pins, MSSP2 and SPI DMA related registers will need to be fully re-initialized before the SPI DMA module can be used again.

20.4.4 REGISTERS

The SPI DMA engine is enabled and controlled by the following Special Function Registers:

- DMACON1
 DMACON2
 - TXADDRL
- RXADDRH
- DMABCH

TXADDRH

RXADDRLDMABCL

20.5.3.4 7-Bit Address Masking Mode

Unlike 5-Bit Address Masking mode, 7-Bit Address Masking mode uses a mask of up to eight bits (in 10-bit addressing) to define a range of addresses than can be Acknowledged, using the lowest bits of the incoming address. This allows the module to Acknowledge up to 127 different addresses with 7-bit addressing, or 255 with 10-bit addressing (see Example 20-4). This mode is the default configuration of the module and is selected when MSSPMSK is unprogrammed ('1').

The address mask for 7-Bit Address Masking mode is stored in the SSPxMSK register, instead of the SSPx-CON2 register. SSPxMSK is a separate, hardware register within the module, but it is not directly addressable. Instead, it shares an address in the SFR space with the SSPxADD register. To access the SSPxMSK register, it is necessary to select MSSP mode, '1001' (SSPCON1<3:0> = 1001), and then read or write to the location of SSPxADD.

To use 7-Bit Address Masking mode, it is necessary to initialize SSPxMSK with a value before selecting the I^2C Slave Addressing mode. Thus, the required sequence of events is:

- 1. Select SSPxMSK Access mode (SSPx-CON2<3:0> = 1001).
- 2. Write the mask value to the appropriate SSPxADD register address (FC8h for MSSP1, F6Eh for MSSP2).
- Set the appropriate I²C Slave mode (SSPx-CON2<3:0> = 0111 for 10-bit addressing, 0110 for 7-bit addressing).

Setting or clearing mask bits in SSPxMSK behaves in the opposite manner of the ADMSK bits in 5-Bit Address Masking mode. That is, clearing a bit in SSPxMSK causes the corresponding address bit to be masked; setting the bit requires a match in that position. SSPxMSK resets to all '1's upon any Reset condition, and therefore, has no effect on the standard MSSP operation until written with a mask value.

With 7-Bit Address Masking mode, the SSPxMSK<7:1> bits mask the corresponding address bits in the SSPxADD register. For any SSPxMSK bits that are active (SSPxMSK<n> = 0), the corresponding SSPxADD address bit is ignored (SSPxADD<n> = x). For the module to issue an address Acknowledge, it is sufficient to match only on addresses that do not have an active address mask.

With 10-Bit Address Masking mode, SSPxMSK<7:0> bits mask the corresponding address bits in the SSPxADD register. For any SSPxMSK bits that are active (= 0), the corresponding SSPxADD address bit is ignored (SSPxADD<n> = x).

Note: The two MSbs of the address are not affected by address masking.

EXAMPLE 20-4: ADDRESS MASKING EXAMPLES IN 7-BIT MASKING MODE

7-Bit Addressing:

SSPxADD<7:1>= 1010 000

SSPxMSK<7:1>= 1111 001

Addresses Acknowledged = A8h, A6h, A4h, A0h

10-Bit Addressing:

SSPxADD<7:0> = 1010 0000 (the two MSbs are ignored in this example since they are not affected)

SSPxMSK<5:1> = 1111 0

Addresses Acknowledged = A8h, A6h, A4h, A0h

20.5.17.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDAx or SCLx is sampled low at the beginning of the Start condition (Figure 20-28).
- b) SCLx is sampled low before SDAx is asserted low (Figure 20-29).

During a Start condition, both the SDAx and the SCLx pins are monitored.

If the SDAx pin is already low, or the SCLx pin is already low, then all of the following occur:

- The Start condition is aborted
- · The BCLxIF flag is set
- The MSSP module is reset to its inactive state (Figure 20-28)

The Start condition begins with the SDAx and SCLx pins deasserted. When the SDAx pin is sampled high, the BRG is loaded from SSPxADD<6:0> and counts down to 0. If the SCLx pin is sampled low while SDAx is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDAx pin is sampled low during this count, the BRG is reset and the SDAx line is asserted early (Figure 20-30). If, however, a '1' is sampled on the SDAx pin, the SDAx pin is asserted low at the end of the BRG count. The BRG is then reloaded and counts down to 0. If the SCLx pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCLx pin is asserted low.

Note: The reason that a bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDAx before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.



FIGURE 20-28: BUS COLLISION DURING START CONDITION (SDAx ONLY)



FIGURE 21-5: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



TABLE 21-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 4 Bit 3		Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PMPIF ⁽¹⁾	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
PIE1	PMPIE ⁽¹⁾	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE
IPR1	PMPIP ⁽¹⁾	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CTMUIF	TMR3GIF	RTCCIF
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	TMR4IE CTMUIE		RTCCIE
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CTMUIP	TMR3GIP	RTCCIP
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
TXREGx	EUSARTx T	ransmit Regi	ster					
TXSTAx	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCONx	ABDOVF	RCIDL	RXDTP	XDTP TXCKP BRG16 — WU		WUE	ABDEN	
SPBRGHx	EUSARTx E	aud Rate Ge	nerator Regi	ster High By	te			
SPBRGx	EUSARTx E	aud Rate Ge	nerator Regi	ster Low Byt	е			
ODCON2		—	—	_	CCP10OD	CCP9OD	U2OD	U10D

Legend: - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: These bits are only available on 44-pin devices.



FIGURE 21-7: ASYNCHRONOUS RECEPTION

TABLE 21-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PMPIF ⁽¹⁾	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
PIE1	PMPIE ⁽¹⁾	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE
IPR1	PMPIP ⁽¹⁾	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CTMUIF	TMR3GIF	RTCCIF
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CTMUIE	TMR3GIE	RTCCIE
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CTMUIP	TMR3GIP	RTCCIP
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
RCREGx	EUSARTx R	Receive Regist	er					
TXSTAx	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCONx	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16		WUE	ABDEN
SPBRGHx	EUSARTx B	Baud Rate Ger	nerator High	Byte				
SPBRGx	EUSARTx B	Baud Rate Ger	erator Low I	Byte				

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: These bits are only available on 44-pin devices.

21.2.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the BRG is inactive and a proper byte reception cannot be performed. The auto-wake-up feature allows the controller to wake-up due to activity on the RXx/DTx line while the EUSART is operating in Asynchronous mode.

The auto-wake-up feature is enabled by setting the WUE bit (BAUDCONx<1>). Once set, the typical receive sequence on RXx/DTx is disabled and the EUSART remains in an Idle state, monitoring for a

wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RXx/DTx line. (This coincides with the start of a Sync Break or a Wake-up Signal character for the LIN/J2602 protocol.)

Following a wake-up event, the module generates an RCxIF interrupt. The interrupt is generated synchronously to the Q clocks in normal operating modes (Figure 21-8) and asynchronously if the device is in Sleep mode (Figure 21-9). The interrupt condition is cleared by reading the RCREGx register.

21.3 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTAx<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTAx<4>). In addition, enable bit, SPEN (RCSTAx<7>), is set in order to configure the TXx and RXx pins to CKx (clock) and DTx (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CKx line. Clock polarity is selected with the TXCKP bit (BAUDCONx<4>). Setting TXCKP sets the Idle state on CKx as high, while clearing the bit sets the Idle state as low. This option is provided to support Microwire devices with this module.

21.3.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 21-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The shift register obtains its data from the Read/Write Transmit Buffer register, TXREGx. The TXREGx register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREGx (if available).

Once the TXREGx register transfers the data to the TSR register (occurs in one TCY), the TXREGx is empty and the TXxIF flag bit is set. The interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXxIE. TXxIF is set regardless of the state of enable bit, TXxIE; it cannot be cleared in software. It will reset only when new data is loaded into the TXREGx register.

While flag bit, TXxIF, indicates the status of the TXREGx register, another bit, TRMT (TXSTAx<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user must poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

To set up a Synchronous Master Transmission:

- 1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the required baud rate.
- 2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
- 3. If interrupts are desired, set enable bit, TXxIE.
- 4. If 9-bit transmission is required, set bit, TX9.
- 5. Enable the transmission by setting bit, TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- 7. Start transmission by loading data to the TXREGx register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.



FIGURE 21-11: SYNCHRONOUS TRANSMISSION



FIGURE 21-12: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

TABLE 21-7:	REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION
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Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PMPIF ⁽¹⁾	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
PIE1	PMPIE ⁽¹⁾	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE
IPR1	PMPIP ⁽¹⁾	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CTMUIF	TMR3GIF	RTCCIF
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CTMUIE	TMR3GIE	RTCCIE
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CTMUIP	TMR3GIP	RTCCIP
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
TXREGx	EUSARTx T	ransmit Regis	ster					
TXSTAx	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
BAUDCONx	ABDOVF	RCIDL	RXDTP	TXCKP BRG16 — WUE				ABDEN
SPBRGHx	EUSARTx Baud Rate Generator High Byte							
SPBRGx	EUSARTx B	aud Rate Ge	nerator Low I	Byte				
ODCON2	—	_	_	_	CCP100D	CCP90D	U2OD	U10D

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

Note 1: These pins are only available on 44-pin devices.

24.5 Comparator Control and Configuration

Each comparator has up to eight possible combinations of inputs: up to four external analog inputs and one of two internal voltage references.

Both comparators allow a selection of the signal from pin, CxINA, or the voltage from the comparator reference (CVREF) on the non-inverting channel. This is compared to either CxINB, CxINC, CxIND, CTMU or the microcontroller's fixed internal reference voltage (VIRV, 0.6V nominal) on the inverting channel.

Table 24-1 provides the comparator inputs and outputs tied to fixed I/O pins.

Comparator	Input or Output	I/O Pin
	C1INA (VIN+)	RA0
	C1INB (VIN-)	RA3
1	C1INC (VIN-)	RA5
	C1IND (VIN-)	RA2
	C1OUT	Remapped RPn
	C2INA(VIN+)	RA1
	C2INB(VIN-)	RA2
2	C2INC (VIN-)	RB2
2	C2IND (VIN-)	RC2
	C2OUT	Remapped RPn
	C3INA(VIN+)	RB3
	C3INB(VIN-)	RA2
3	C3INC (VIN-)	RB1
J	C3IND (VIN-)	RB0
	C3OUT	Remapped RPn

TABLE 24-1: COMPARATOR INPUTS AND OUTPUTS

24.5.1 COMPARATOR ENABLE AND INPUT SELECTION

Setting the CON bit of the CMxCON register (CMxCON<7>) enables the comparator for operation. Clearing the CON bit disables the comparator, minimizing current consumption.

The CCH<1:0> bits in the CMxCON register (CMxCON<1:0>) direct either one of three analog input pins, or the Internal Reference Voltage (VIRV), to the comparator, VIN-. Depending on the comparator operating mode, either an external or internal voltage reference may be used. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly.

The external reference is used when CREF = 0 (CMxCON<2>) and VIN+ is connected to the CxINA pin. When external voltage references are used, the comparator module can be configured to have the reference sources externally. The reference signal must be between VSS and VDD, and can be applied to either pin of the comparator.

The comparator module also allows the selection of an internally generated voltage reference (CVREF) from the comparator voltage reference module. This module is described in more detail in **Section 24.0 "Comparator Module"**. The reference from the comparator voltage reference module is only available when CREF = 1. In this mode, the internal voltage reference is applied to the comparator's VIN+ pin.

Note:	The comparator input pin selected by								
	CCH<1:0> must be configured as an input								
	by setting both the corresponding TRIS bits								
	and PCFG bits in the ANCON1 register.								

24.5.2 COMPARATOR ENABLE AND OUTPUT SELECTION

The comparator outputs are read through the CMSTAT register. The CMSTAT<0> reads the Comparator 1 output, CMSTAT<1> reads the Comparator 2 output and CMSTAT<2> reads the Comparator 3 output. These bits are read-only.

The comparator outputs may also be directly output to the RPn I/O pins by setting the COE bit (CMxCON<6>). When enabled, multiplexers in the output path of the pins switch to the output of the comparator.

By default, the comparator's output is at logic high whenever the voltage on VIN+ is greater than on VIN-. The polarity of the comparator outputs can be inverted using the CPOL bit (CMxCON<5>).

The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications, as discussed in **Section 24.2 "Comparator Operation"**.





Clock failure is tested for on the falling edge of the sample clock. If a sample clock falling edge occurs while the clock monitor is still set, and a clock failure has been detected (Figure 28-5), the following results:

- The FSCM generates an oscillator fail interrupt by setting bit, OSCFIF (PIR2<7>);
- The device clock source is switched to the internal oscillator block (OSCCON is not updated to show the current clock source this is the Fail-safe condition); and
- · The WDT is reset.

During switchover, the postscaler frequency from the internal oscillator block may not be sufficiently stable for timing-sensitive applications. In these cases, it may be desirable to select another clock configuration and enter an alternate power-managed mode. This can be done to attempt a partial recovery or execute a controlled shutdown. See Section 4.1.4 "Multiple Sleep Commands" and Section 28.4.1 "Special Considerations For Using Two-speed Start-up" for more details.

The FSCM will detect failures of the primary or secondary clock sources only. If the internal oscillator block fails, no failure would be detected, nor would any action be possible.

28.5.1 FSCM AND THE WATCHDOG TIMER

Both the FSCM and the WDT are clocked by the INTRC oscillator. Since the WDT operates with a separate divider and counter, disabling the WDT has no effect on the operation of the INTRC oscillator when the FSCM is enabled.

As already noted, the clock source is switched to the INTRC clock when a clock failure is detected; this may mean a substantial change in the speed of code execution. If the WDT is enabled with a small prescale value, a decrease in clock speed allows a WDT time-out to occur and a subsequent device Reset. For this reason, Fail-Safe Clock Monitor events also reset the WDT and postscaler, allowing it to start timing from when execution speed was changed and decreasing the likelihood of an erroneous time-out.



FIGURE 28-5: FSCM TIMING DIAGRAM

WFC	ADD W an	d Carry bit t	o f	Α				
ix:	ADDWFC	f {,d {,a}}		S				
ands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$			0				
ation:	(W) + (f) +	$(C) \rightarrow dest$		Si				
s Affected:	N,OV, C, D	C, Z		E				
ding:	0010	00da fi	ff ffff	ט ך				
ription:	Add W, the location 'f'. placed in W placed in d	Carry flag an If 'd' is '0', th /. If 'd' is '1', ata memory l	d data memory e result is the result is ocation 'f'.	- - - - - - - - - - - - - - - - - - -				
	lf 'a' is '0', t If 'a' is '1', t GPR bank	If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).						
	If 'a' is '0' a set is enabl in Indexed mode wher Section 29 Bit-Oriente Literal Offs	If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for dotaile						
s:	1							
s:	1							
cle Activity:								
Q1	Q2	Q3	Q4	_				
Decode	Read register 'f'	Process Data	Write to destination					
iple:	ADDWFC	REG, 0,	1					
Before Instruc Carry bit REG W After Instructic Carry bit REG W	tion = 1 = 02h = 4Dh on = 0 = 02h = 50h							
	NFC IX: ands: ation: s Affected: ding: ription: ription: s: ycle Activity: Q1 Decode pele: Before Instruct Carry bit REG W After Instruction Carry bit REG W	WFCADD W and ADDWFCands: $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ ation: $(W) + (f) +$ s Affected:N,OV, C, Dding: 0010 ription:Add W, the location 'f'. placed in W placed in d If 'a' is '0', t If 'a' is '0', t GPR bankIf 'a' is '0', t If 'a' is '0' a set is enable in Indexed mode wher Section 29 Bit-Oriente Literal Offss:1s:1ycle Activity: Q1Q2DecodeRead register 'f'ple:ADDWFCBefore Instruction Carry bit = 1 REG = 02h W = 4DhAfter Instruction Carry bit = 0 REG = 02h W = 50h	WFCADD W and Carry bit toands: $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ ation: $(W) + (f) + (C) \rightarrow dest$ s Affected:N,OV, C, DC, Zding: 0010 $00da$ fription:Add W, the Carry flag an location 'f'. If 'd' is '0', th placed in data memory I If 'a' is '0', the Access Ba If 'a' is '0', the Access Ba If 'a' is '0' and the extenset is enabled, this instru- in Indexed Literal Offset mode whenever $f \le 95$ (section 29.2.3 "Byte-O Bit-Oriented Instruction Literal Offset Mode" for ss:ss:1ycle Activity:Q2Q3Q1Q2Q3DecodeRead register 'f'Datample:ADDWFCREGadDWFCREG0,Before Instruction Carry bit = 1 REG = 02h W = 4DhAfter Instruction Carry bit = 0 REG = 02h W = 50h	NFC ADD W and Carry bit to fix:ADDWFC $f \{.d \{.a\}\}$ ands: $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ ation: $(W) + (f) + (C) \rightarrow dest$ s Affected:N,OV, C, DC, Zding: 0010 $00da$ ffffffffription:Add W, the Carry flag and data memorylocation 'f. If 'd' is '0', the result isplaced in W. If 'd' is '1', the result isplaced in data memory location 'f'.If 'a' is '0', the Access Bank is selected.If 'a' is '0' and the extended instructionset is enabled, this instruction operatesin Indexed Literal Offset Addressingmode whenever $f \le 95$ (5Fh). SeeSection 29.2.3 "Byte-Oriented andBit-Oriented Instructions in IndexedLiteral Offset Mode" for details.s:1s:1s:1gle codeReadregister 'f'DataDecodeReadregister 'f'DatadestinationCarry bit = 1REG = 02hW = 4DhAfter InstructionCarry bit = 0REG = 02hW = 4DhW = 4Dh				

ANDLW	AND Litera	AND Literal with W					
Syntax:	ANDLW	k					
Operands:	$0 \le k \le 255$						
Operation:	(W) .AND.	$k \rightarrow W$					
Status Affected:	N, Z						
Encoding:	0000	1011	kkkk	kkkk			
Description:	The conten 8-bit literal	ts of W a 'k'. The r	re ANDec esult is pla	I with the aced in W			
Words:	1						
Cycles:	1						
Q Cycle Activity:							
Q1	Q2	Q3	1	Q4			
Decode	Read literal 'k'	Proce Data	ss V a	Vrite to W			
Example:	ANDLW	05Fh					
Before Instruc W After Instructic	tion = A3h on						

31.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any digital only I/O pin or MCLR with respect to Vss (except VDD)	-0.3V to 6.0V
Voltage on any combined digital and analog pin with respect to Vss (except VDD)	0.3V to (VDD + 0.3V)
Voltage on VDDCORE with respect to Vss	0.3V to 2.75V
Voltage on VDD with respect to Vss	-0.3V to 4.0V
Voltage on VUSB with respect to VSS	(VDD – 0.3V) to 4.0V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	
Maximum current into VDD pin	
Maximum output current sunk by any PORTB, PORTC and RA6 I/O pin	25 mA
Maximum output current sunk by any PORTA (except RA6), PORTD and PORTE I/O pin	8 mA
Maximum output current sourced by any PORTB, PORTC and RA6 I/O pin	25 mA
Maximum output current sourced by any PORTA (except RA6), PORTD and PORTE I/O pin	8 mA
Maximum current sunk by all ports	
Maximum current sourced by all ports	
Note 1: Power dissipation is calculated as follows: $PDIS = VDD x \{IDD - \sum IOH\} + \sum \{(VDD - VOH) x IOH\} + \sum (VOL x IOL)$	

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F47J53 Family (Industrial) (Continued)

PIC18LF	47J53 Family	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$								
PIC18F4	7J53 Family	Standa Operat	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial							
Param. No.	Device	Тур.	Max.	Units	s Conditions					
	PIC18LFXXJ53	6.9	11.0	mA	-40°C					
		6.7	11.0	mA	+25°C	VDD = 2.5V, $VDDCORE = 2.5V$	Fosc = 24 MHz PRI_RUN mode, ECPLL Oscillator			
		6.4	10.0	mA	+85°C	VDDCORE - 2.5V				
	PIC18FXXJ53	7.0	15.0	mA	-40°C	VDD = 3.3V,				
		6.8	14.0	mA	+25°C	VDDCORE = 10 μ F	(4 MHz Input)			
		6.6	14.0	mA	+85°C	Capacitor				
	PIC18LFXXJ53	9.9	14.0	mA	-40°C					
		9.7	14.0	mA	+25°C	VDD = 2.5V, $VDDCOPE = 2.5V$	$F_{OSC} = 48 \text{ MHz}$			
		9.5	14.0	mA	+85°C	VDDCORE - 2.3V	PRI_RUN mode,			
	PIC18FXXJ53	10.3	21.5	mA	-40°C	VDD = 3.3V,	ECPLL Oscillator			
		10.0	20.5	mA	+25°C	VDDCORE = 10 µF	(4 MHz Input)			
		9.7	20.5	mA	+85°C	Capacitor				

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption. All features that add delta current are disabled (USB module, WDT, etc.). The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD/VSS;

MCLR = VDD; WDT disabled unless otherwise specified.

- **3:** Low-power Timer1 with standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
- 4: This is the module differential current when the USB module is enabled and clocked at 48 MHz, but with no USB cable attached. When the USB cable is attached or data is being transmitted, the current consumption may be much higher (see Section 23.6.4 "USB Transceiver Current Consumption"). During USB Suspend mode (USBEN = 1, SUSPND = 1, bus in Idle state), the USB module current will be dominated by the D+ or D- pull-up resistor. The integrated pull-up resistor use "resistor switching" according to the resistor_ecn supplement to the USB 2.0 Specifications, and therefore, may be as low as 900Ω during Idle conditions.

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param. No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Comments
D313	VUSB	USB Voltage	3.0	—	3.6	V	Voltage on VUSB pin must be in this range for proper USB operation
D314	lı∟	Input Leakage on D+ or D-	_	_	<u>+</u> 0.2	μA	Vss <u><</u> Vpin <u><</u> Vusb
D315	VILUSB	Input Low Voltage for USB Buffer	-	_	0.8	V	For VUSB range
D316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	For VUSB range
D318	VDIFS	Differential Input Sensitivity	_	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
D319	Vсм	Differential Common Mode Range	0.8	—	2.5	V	
D320	Zout	Driver Output Impedance ⁽¹⁾	28	—	44	Ω	
D321	Vol	Voltage Output Low	0.0	-	0.3	V	1.5 k Ω load connected to 3.6V
D322	Vон	Voltage Output High	2.8	—	3.6	V	1.5 k Ω load connected to ground

TABLE 31-7: USB MODULE SPECIFICATIONS

Note 1: The D+ and D- signal lines have built-in impedance matching resistors. No external resistors, capacitors or magnetic components are necessary on the D+/D- signal paths between the PIC18F47J53 family device and a USB cable.