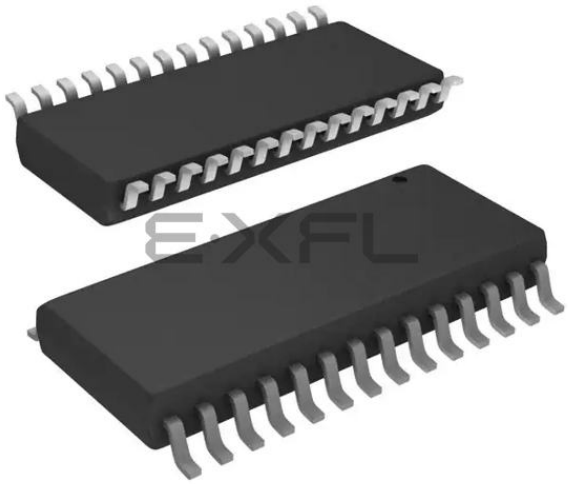

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 128KB (64K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3.8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 2.75V |
| Data Converters | A/D 10x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18lf27j53-i-so |

TABLE 1-3: PIC18F2XJ53 PINOUT I/O DESCRIPTIONS (CONTINUED)

| Pin Name | Pin Number | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|
| | 28-SPDIP/ SSOP/ SOIC | 28-QFN | | | |
| $V_{SS}1$ | 8 | 5 | P | — | Ground reference for logic and I/O pins. |
| $V_{SS}2$ | 19 | 16 | — | — | |
| $V_{DD}$ | 20 | 17 | P | — | Positive supply for peripheral digital logic and I/O pins. |
| $V_{DDCORE}/V_{CAP}$ | 6 | 3 | — | — | Core logic power or external filter capacitor connection. |
| $V_{DDCORE}$ | | | P | — | Positive supply for microcontroller core logic (regulator disabled). |
| $V_{CAP}$ | | | P | — | External filter capacitor connection (regulator enabled). |
| $V_{USB}$ | 14 | 11 | P | — | USB voltage input pin. |

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to $V_{DD}$); DIG = Digital output; $I^2C$ = Open-Drain, $I^2C$ specific

Note 1: RA7 and RA6 will be disabled if OSC1 and OSC2 are used for the clock function.

2: 5.5V tolerant.

FIGURE 4-7: TRANSITION TIMING FOR ENTRY TO IDLE MODE

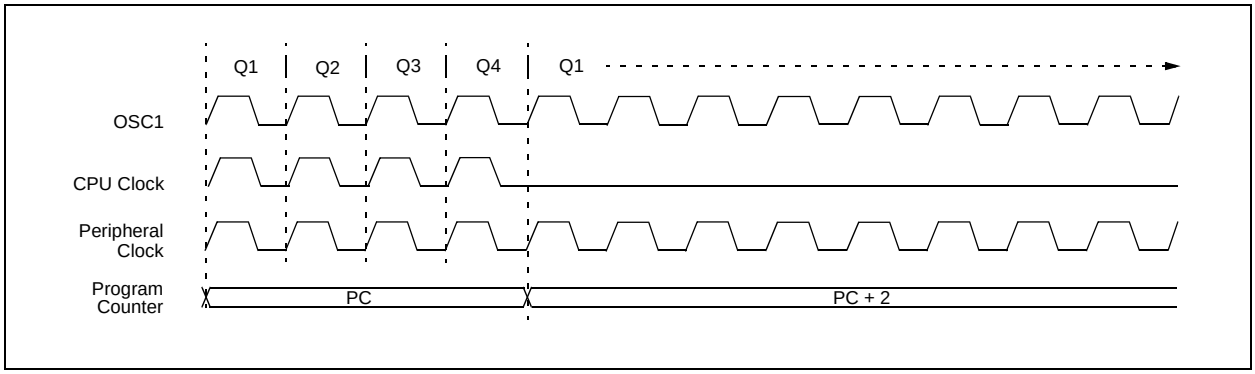


FIGURE 4-8: TRANSITION TIMING FOR WAKE FROM IDLE TO RUN MODE

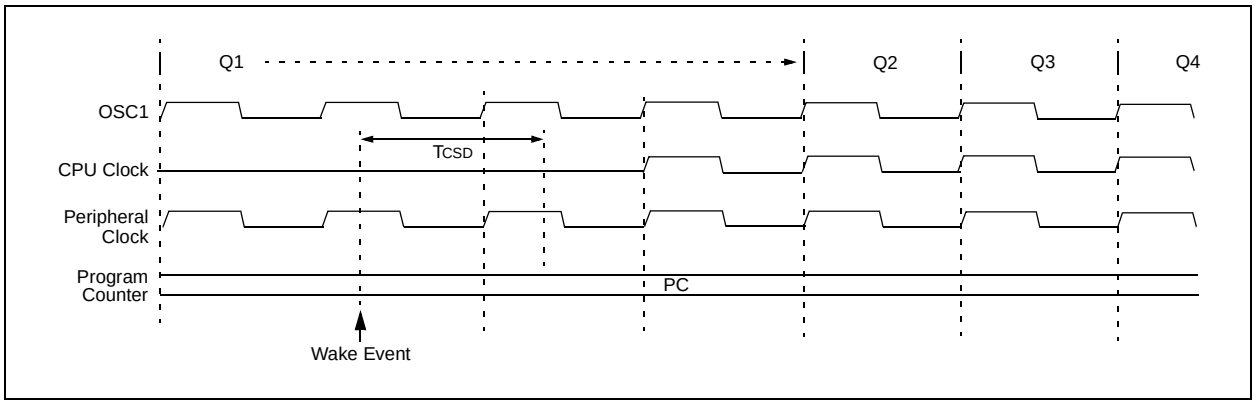

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

| Register | Applicable Devices | | Power-on Reset, Brown-out Reset, Wake From Deep Sleep | $\overline{\text{MCLR}}$ Resets WDT Reset RESETInstruction Stack Resets CM Resets | Wake-up via WDT or Interrupt |
|---|---|---|---|---|---|
| IPR1 | PIC18F2XJ53 | PIC18F4XJ53 | 1111 1111 | 1111 1111 | uuuu uuuu |
| PIR1 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu (3) |
| PIE1 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| RCSTA2 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 000x | 0000 000x | uuuu uuuu |
| OSCTUNE | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| T1GCON | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0x00 | 0000 0x00 | uuuu uuuu |
| T3GCON | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0x00 | uuuu uxuu | uuuu uxuu |
| TRISE(5) | PIC18F2XJ53 | PIC18F4XJ53 | 00-- -111 | uu-- -111 | uu-- -uuu |
| TRISD(5) | PIC18F2XJ53 | PIC18F4XJ53 | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISC | PIC18F2XJ53 | PIC18F4XJ53 | 11-- -111 | 11-- -111 | uu-- -uuu |
| TRISB | PIC18F2XJ53 | PIC18F4XJ53 | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISA | PIC18F2XJ53 | PIC18F4XJ53 | 111- 1111 | 111- 1111 | uuu- uuuu |
| LATE(5) | PIC18F2XJ53 | PIC18F4XJ53 | ---- -xxx | ---- -uuu | ---- -uuu |
| LATD(5) | PIC18F2XJ53 | PIC18F4XJ53 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| LATC | PIC18F2XJ53 | PIC18F4XJ53 | xx-- -xxx | uu-- -uuu | uu-- -uuu |
| LATB | PIC18F2XJ53 | PIC18F4XJ53 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| LATA | PIC18F2XJ53 | PIC18F4XJ53 | xxx- xxxx | uuu- uuuu | uuu- uuuu |
| DMACON1 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| OSCCON2 | PIC18F2XJ53 | PIC18F4XJ53 | -0-1 01-- | — | — |
| DMACON2 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| HLVDCON | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| PORTE(5) | PIC18F2XJ53 | PIC18F4XJ53 | ---- -xxx | ---- -uuu | ---- -uuu |
| PORTD(5) | PIC18F2XJ53 | PIC18F4XJ53 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTC | PIC18F2XJ53 | PIC18F4XJ53 | xxxx -xxx | uuuu -uuu | uuuu -uuu |
| PORTB | PIC18F2XJ53 | PIC18F4XJ53 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTA | PIC18F2XJ53 | PIC18F4XJ53 | xxx- xxxx | uuu- uuuu | uuu- uuuu |
| SPBRGH1 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| BAUDCON1 | PIC18F2XJ53 | PIC18F4XJ53 | 0100 0-00 | 0100 0-00 | uuuu u-uu |
| SPBRGH2 | PIC18F2XJ53 | PIC18F4XJ53 | 0000 0000 | 0000 0000 | uuuu uuuu |
| BAUDCON2 | PIC18F2XJ53 | PIC18F4XJ53 | 0100 0-00 | 0100 0-00 | uuuu u-uu |

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for Reset value for specific condition.

5: Not implemented for PIC18F2XJ53 devices.

6: Not implemented for "LF" devices.

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