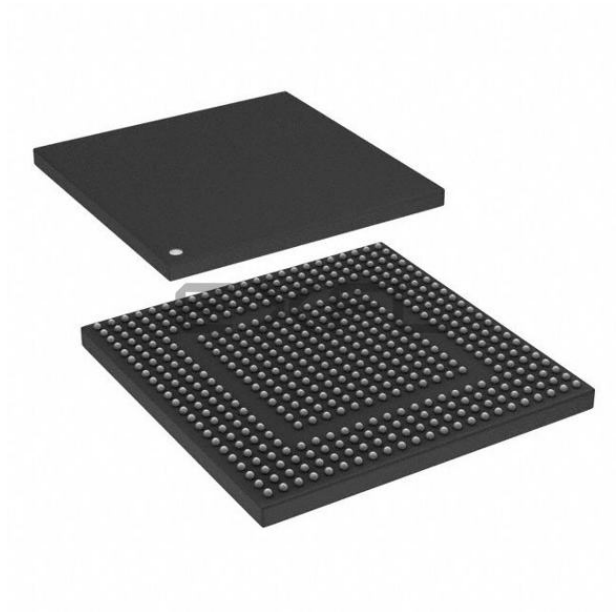

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673kff0mms1r

1.3 Device comparison

Table 1. MPC5675K family device comparison

Features		MPC5673K	MPC5674K	MPC5675K
CPU	Type	2 × e200z7d (SoR[1]) in lock-step or decoupled operation		
	Architecture	Harvard		
	Execution speed	0–150 MHz (+2% FM)	0–180 MHz (+2% FM)	0–180 MHz (+2% FM)
	Nominal platform frequency (in 1:1, 1:2, and 1:3 modes)	0–75 MHz (+2% FM)	0–90 MHz (+2% FM)	0–90 MHz (+2% FM)
	MMU	64 entries (SoR)		
	Instruction set PPC	Yes		
	Instruction set VLE	Yes		
	Instruction cache	16 KB, 4-way with EDC (SoR)		
	Data cache	16 KB, 4-way with Parity (SoR)		
	MPU	Yes (SoR)		
Buses	Core bus	32-bit address, 64-bit data		
	Internal periphery bus	32-bit address, 32-bit data		
XBAR	Master × slave ports	Yes (SoR)		
Memory	Static RAM (SRAM)	256 KB (ECC)	384 KB (ECC)	512 KB (ECC)
	Code flash memory	1 MB[2]	1.5 MB[2]	2 MB[2]
	Data flash memory	64 KB[2]		
Modules	Analog-to-Digital Converter (ADC)	257 pin pkg: 4 × 12 bit (22 external channels) 473 pin pkg: 4 × 12 bit (up to 34 external channels)		
	CRC unit	2 (3 contexts each)		
	Cross Triggering Unit (CTU)	2 modules		
	Deserial Serial Peripheral Interface (DSPI)	2 modules (3 chip selects)[3]	3 modules[4]	
	Digital I/Os	≥ 16		
	DRAM Controller (DRAMC)	No	Yes[5]	
	Enhanced Direct Memory Access (eDMA)	2 modules, 32 channels each		
	eTimer	3 modules, 6 channels each		

Table 1. MPC5675K family device comparison (continued)

Features		MPC5673K	MPC5674K	MPC5675K
Packages	MAPBGA	257 pins 473 pins		
Temperature	Ambient	See the T_A recommended operating condition in the device data sheet		

1 Sphere of Replication.

2 Does not include Test or Shadow Flash memory space.

3 DSPI_0 and DSPI_1.

4 DSPI_0 has 8 chip selects; DSPI_1 and DSPI_2 have 4 chip selects each.

5 Available only on 473-pin package.

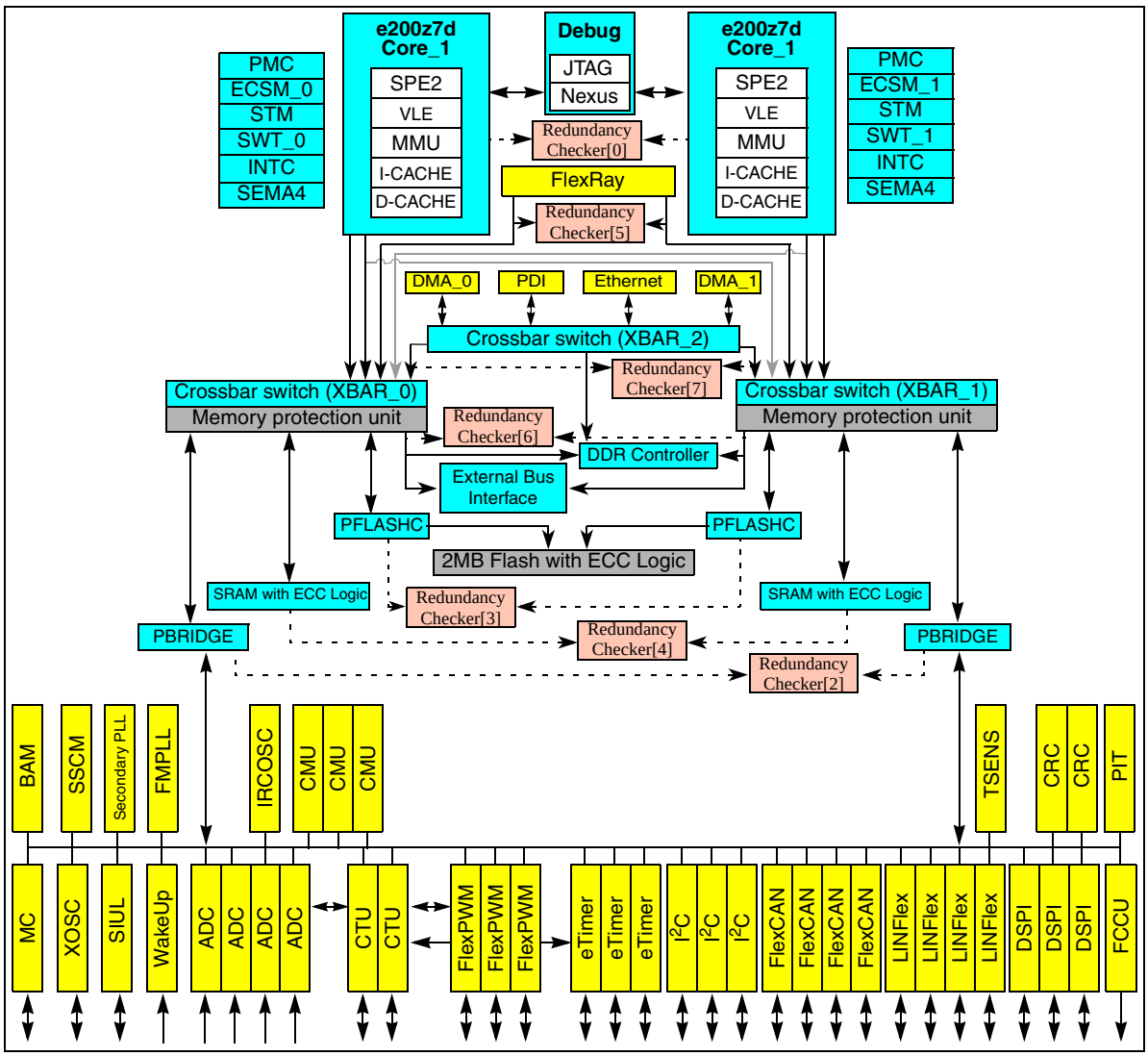
6 I2C_0 and I2C_1.

7 LinFlex_0, LinFlex_1, and LinFlex_2.

8 DDR available only on 473 package. Other modules available as follows:
EBI or DDR on 473 package
EBI + PDI on 473 package
DDR + PDI on 473 package
PDI only on 257 package

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5675K device.



ADC – Analog-to-digital converter
BAM – Boot assist module
CMU – Clock monitoring unit
CRC – Cyclic redundancy check unit
CTU – Cross triggering unit
DSPI – Deserial serial peripheral interface
EBI – External bus interface
ECC – Error correction code
ECSM – Error correction status module
eDMA – Enhanced direct memory access controller
FCCU – Fault collection and control unit
FEC – Fast Ethernet controller
FlexCAN – Controller area network controller
FlexPWM – Pulse width modulator module
FMPLL – Frequency-modulated phase-locked loop
I2C – Inter-integrated circuit controller
INTC – Interrupt controller
IRCOSC – Internal RC oscillator
JTAG – Joint Test Action Group interface
MC – Mode entry, clock, reset, and power modules
mDDR – Mobile double data rate dynamic RAM
PBRIDGE – Peripheral bridge
PDI – Parallel data interface
PIT – Periodic interrupt timer
PMC – Power management controller
RC – Redundancy checker
RTC – Real time clock
SEMA4 – Semaphore unit
SIUL – System integration unit Lite
SSCM – System status and configuration module
STM – System timer module
SWT – Software watchdog timer
TSENS – Temperature sensor
XOSC – Crystal oscillator

Figure 1. MPC5675K block diagram

1.5 Feature list

- High-performance e200z7d dual core
  - 32-bit Power Architecture® technology CPU
  - Up to 180 MHz core frequency
  - Dual-issue core
  - Variable length encoding (VLE)
  - Memory management unit (MMU) with 64 entries
  - 16 KB instruction cache and 16 KB data cache
- Memory available
  - Up to 2 MB code flash memory with ECC
  - 64 KB data flash memory with ECC
  - Up to 512 KB on-chip SRAM with ECC
- SIL3/ASILD innovative safety concept: LockStep mode and fail-safe protection
  - Sphere of replication (SoR) for key components
  - Redundancy checking units on outputs of the SoR connected to FCCU
  - Fault collection and control unit (FCCU)
  - Boot-time built-in self-test for memory (MBIST) and logic (LBIST) triggered by hardware
  - Boot-time built-in self-test for ADC and flash memory
  - Replicated safety-enhanced watchdog timer
  - Silicon substrate (die) temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) units
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority interrupt controller
- GPIOs individually programmable as input, output, or special function
- 3 general-purpose eTimer units (6 channels each)
- 3 FlexPWM units with four 16-bit channels per module
- Communications interfaces
  - 4 LINFlex modules
  - 3 DSPI modules with automatic chip select generation
  - 4 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1) with dual channel, up to 128 message objects and up to 10 Mbit/s
  - Fast Ethernet Controller (FEC)
  - 3 I^2C modules
- Four 12-bit analog-to-digital converters (ADCs)
  - 22 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADC conversion with timer and PWM
- External bus interface
- 16-bit external DDR memory controller
- Parallel digital interface (PDI)

1.6.7 External Bus Interface (EBI)

- Available on 473-pin devices
- Data and address options:
  - 16-bit data and address (non-muxed)
  - 32-bit data and address (bus-muxed)
- MPC5561 324 BGA compatibility mode: 16-bit data bus, 24-bit address bus is default ADDR[8:31], but configurable to 26-bit address bus
- Memory controller with support for various memory types
  - Non-burst and burst mode SDR flash and SRAM
  - Asynchronous/legacy flash and SRAM
- Configurable bus speed modes
- Support for 2 MB address space
- Chip select and write/byte enable options as presented in the pin-muxing table in the “Signal Description” chapter of
- the MPC5675K reference manual
- Configurable wait states (via chip selects)
- Optional automatic CLKOUT gating to save power and reduce EMI

1.6.8 On-chip flash memory

- Up to 2 MB code flash memory with ECC
- 64 KB data flash memory with ECC
- Censorship protection scheme to prevent flash content visibility
- Multiple block sizes to support features such as boot block, operating system block, and EEPROM emulation
- Read-while-write with multiple partitions
- Parallel programming mode to support rapid end-of-line programming
- Hardware programming state machine

1.6.9 Cache memory

- Harvard architecture cache
- 16 KB instruction / 16 KB data
- Four-way set-associative Harvard (instruction and data) 256-bit long cache
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data cache parity
  - Supports EDC for instruction cache

1.6.10 On-chip internal static RAM (SRAM)

- Up to 512 KB general-purpose SRAM
- ECC performs single-bit correction, double-bit error detection
  - Address included in ECC checkbase

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
J17	GPIO	flexpwm0 X[1]	A0: siul_GPIO[195] A1: flexpwm0_X[1] A2: ebi_AD29 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K1	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K2	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K3	GPIO	nexus RDY_B	A0: siul_GPIO[216] A1: _ A2: nexus_RDY_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K4	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
K14	GPIO	flexpwm0 X[2]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_AD30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K15	GPIO	flexpwm0 X[3]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_AD31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K16	GPIO	flexpwm0 A[1]	A0: siul_GPIO[149] A1: _ A2: ebi_RD_WR A3: flexpwm0_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K17	GPIO	flexpwm0 B[0]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
P6	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P7	ANA	adc0 AN[0]	—	siul_GPI[23] lin0_RXD	AN: adc0_AN[0]		Analog	VDD_HV_ADR02
P8	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
P11	ANA	adc0_adc1 AN[14]	—	siul_GPI[28]	AN: adc0_adc1_AN[14]		Analog Shared	VDD_HV_ADR02
P12	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
P13	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
P15	GPIO	flexpwm0 A[3]	A0: siul_GPIO[153] A1: dramc_WEB A2: ebi_WE_BE_2 A3: flexpwm0_A[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P16	GPIO	flexpwm0 A[0]	A0: siul_GPIO[147] A1: dramc_CKE A2: ebi_OE A3: flexpwm0_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P17	GPIO	flexpwm1 B[1]	A0: siul_GPIO[163] A1: dramc_ADD[5] A2: ebi_ADD13 A3: flexpwm1_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
A4	GPIO	nexus MDO[5][1]	A0: siul_GPIO[114] A1: _ A2: npc_wrapper_MDO[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A5	GPIO	nexus MDO[7][1]	A0: siul_GPIO[112] A1: _ A2: npc_wrapper_MDO[7] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A6	GPIO	nexus MDO[9][1]	A0: siul_GPIO[110] A1: _ A2: npc_wrapper_MDO[9] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A7	GPIO	flexray CB_TX	A0: siul_GPIO[51] A1: flexray_CB_TX A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A8	GPIO	flexray CA_TR_EN	A0: siul_GPIO[47] A1: flexray_CA_TR_EN A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A9	GPIO	fec RX_DV	A0: siul_GPIO[210] A1: flexray_DBG3 A2: etimer2_ETC[0] A3: dspi0_CS7	I: fec_RX_DV I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A10	GPIO	fec MDIO	A0: siul_GPIO[198] A1: fec_MDIO A2: _ A3: dspi2_CS0	I: _ I: _ I: siul_EIRQ[28]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A11	GPIO	fec TX_CLK	A0: siul_GPIO[207] A1: flexray_DBG0 A2: etimer2_ETC[4] A3: dspi0_CS4	I: fec_TX_CLK I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A12	GPIO	fec TX_EN	A0: siul_GPIO[200] A1: fec_TX_EN A2: _ A3: lin0_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
U20	GPIO	dramc ADD[6]	A0: siul_GPIO[164] A1: dramc_ADD[6] A2: ebi_ADD14 A3: flexpwm1_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U21	GPIO	dramc ADD[12]	A0: siul_GPIO[170] A1: dramc_ADD[12] A2: ebi_AD4 A3: ebi_ADD20	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U23	GPIO	dramc ADD[0]	A0: siul_GPIO[158] A1: dramc_ADD[0] A2: ebi_ADD8 A3: ebi_CS2	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V3	GPIO	flexpwm1 B[2]	A0: siul_GPIO[124] A1: flexpwm1_B[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V4	GPIO	dspi1 CS2	A0: siul_GPIO[56] A1: dspi1_CS2 A2: _ A3: dspi0_CS5	I: flexpwm0_FAULT[3] I: lin2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V20	GPIO	lin0 TXD	A0: siul_GPIO[18] A1: lin0_TXD A2: i2c0_clock A3: sscm_DEBUG[2]	I: _ I: _ I: siul_EIRQ[17]	—	disabled	GP Slow/ Medium	VDD_HV_IO
V21	GPIO	dramc ADD[13]	A0: siul_GPIO[171] A1: dramc_ADD[13] A2: ebi_AD5 A3: ebi_ADD21	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V23	GPIO	dramc ADD[2]	A0: siul_GPIO[160] A1: dramc_ADD[2] A2: ebi_ADD10 A3: ebi_TA	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
W3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 11. Absolute maximum ratings[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	–0.1	0.1	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage	—	–0.3	1.32	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	–0.1	0.1	V
21	TV_{DD}	SR	Slope characteristics on all V_{DD} during power up	—	—	25	mV/µs
22	V_{IN}	SR	Voltage on any pin with respect to its supply rail $V_{DD\_HV\_xxx}$	Relative to $V_{DD\_HV\_xxx}$	–0.3	$V_{DD\_HV\_xxx}$ + 0.3[8]	V
23	I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
24	$I_{INJPADA}$	SR	Injected input current on any analog pin during overload condition	—	–3	3	mA
25	I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
26	T_{STG}	SR	Storage temperature	—	–55[9]	150	°C
27	T_{SDR}	SR	Maximum Solder Temperature[10] Pb-free package SnPb package	—	 — —	 260 245	°C
28	MSL	SR	Moisture Sensitivity Level[11]	—	—	3	—

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 6.5 V for 10 hours cumulative time, 5.0 V + 10% for time remaining.

3 5.3 V for 10 hours cumulative over lifetime of device, 3.63 V for time remaining.

4 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

5 As the $V_{DD\_HV\_DRAM\_VREF}$ supply should always be constrained by the $V_{DD\_HV\_DRAM}$ supply for example through a voltage divider network per the JEDEC specification, the maximum ratings for the $V_{DD\_HV\_DRAM}$ supply should be used for the $V_{DD\_HV\_DRAM\_VREF}$ reference as well.

6 All $V_{DD\_HV\_ADRx}$ rails must be operated at the same supply voltage.

7 2.0 V for 10 hours cumulative time, 1.2 V + 10% for time remaining.

8 Only when $V_{DD\_HV\_xxx} < 5.2$ V.

9 If the ambient temperature is at or above the minimum storage temperature and below the recommended minimum operating temperature, power may be applied to the device safely. However, functionality is not guaranteed and a power cycle must be administered if in internal regulation mode or an assertion of RESET_SUP_B must be administered if in external regulation mode once device enters into the recommended operating temperature range.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

3.3 Recommended operating conditions

Table 12. Recommended operating conditions[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	3.0	5.5	V

than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

$$C_F > 8192 \bullet C_S \qquad \textit{Eqn. 12}$$

Table 24. ADC conversion characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	f_{CK}	SR	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
2	f_s	SR	Sampling frequency	—	—	—	959	kHz
3	t_{ADC_S}	D	Sample time[3]	60 MHz	383	—	—	ns
4	$t_{ADC\_S\_PMC}$	C	Sample time of internal PMC channels.	—	717	—	—	ns
5	t_{ADC_E}	P	Evaluation time[4]	60 MHz	600	—	—	ns
6	C_S[5]	D	ADC input sampling capacitance	—	—	—	7.32	pF
7	C_{P1}[5]	D	ADC input pin capacitance 1	—	—	—	2.5	pF
8	C_{P2}[5]	D	ADC input pin capacitance 2	—	—	—	0.8	pF
9	R_{SW1}[5]	D	Channel selection switch resistance	V_{REF} range = 4.5 to 5.5 V	—	—	1.0	kΩ
10				V_{REF} range = 3.0 to 3.6 V	—	—	1.2	kΩ
11	R_{AD}[5]	D	Sample switching resistance	—	—	—	825	Ω
12	I_{INJ}	T	Current injection	Current injection on one ADC input channel, different from the converted one. Other parameters stay within specified limits as long as the ADC supply stays within its specified limits due to the current injection.	–3	—	3	mA
13	INL	P	Integral non linearity	—	–3	—	3	LSB
14	DNL	P	Differential non linearity[6]	—	–1.0	—	2	LSB

2 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are verified at production test.

3 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.

4 Actual hardware programming times. This does not include software overhead.

Table 26 shows the data flash memory program and erase characteristics.

Table 26. Data flash memory program and erase electrical specifications

No.	Symbol		Parameter	Min	Typ[1]	Initial max[2]	Lifetime max[3]	Unit
1	$T_{DWPROGRAM}$	CC	Doubleword (64 bits) program time[4]	—	30	70	300	µs
2	$T_{16KPPERASE}$	CC	16 KB block pre-program and erase time	—	700	800	1500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are verified at production test.

3 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.

4 Actual hardware programming times. This does not include software overhead.

Table 27. Flash memory module life

No.	Symbol		Parameter	Condition	Value			Unit
					Min	Typ[1]	Max	
1a	P/E	CC	Number of program/erase cycles per block for over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
1b				32 KB and 64 KB blocks	10,000	100,000	—	cycles
1c				128 KB blocks	1,000	100,000	—	cycles
2	Retention	CC	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 49. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	
2	DRAM DQ	1.4/1.4	2.4/2.4	0.6/1.0	2.7/2.6	5	000
		1.7/1.7	2.8/2.7	0.2/0.4	0.5/0.6	20	
		1.4/1.5	2.4/2.5	1.1/1.1	3.0/2.7	5	001
		1.7/1.7	2.8/2.8	0.4/0.4	0.7/0.7	20	
		1.4/1.5	2.4/2.4	1.0/1.1	2.9/2.7	5	010
		1.7/1.7	2.8/2.7	0.3/0.4	0.6/0.7	20	
		1.4/1.5	2.5/2.5	1.5/1.1	3.1/2.6	5	110
		1.7/1.8	2.8/2.8	0.4/0.4	0.7/0.6	20	
3	DRAM CLK	1.4/1.4	2.4/2.4	0.4/0.6	2.7/2.7	5	000
		1.6/1.6	2.7/2.7	0.7/0.9	1.8/3.4	20	
		1.4/1.4	2.4/2.4	1.1/1.1	3.0/2.8	5	001
		1.7/1.7	2.7/2.7	0.3/0.4	1.0/1.1	20	
		1.4/1.4	2.4/2.4	0.9/1.1	3.0/2.8	5	010
		1.6/1.6	2.7/2.7	0.3/0.4	0.9/1.0	20	
		1.4/1.4	2.5/2.5	1.5/1.2	3.2/2.6	5	110
		1.7/1.7	2.7/2.7	0.4/0.4	1.1/1.2	20	

[1] L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

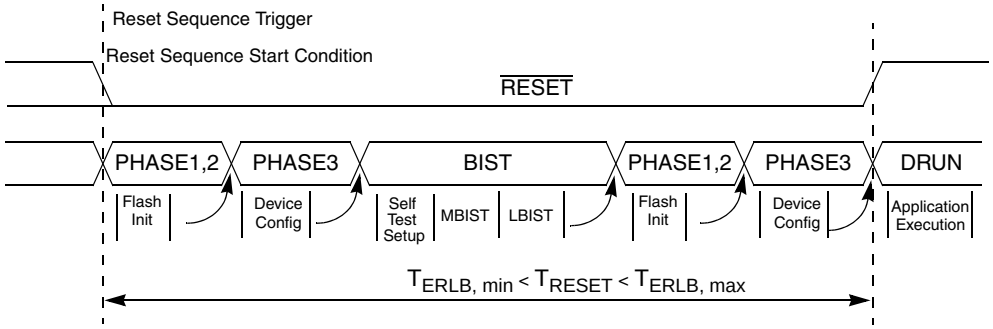


Figure 14. External reset sequence long, BIST enabled

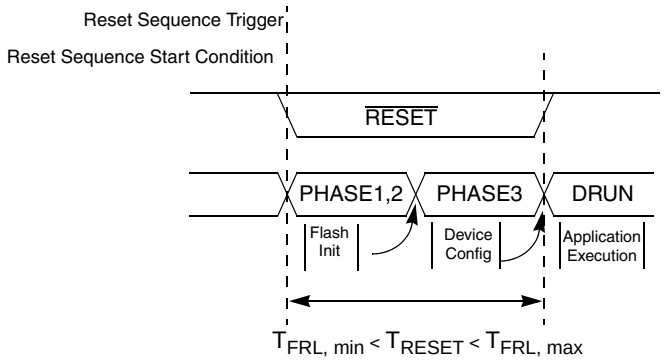


Figure 15. Functional reset sequence long

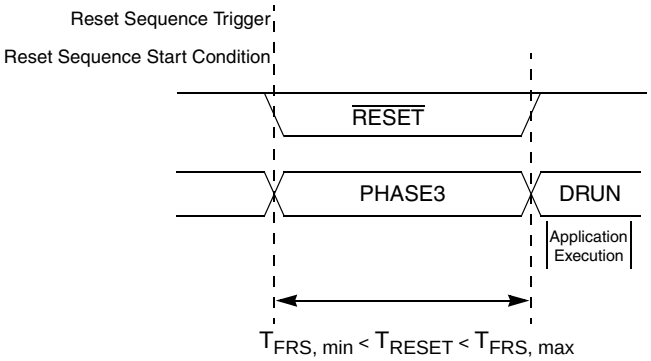


Figure 16. Functional reset sequence short

The reset sequences shown in Figure 15 and Figure 16 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence. See the RGM_FBRE register in the *MPC5675K Reference Manual* for more information.

3.21.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences, depending on the VREG mode (external or internal). It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 52.

8 If $\overline{\text{RESET}}$ is configured for short reset.

9 Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.21.4 Reset sequence—start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.21.4.1 Internal VREG mode

Figure 17 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*. The last voltage rail crossing the levels shown in Figure 17 determines the start of the reset times specified in Table 52.

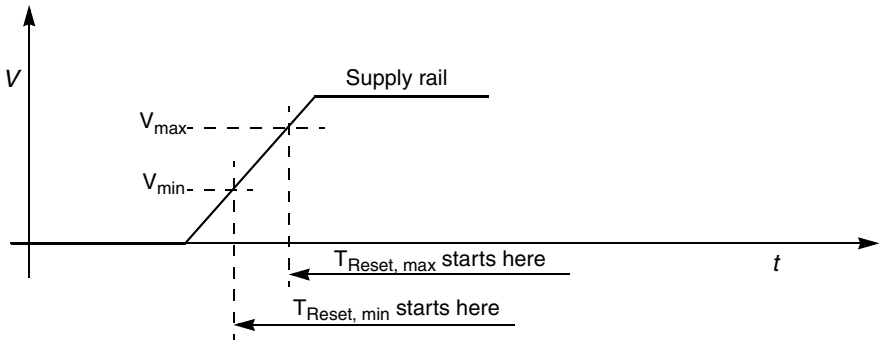


Figure 17. Reset sequence start in internal VREG mode

Table 54. Voltage thresholds

Variable name	Value
V_{min}	LvdReg – 3.5%
V_{max}	LvdReg + 3.5%
Supply Rail	VDD_HV_PMU VDD_HV_IO VDD_HV_FLASH VDD_HV_ADV

3.21.4.2 External VREG mode

Figure 18 and Figure 19 show the voltage thresholds that determine the start of the Destructive Reset Sequence, BIST enabled and the start for the Destructive Reset Sequence, BIST disabled.

NOTE

$\overline{\text{RESET\_SUP}}$ must not be released unless $V_{DD\_LV\_xxx}$ is within its valid range of operation. $\overline{\text{RESET\_SUP}}$ input circuitry needs a valid $V_{DD\_HV\_IO}$ rail in order to detect a high level on $\overline{\text{RESET\_SUP}}$.

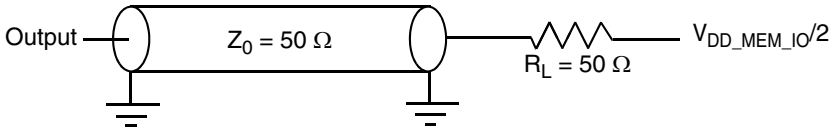


Figure 25. DDR AC test load

3.22.2 IEEE 1149.1 (JTAG) interface timing

3.22.2.1 Standard interface timing

Table 56. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	60	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	12	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	6	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	18	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	6	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	18	ns
9	t_{BSDV}	D	TCK falling edge to output valid (BSR)	—	—	14	ns
10	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance (BSR)	—	—	15	ns
11	t_{BSDHZ}	D	TCK falling edge to output high impedance (BSR)	—	—	10	ns
12	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	15	—	ns
13	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	2	—	ns

[1] $f_{TCK} = 1/t_{TCK}$. f_{TCK} needs to be smaller than the system clock (SYS_CLK).

3.22.2.2 Interface timing for Full Cycle mode

Table 57. JTAG pin Full Cycle mode AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	40	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	12	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	6	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	18	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	6	—	ns

[1] $f_{TCK} = 1/t_{TCK}$. f_{TCK} needs to be smaller than the system clock (SYS_CLK). This frequency is valid only in special modes where TDO is sampled at the next falling edge for Core0/1 Nexus TAPs and hence full cycle is given to TDO for settling before it is sampled.

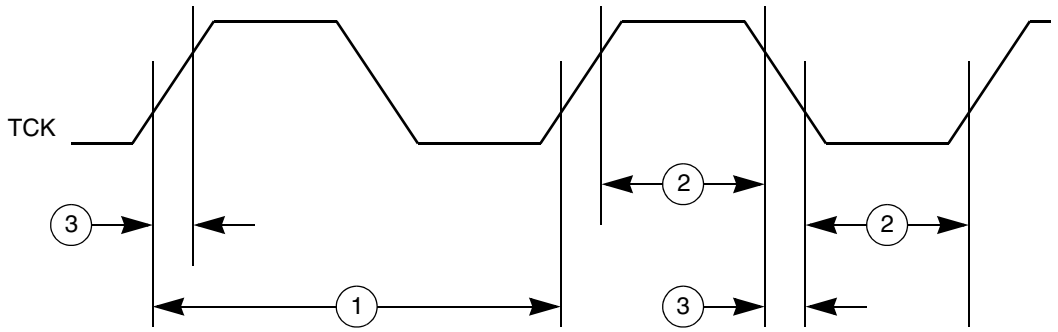


Figure 26. JTAG test clock input timing

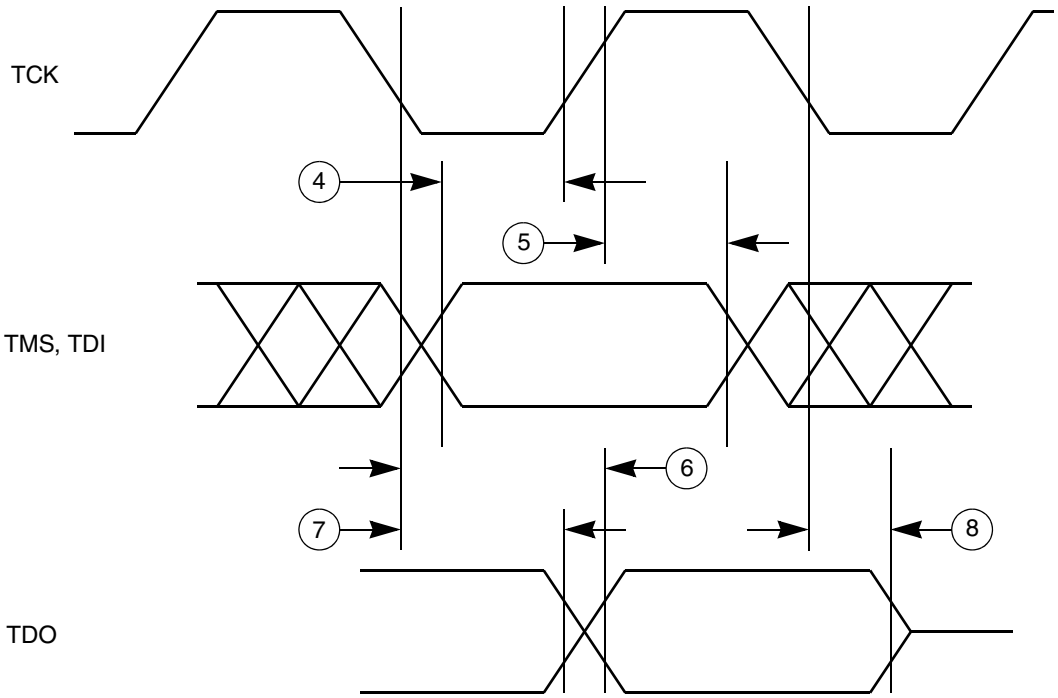


Figure 27. JTAG test access port timing

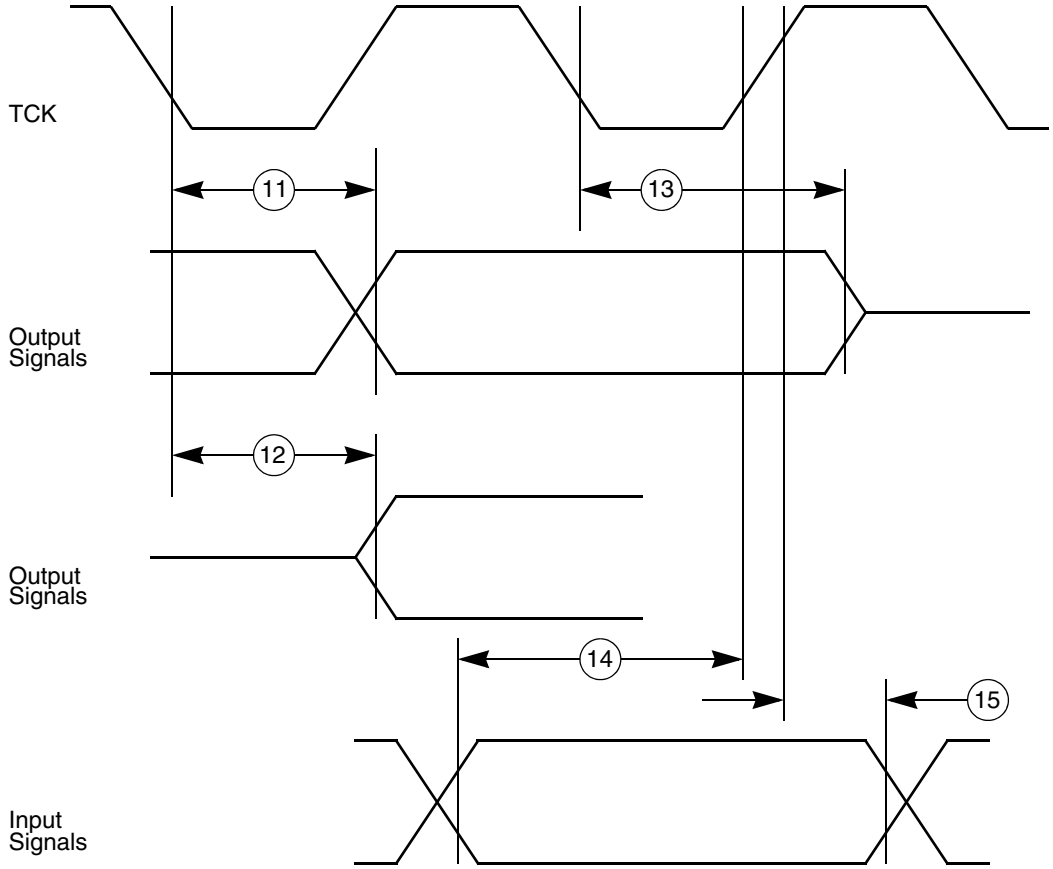


Figure 28. JTAG boundary scan timing

3.22.3 Nexus timing

Table 58. Nexus debug port timing Div mode = 2[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCKO}	CC	MCKO cycle time	—	16.67	—	ns
2	t_{MDC}	CC	MCKO duty cycle[2]	—	50	50	%
3	t_{MDOV}	CC	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ data valid[3]	—	–1.67	3.34	ns
4	t_{EVTIPW}	CC	$\overline{\text{EVTI}}$ pulse width. Captured on JTAG TCK.	—	4.0	—	t_{JCYC}
5	t_{PW}	CC	MDO, $\overline{\text{MSEO}}$,$\overline{\text{EVTO}}$ pulse width in SDR mode	—	1	—	t_{MCKO}

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Rise/Fall time for Nexus signals can be derived from Fast GPIO pad specification section.

2 Jitter/tolerance for MCKO clock is derived from PLL. Please see PLL section for jitter specification.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle in SDR mode. For DDR mode, this timing is same for both MCKO edges.

Table 60. Nexus debug port timing DIVIDE by 4 DDR mode[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCKO}	CC	MCKO cycle time	—	22.22	—	ns
2	t_{MDC}	CC	MCKO duty cycle[2]	—	50	50	%
3	t_{MDOV}	CC	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ data valid[3]	—	–2.23	4.45	ns
4	t_{EVTIPW}	CC	$\overline{\text{EVTI}}$ pulse width	—	4.0	—	t_{JCYC}
5	t_{PW}	CC	MDO, $\overline{\text{MSEO}}$,$\overline{\text{EVTO}}$ pulse width in DDR mode	—	0.5	—	t_{MCKO}

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.Rise/Fall time for Nexus signals can be derived from Fast GPIO pad specification section.

2 Jitter/tolerance for MCKO clock is derived from PLL. Please see PLL section for jitter specification.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid for half of time period. Using this time period, Data valid window for these signals is between 0.2 t_{MCKO} to 0.4 t_{MCKO} starting from each MCKO edge.

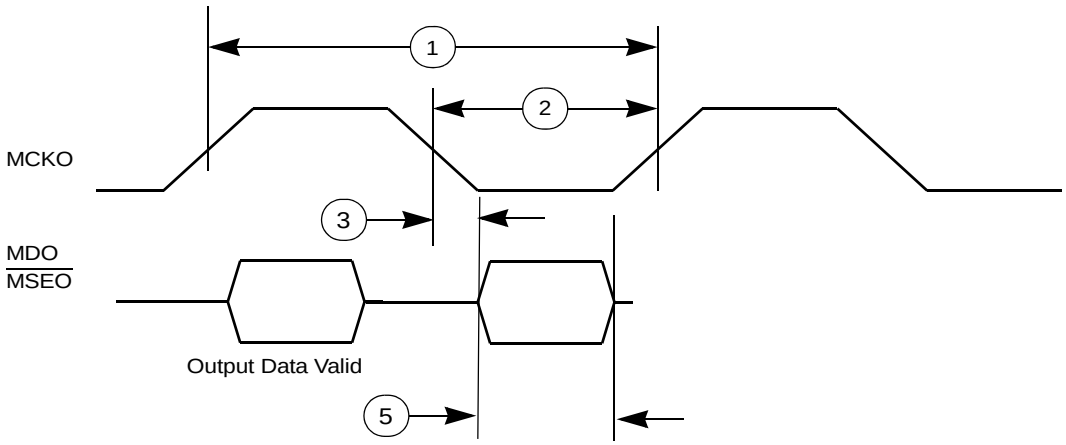


Figure 31. Nexus DDR mode timing

3.22.4 External interrupt timing (IRQ pins)

Table 61. External interrupt timing (NMI IRQ)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	SR	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	SR	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	SR	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Table 62. External interrupt timing (GPIO IRQ)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	SR	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	SR	IRQ pulse width high	—	3	—	t_{CYC}

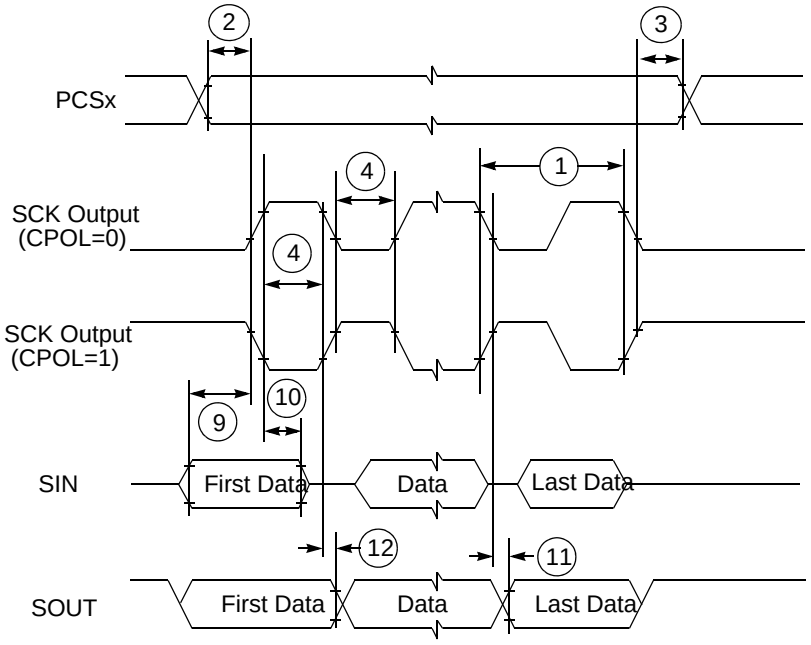


Figure 33. DSPI classic SPI timing—master, CPHA = 0

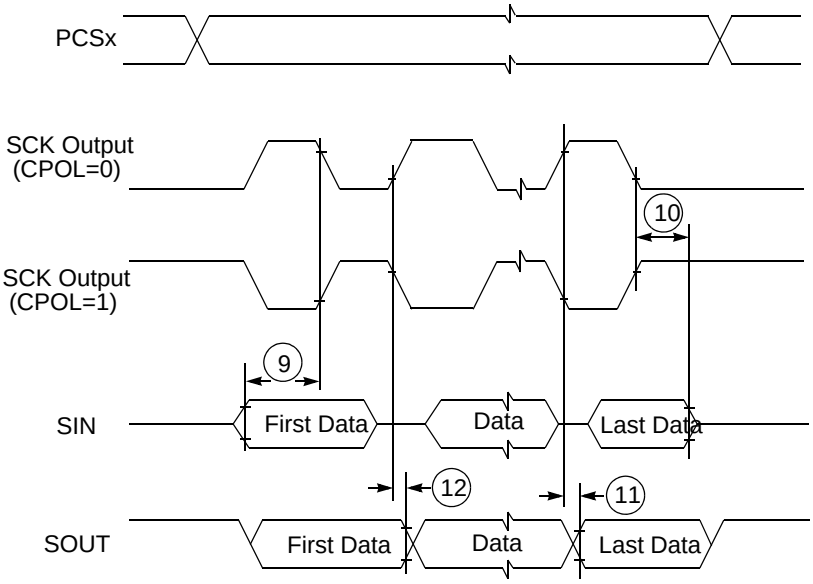


Figure 34. DSPI classic SPI timing—master, CPHA = 1