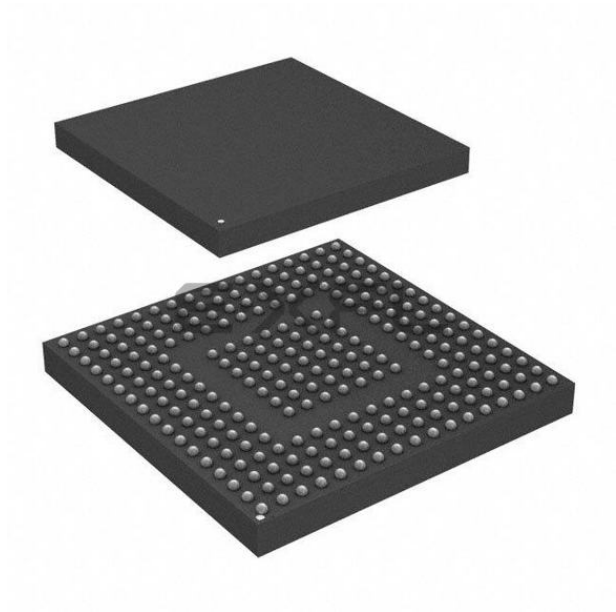

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5673kff0vmm1r

- On-chip CAN/UART bootstrap loader
- Capable of operating on a single 3.3 V voltage supply
  - 3.3 V-only modules: I/O, oscillators, flash memory
  - 3.3 V or 5 V modules: ADCs, supply to internal VREG
  - 1.8–3.3 V supply range: DRAM/PDI
- Operating junction temperature range –40 to 150 °C

1.6 Feature details

1.6.1 High-performance e200z7d core processor

- Dual 32-bit Power Architecture® processor core
- Loose or tight core coupling
- Freescale Variable Length Encoding (VLE) enhancements for code size footprint reduction
- Thirty-two 64-bit general-purpose registers (GPRs)
- Memory management unit (MMU) with 64-entry fully-associative translation look-aside buffer (TLB)
- Branch processing unit
- Fully pipelined load/store unit
- 16 KB Instruction and 16 KB Data caches per core with line locking
  - Four way set associative
  - Two 32-bit fetches per clock
  - Eight-entry store buffer
  - Way locking
  - Supports tag and data cache parity
  - Supports EDC for instruction cache
- Vectored interrupt support
- Signal processing engine 2 (SPE2) auxiliary processing unit (APU) operating on 64-bit general purpose registers
- Floating point
  - IEEE® 754 compatible with software wrapper
  - Single precision in hardware; double precision with software library
  - Conversion instructions between single precision floating point and fixed point
- Long cycle time instructions (except for guarded loads) do not increase interrupt latency in the MPC5675K
- To reduce latency, long cycle time instructions are aborted upon interrupt requests
- Extensive system development support through Nexus debug module

1.6.2 Crossbar Switch (XBAR)

- 32-bit address bus, 64-bit data bus
- Simultaneous accesses from different masters to different slaves (there is no clock penalty when a parked master accesses a slave)

1.6.3 Memory Protection Unit (MPU)

Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

1.6.11 DRAM controller

The DRAM controller (available only on 473-pin devices) is a multi-port controller that monitors incoming requests on the three AHB slave ports and decides (at each rising clock edge) what command needs to be sent to the external DRAM.

The DRAM controller on this device supports the following types of memories:

- Mobile DDR (mDDR)
- DDR 1
- DDR 2 (optional)
- SDR

The controller has the following features:

- Optimized timing for 32-byte bursts and single read accesses on the AHB interface
- Optimized timing for 8-byte and 16-byte bursts on the DRAMC interface
- Supports priority elevation on the slave ports for single accesses
- 16-bit wide DRAM interface
- One chip select (CS)
- mDDR memory controller
  - 16-bit external interface
  - Address range up to 8 MB

1.6.12 Boot Assist Module (BAM)

- Enables booting via serial mode (FlexCAN, LINFlex)
- Handles static mode in case of an erroneous boot procedure
- Implemented in 8 KB ROM
- Supports Lock Step Mode (LSM) and Decoupled Parallel Mode (DPM)

1.6.13 Parallel Data Interface (PDI)

- Support for external ADC and CMOS image sensors
- Parallel interface operation up to MCU system bus frequency
- Selectable data capture from rising or falling edge
- Receive FIFO with adjustable trigger thresholds
- Data width for 8, 10, 12, 14, and 16 bits
- Data Packing Unit to pack input data on 64-bit words — data packed on 8- or 16- bit boundary, depending on input data width
- Binary increasing channel select that allows as many as eight channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK

1.6.14 Deserial Serial Peripheral Interface (DSPI) modules

- Three serial peripheral interfaces
  - Full duplex communication ports with interrupt and eDMA request support
  - Support for all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
D13	VDD_HV_FLA	VDD_HV	V6	VDD_LV_COR	VDD_LV
V1	VDD_HV_OSC	VDD_HV	V7	VDD_LV_COR	VDD_LV
D16	VDD_HV_PDI	VDD_HV	V8	VDD_LV_COR	VDD_LV
D20	VDD_HV_PDI	VDD_HV	V9	VDD_LV_COR	VDD_LV
AC17	VDD_HV_PMU	VDD_HV	V10	VDD_LV_COR	VDD_LV
F6	VDD_LV_COR	VDD_LV	V11	VDD_LV_COR	VDD_LV
F7	VDD_LV_COR	VDD_LV	V12	VDD_LV_COR	VDD_LV
F8	VDD_LV_COR	VDD_LV	V13	VDD_LV_COR	VDD_LV
F9	VDD_LV_COR	VDD_LV	V14	VDD_LV_COR	VDD_LV
F10	VDD_LV_COR	VDD_LV	V15	VDD_LV_COR	VDD_LV
F11	VDD_LV_COR	VDD_LV	V16	VDD_LV_COR	VDD_LV
F12	VDD_LV_COR	VDD_LV	V17	VDD_LV_COR	VDD_LV
F13	VDD_LV_COR	VDD_LV	V18	VDD_LV_COR	VDD_LV
F14	VDD_LV_COR	VDD_LV	Y4	VDD_LV_PLL	VDD_LV
V_{SS}					
A2	VSS_HV_IO	VSS_HV	L7	VSS_LV_COR	VSS_LV
A22	VSS_HV_IO	VSS_HV	L8	VSS_LV_COR	VSS_LV
A23	VSS_HV_IO	VSS_HV	L9	VSS_LV_COR	VSS_LV
B1	VSS_HV_IO	VSS_HV	L10	VSS_LV_COR	VSS_LV
B2	VSS_HV_IO	VSS_HV	L11	VSS_LV_COR	VSS_LV
B14	VSS_HV_IO	VSS_HV	L12	VSS_LV_COR	VSS_LV
B23	VSS_HV_IO	VSS_HV	L13	VSS_LV_COR	VSS_LV
C3	VSS_HV_IO	VSS_HV	L14	VSS_LV_COR	VSS_LV
D9	VSS_HV_IO	VSS_HV	L15	VSS_LV_COR	VSS_LV
D11	VSS_HV_IO	VSS_HV	L16	VSS_LV_COR	VSS_LV
H2	VSS_HV_IO	VSS_HV	L17	VSS_LV_COR	VSS_LV
K20	VSS_HV_IO	VSS_HV	M7	VSS_LV_COR	VSS_LV
L4	VSS_HV_IO	VSS_HV	M8	VSS_LV_COR	VSS_LV
N2	VSS_HV_IO	VSS_HV	M9	VSS_LV_COR	VSS_LV
A1	VSS_HV_IO	VSS_HV	M10	VSS_LV_COR	VSS_LV
R4	VSS_HV_IO	VSS_HV	M11	VSS_LV_COR	VSS_LV
W2	VSS_HV_IO	VSS_HV	M12	VSS_LV_COR	VSS_LV
Y12	VSS_HV_IO	VSS_HV	M13	VSS_LV_COR	VSS_LV
AA3	VSS_HV_IO	VSS_HV	M14	VSS_LV_COR	VSS_LV

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
T2	GPIO	flexpwm1 A[0]	A0: siul_GPIO[117] A1: flexpwm1_A[0] A2: _ A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T3	GPIO	flexpwm1 A[1]	A0: siul_GPIO[120] A1: flexpwm1_A[1] A2: _ A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T20	GPIO	dramc ADD[8]	A0: siul_GPIO[166] A1: dramc_ADD[8] A2: ebi_AD0 A3: ebi_ADD16	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T21	GPIO	dramc ADD[9]	A0: siul_GPIO[167] A1: dramc_ADD[9] A2: ebi_AD1 A3: ebi_ADD17	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T22	GPIO	dramc ADD[1]	A0: siul_GPIO[159] A1: dramc_ADD[1] A2: ebi_ADD9 A3: ebi_CS3	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U1	GPIO	flexpwm1 B[0]	A0: siul_GPIO[118] A1: flexpwm1_B[0] A2: _ A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U2	GPIO	flexpwm1 B[1]	A0: siul_GPIO[121] A1: flexpwm1_B[1] A2: _ A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U3	GPIO	flexpwm1 A[2]	A0: siul_GPIO[123] A1: flexpwm1_A[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U4	GPIO	dspi2 SCK	A0: siul_GPIO[11] A1: dspi2_SCK A2: _ A3: _	I: can3_RXD I: _ I: siul_EIRQ[10]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
Y9	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y10	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y11	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
Y14	ANA	adc0_adc1 AN[11]	—	siul_GPI[25]	AN: adc0_adc1_AN[11]	—	Analog Shared	VDD_HV_ADR0
Y15	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y16	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y17	ANA	adc1 AN[8]	—	siul_GPI[74]	AN: adc1_AN[8]	—	Analog	VDD_HV_ADR1
Y18	ANA	adc1 AN[6]	—	siul_GPI[76]	AN: adc1_AN[6]	—	Analog	VDD_HV_ADR1
Y21	GPIO	dramc ADD[15]	A0: siul_GPIO[173] A1: dramc_ADD[15] A2: ebi_AD7 A3: ebi_ADD23	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AA14	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR0
AA15	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR1
AA16	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR1
AA17	ANA	adc1 AN[5]	—	siul_GPI[64]	AN: adc1_AN[5]	—	Analog	VDD_HV_ADR1
AA18	ANA	adc1 AN[7]	—	siul_GPI[73]	AN: adc1_AN[7]	—	Analog	VDD_HV_ADR1
AA19	GPIO	TDI	A0: siul_GPIO[21] A1: _ A2: _ A3: _	I: jtagc_TDI I: _ I: _	—	pullup	GP Slow/ Medium	VDD_HV_IO
AA20	GPIO	etimer1 ETC[0]	A0: siul_GPIO[4] A1: etimer1_ETC[0] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[4]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA22	GPIO	lin1 TXD	A0: siul_GPIO[94] A1: lin1_TXD A2: i2c1_clock A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA23	GPIO	dramc ADD[10]	A0: siul_GPIO[168] A1: dramc_ADD[10] A2: ebi_AD2 A3: ebi_ADD18	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AB3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AB15	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR1
AB16	ANA	adc1 AN[3]	—	siul_GPI[32]	AN: adc1_AN[3]	—	Analog	VDD_HV_ADR1
AB17	ANA	adc1 AN[4]	—	siul_GPI[75]	AN: adc1_AN[4]	—	Analog	VDD_HV_ADR1
AB18	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
AB21	GPIO	lin1 RXD	A0: siul_GPIO[95] A1: _ A2: i2c1_data A3: _	I: lin1_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC3	GPIO	dspi2 SIN	A0: siul_GPIO[13] A1: _ A2: _ A3: _	I: dspi2_SIN I: flexpwm0_FAULT[0] I: siul_EIRQ[12]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC4	GPIO	flexpwm1 A[3]	A0: siul_GPIO[126] A1: flexpwm1_A[3] A2: etimer2_ETC[4] A3: dspi0_CS7	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC5	GPIO	flexpwm1 B[3]	A0: siul_GPIO[127] A1: flexpwm1_B[3] A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC6	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	GP Slow/ Medium	VDD_HV_ADR23
AC9	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR23

Table 11. Absolute maximum ratings[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	–0.1	0.1	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage	—	–0.3	1.32	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	–0.1	0.1	V
21	TV_{DD}	SR	Slope characteristics on all V_{DD} during power up	—	—	25	mV/µs
22	V_{IN}	SR	Voltage on any pin with respect to its supply rail $V_{DD\_HV\_xxx}$	Relative to $V_{DD\_HV\_xxx}$	–0.3	$V_{DD\_HV\_xxx}$ + 0.3[8]	V
23	I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
24	$I_{INJPADA}$	SR	Injected input current on any analog pin during overload condition	—	–3	3	mA
25	I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
26	T_{STG}	SR	Storage temperature	—	–55[9]	150	°C
27	T_{SDR}	SR	Maximum Solder Temperature[10] Pb-free package SnPb package	—	 — —	 260 245	°C
28	MSL	SR	Moisture Sensitivity Level[11]	—	—	3	—

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 6.5 V for 10 hours cumulative time, 5.0 V + 10% for time remaining.

3 5.3 V for 10 hours cumulative over lifetime of device, 3.63 V for time remaining.

4 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

5 As the $V_{DD\_HV\_DRAM\_VREF}$ supply should always be constrained by the $V_{DD\_HV\_DRAM}$ supply for example through a voltage divider network per the JEDEC specification, the maximum ratings for the $V_{DD\_HV\_DRAM}$ supply should be used for the $V_{DD\_HV\_DRAM\_VREF}$ reference as well.

6 All $V_{DD\_HV\_ADRx}$ rails must be operated at the same supply voltage.

7 2.0 V for 10 hours cumulative time, 1.2 V + 10% for time remaining.

8 Only when $V_{DD\_HV\_xxx} < 5.2$ V.

9 If the ambient temperature is at or above the minimum storage temperature and below the recommended minimum operating temperature, power may be applied to the device safely. However, functionality is not guaranteed and a power cycle must be administered if in internal regulation mode or an assertion of RESET_SUP_B must be administered if in external regulation mode once device enters into the recommended operating temperature range.

10 Solder profile per CDF-AEC-Q100.

11 Moisture sensitivity per JEDEC test method A112.

3.3 Recommended operating conditions

Table 12. Recommended operating conditions[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	3.0	5.5	V

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$\mathbf{T_J = T_T + (\Psi_{JT} \times P_D)} \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

See [6] to [10] in Section 6, Reference documents, for more information.

3.5 Electromagnetic interference (EMI) characteristics

3.5.1 Test Setup

Electromagnetic emission tests are performed by TEM cell [2] and via direct coupling [3] (150 Ω) measurements.

Electromagnetic immunity is measured by DPI [4].

See Section 6, Reference documents, for more information.

3.5.2 Test parameters

The following test parameters shall be used:

Table 14. EMC test parameters

Method	Frequency Range	Receiver	
		BW	Step Size
150 Ω	1 MHz to 1000 MHz	1 MHz	500 kHz
TEM			

3 "Loss of Reference Frequency" window is the reference frequency range outside of which the FMPLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the f_{LOR} window.

5 f_{VCO} is the frequency at the output of the VCO; its range is 256–512 MHz.
f_{SCM} is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
$f_{sys} = f_{VCO} \div ODF$

6 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.

7 This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{FMPLLOUT}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

12 Core operating at 180 MHz.

13 Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

14 PLL Loop Division Factor (LDF).

3.13 16 MHz RC oscillator electrical characteristics

Table 23. RC oscillator electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	f_{RC}	CC	RC oscillator frequency	25 °C, 1.2 V trimmed	—	16	—	MHz
2	Δ_{RCMVAR}	CC	Frequency spread: The variation in output frequency from PTF[1] across temperature and supply voltage range	—	—	—	±5	%
3	$\Delta_{IRCTRIM}$	CC	Internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1 PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature.

3.14 ADC electrical characteristics

The MPC5675K provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

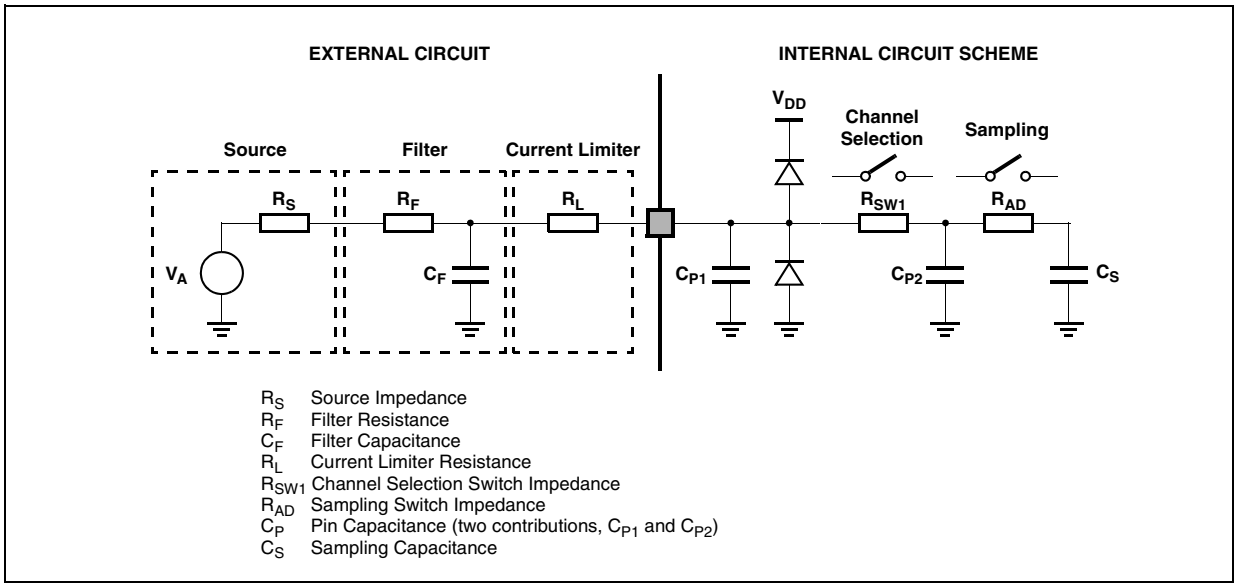

Figure 9. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1}, and C_{P2} are initially charged at the source voltage V_A (please see the equivalent circuit in Figure 9): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch is closed).

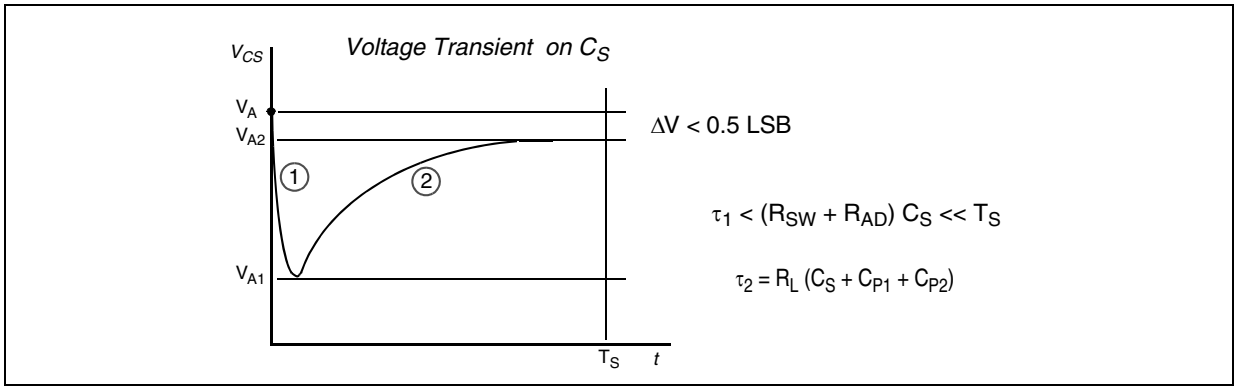

Figure 10. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is:

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 5}$$

– 150 Ω

The electrical data provided in Section 3.19, DRAM pad specifications, applies to the pads listed in Table 39.

Table 39. DRAM pads

Name	Voltage	Used For	Notes[1]
DRAM ACC	1.62 V–3.6 V	I/O	Bidirectional DDR pad
DRAM CLK	1.62 V–3.6 V	O	Output only differential clock driver pad
DRAM DQ	1.62 V–3.6 V	I/O	Bidirectional DDR pad with integrated ODT

1 All pads can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.

All three pad types can be configured to support SDR, DDR, DDR2 half and full strength, and LPDDR half and full strength modes, according to Table 40.

Table 40. Mode configuration for DRAM pads

Configuration[1]	Mode
000	1.8 V LPDDR Half Strength
001	1.8 V LPDDR Full Strength
010	1.8 V DDR2 Half Strength
011	2.5 V DDR
100	Not supported
101	Not supported
110	1.8 V DDR2 Full Strength
111	SDR

1 Configuration is selected in the corresponding PCR registers of the SIUL.

NOTE

0.7 V overshoot/undershoot can be allowed to occur repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.

3.19.1 DRAM pads electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

Table 41. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	3.0	3.6	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	1.3	1.7	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ − 0.05	$V_{DD\_HV\_DRAM\_VREF}$ + 0.05	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.20	—	V

Table 47. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 1.8 V) (continued)

No.	Symbol		Parameter	Condition	Min	Max	Unit
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	$0.49 \times V_{DD\_HV\_DRAM}$	$0.51 \times V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.125	—	V
5	V_{IL}	CC	Input low voltage	—	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.125	V
6	V_{OH}	CC	Output high voltage	—	1.42	—	V
7	V_{OL}	CC	Output low voltage	—	—	0.28	V

1 BGA473: Termination voltage can be supplied via package pins. BGA257 Termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT.

Table 48. Output drive current @ V_{DDE} = 1.8 V (±100 mV)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
2	DRAM DQ	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4
3	DRAM CLK	000	–3.57	3.57
		001	–7.84	7.84
		010	–5.36	5.36
		110	–13.4	13.4

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.

2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

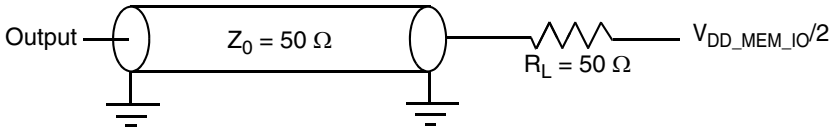

Figure 25. DDR AC test load

3.22.2 IEEE 1149.1 (JTAG) interface timing

3.22.2.1 Standard interface timing

Table 56. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	60	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	12	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	6	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	18	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	6	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	18	ns
9	t_{BSDV}	D	TCK falling edge to output valid (BSR)	—	—	14	ns
10	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance (BSR)	—	—	15	ns
11	t_{BSDHZ}	D	TCK falling edge to output high impedance (BSR)	—	—	10	ns
12	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	15	—	ns
13	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	2	—	ns

[1] $f_{TCK} = 1/t_{TCK}$. f_{TCK} needs to be smaller than the system clock (SYS_CLK).

3.22.2.2 Interface timing for Full Cycle mode

Table 57. JTAG pin Full Cycle mode AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time [1]	—	40	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at $V_{DDE}/2$)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	12	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	6	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	18	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	6	—	ns

Table 64. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
6	t_{DIS}	CC	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	CC	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	$\overline{PCSS}$ to PCS*x* time	—	13	—	ns
9	t_{SUI}	CC	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	CC	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	CC	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	11	
				Master (MTFE = 1, CPHA = 1)	—	5	
12	t_{HO}	CC	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	
13	t_{DT}	CC	Delay after Transfer (minimum $\overline{CS}$ negation time)	Continuous mode Non-continuos mode[2]	62 134	— —	ns

1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. Note that in this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

2 In non-continuous mode, this value is always t_{SCK} × DSPI_CTAR*n*[DT] × DSPI_CTAR*n*[PDT]. The minimum permissible value of DT is 2 and the minimum permissible value of PDT is 1. See the DSPI chapter of the *MPC5675K Reference Manual* for more information.

Table 70. EBI timing (continued)

No.	Symbol		Parameter	45 MHz (Ext. Bus Freq)[1]		Unit	Notes
				Min	Max		
6	t_{COV}	CC	D_CLKOUT posedge to output signal valid (output delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE $\overline{\text{D\_RD\_WR}}$ D_TA D_TS $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]	—	10	ns	—
7	t_{CIS}	CC	Input signal valid to D_CLKOUT posedge (setup time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	7.5	—	ns	—
8	t_{CIH}	CC	D_CLKOUT posedge to input signal invalid (hold time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	1.0	—	ns	—
9	t_{APW}	CC	D_ALE pulse width	6.5	—	ns	The timing is for asynchronous external memory system.
10	t_{AAI}	CC	D_ALE negated to address invalid	1.5	—	ns	• The timing is for asynchronous external memory system. • ALE is measured at 50% of VDDE.

[1] Speed is the nominal maximum frequency. Maximum core speed allowed is 180 MHz plus frequency modulation (FM).

Table 73. Revision history

Revision	Date	Description of Changes
1	6 Oct 2009	Initial release.
2	6 Dec 2009	Updated ball map tables, pin mux tables, supply and system pin tables. Added PMC specifications.
3	2 Jul 2010	Updated ball map tables, pin mux tables, supply and system pin tables. Updated pad specifications. Added reset specifications section.
4	30 Apr 2011	Removed thickness dimension from package diagrams on cover page. Added footnote “Do not connect pin directly to a power supply or ground” for MDO[0:15] and MSEO[0:1] pins to Table 9 (257 MAPBGA pin multiplexing) and Table 10 (473 MAPBGA pin multiplexing). In Table 17 (PMC electrical specifications): • Added minimum and maximum slew rate specifications for LvdReg. • Removed LvdC minimum and maximum hysteresis specifications • Removed HvdC minimum and maximum hysteresis specifications • Corrected HvcD nominal hysteresis from 1.32 to 1.36 In Table 18 (VRC SMPS recommended external devices), updated specifications for device Q (FET). Renamed Section 3.9, Supply current characteristics (was “Power dissipation and current consumption”). Renamed Table 19 (Current consumption characteristics) (was “Power dissipation characteristics”). In Table 19 (Current consumption characteristics): • Updated ADC current consumption to 1.2 mA per ADC plus 0.7 mA (2.0 mA total) for ADC0. • Updated Run I_{DD} to 900 mA max. Updated Accuracy specification in Table 20 (Temperature sensor electrical characteristics): changed “T_J = –40 °C to T_A = 25 °C” to “T_J = –40 °C to T_A = 125 °C,” removed row “T_J = T_A to 125 °C”. In Table 21 (Main oscillator electrical characteristics), added symbol name F_{XOSCHS} for Oscillator frequency specification. Removed “Typical” figures for these specifications. Added footnote “ADC0 includes 0.7 mA dissipation for the temperature sensor (TSENS).” In Table 22 (FMPLL electrical characteristics), added minimum and maximum values for specification f_{FREE}, “Free running frequency.” In Table 23 (RC oscillator electrical characteristics): • Added specification $\Delta_{IRCTRIM}$ “Internal RC oscillator trimming step.” • Removed specification Δ_{RCTRIM} “Post trim accuracy: The variation of the PTF from the 16 MHz” (specification replaced by $\Delta_{IRCTRIM}$ “Internal RC oscillator trimming step”). In Table 24 (ADC conversion characteristics), updated Gain Error (GNE) to “min = –4 max = +4 LSB“ . Added Table 30 (Code flash write access timing) and Table 31 (Data flash write access timing).

Table 73. Revision history (continued)

Revision	Date	Description of Changes
5	6 Dec 2011	Editorial changes. Enabled the use of cross-references in this revision-history table beginning with Rev. 4. Changed title of Section 1, Introduction (was “Overview”). Added section headings: Section 1.1, Document overview, Section 1.2, Description In Table 1 (MPC5675K family device comparison): • Revised the DSPI entry to reflect the proper number of chip selects on MPC5675K and MPC5674K. • Revised the FlexRay entry (was optional for all chips, is present on MPC5675K and optional on the others). • Deleted the “Clock output” entry. In Figure 1 (MPC5675K block diagram), added SWT_0 and SWT_1. In Section 1.6.3, Memory Protection Unit (MPU), deleted "The Memory Protection Unit splits the physical memory into 16 different regions." In Section 1.6.11, DRAM controller, deleted “DDR 2 (optional)”. Revised Section 1.6.14, Deserial Serial Peripheral Interface (DSPI) modules, to reflect the accurate number of available chip selects. In Section 1.6.16, FlexCAN, deleted “Safety CAN features on 1 CAN module as implemented on MPC5604P”. In Table 17 (PMC electrical specifications): • Removed Min and Max values for LVD 1.2 V variation at reset, LVD 1.2 V variation after reset, LVD 1.2 V hysteresis, HVD 1.2 V variation at reset, HVD 1.2 V variation after reset, and HVD 1.2 V hysteresis. • Updated Nominal HVD 1.2 V Typ value to 1.36 V. In Table 18 (VRC SMPS recommended external devices), updated the "Part description", “Nominal”, and "Description" columns for reference designator Q. In Table 22 (FMPLL electrical characteristics): • Updated $f_{REF\_CRYSTAL}$ and f_{REF_EXT} min to 4 MHz; max to 120 MHz. For this spec, added footnote: “PFD clock range is 4– 16 MHz. An appropriate IDF should be chosen to divide the reference frequency to this range.” • Updated f_{PLL_IN} min to 4 MHz; max to 16 MHz. • Updated f_{FREE} min to 19 MHz; max to 60 MHz. • Updated t_{lpll} max to 200 µs. • Updated t_{dc} min to 20%; max to 80%. • Updated C_{JITTER} max peak-to-peak to 160 ps; removed min. Added footnote on condition: “Core operating at 180 MHz.” Updated long-term jitter max to 6 ns. • Updated f_{LCK} min to –4%; max to +4%. • Updated f_{UL} min to –16%; max to +16%. • Updated Modulation Depth f_{CS} min to ±0.25%; max to±4%; f_{DS} min to –0.5%; max to –8%. • Removed f_{MOD} min; updated max to 35 kHz for LDF > 63; (2240/LDF)kHz for 31 < LDF < 63. In Table 23 (RC oscillator electrical characteristics), changed the temperature in the condition for f_{RC} (was 27 °C, is 25 °C). In Table 24 (ADC conversion characteristics), changed the maximum specification for DNL (was 1.0 LSB, is 2 LSB). In Section 3.18, PDI pads specifications: • Changed bullet “VDD_HV_PDI range” to “VDD_HV_PDI range 1.8 V to 3.3 V, as specified in the following tables” and removed sub-bullets. • Consolidated the three sets of DC and AC specifications (for 1.8 V, 2.5 V, and 3.3 V) into one set of specifications spanning the range 1.62–3.6 V. (Section headers 3.18.1, 3.18.2, and 3.18.3 removed, and titles of Table 36 (PDI pads DC electrical characteristics), Table 37 (Drive current), and Table 38 (PDI pads AC electrical characteristics) changed.)

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