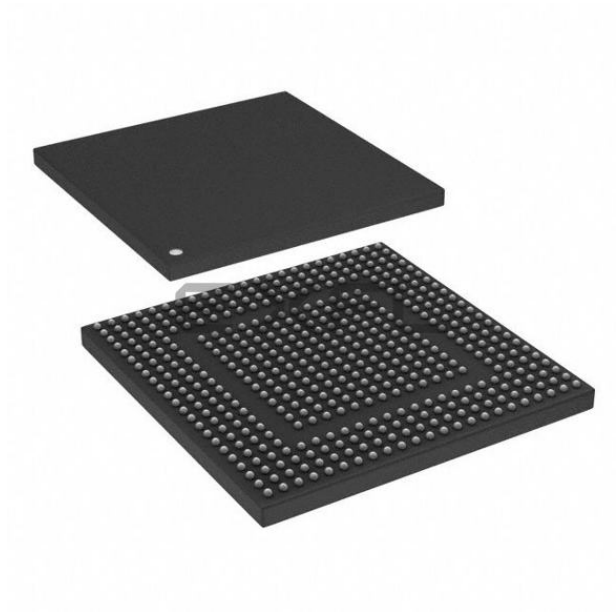

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674kf0vms2r

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

1.6.4 Enhanced Direct Memory Access (eDMA) controller

- 32 channels support independent 8-, 16-, 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to post-increment or remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer

1.6.5 Interrupt Controller (INTC)

- 208 peripheral interrupt requests
- 8 software settable sources
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resources

1.6.6 Frequency-Modulated Phase-Locked Loop (FMPLL)

Two FMPLLs are available on each device.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor and output clock divider ratio are software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 2 modes of operation
  - Normal PLL mode with crystal reference (default)
  - Normal PLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers as well as jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows running motor control periphery at different (precisely lower, equal, or higher, as required) frequency than the system to ensure higher resolution

1.6.11 DRAM controller

The DRAM controller (available only on 473-pin devices) is a multi-port controller that monitors incoming requests on the three AHB slave ports and decides (at each rising clock edge) what command needs to be sent to the external DRAM.

The DRAM controller on this device supports the following types of memories:

- Mobile DDR (mDDR)
- DDR 1
- DDR 2 (optional)
- SDR

The controller has the following features:

- Optimized timing for 32-byte bursts and single read accesses on the AHB interface
- Optimized timing for 8-byte and 16-byte bursts on the DRAMC interface
- Supports priority elevation on the slave ports for single accesses
- 16-bit wide DRAM interface
- One chip select (CS)
- mDDR memory controller
  - 16-bit external interface
  - Address range up to 8 MB

1.6.12 Boot Assist Module (BAM)

- Enables booting via serial mode (FlexCAN, LINFlex)
- Handles static mode in case of an erroneous boot procedure
- Implemented in 8 KB ROM
- Supports Lock Step Mode (LSM) and Decoupled Parallel Mode (DPM)

1.6.13 Parallel Data Interface (PDI)

- Support for external ADC and CMOS image sensors
- Parallel interface operation up to MCU system bus frequency
- Selectable data capture from rising or falling edge
- Receive FIFO with adjustable trigger thresholds
- Data width for 8, 10, 12, 14, and 16 bits
- Data Packing Unit to pack input data on 64-bit words — data packed on 8- or 16- bit boundary, depending on input data width
- Binary increasing channel select that allows as many as eight channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK

1.6.14 Deserial Serial Peripheral Interface (DSPI) modules

- Three serial peripheral interfaces
  - Full duplex communication ports with interrupt and eDMA request support
  - Support for all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis

1.6.20.3 Analog-To-Digital Converter (ADC)

- Four independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V or 0–3.3 V
- Twenty-two single-ended input channels
- Supports eight FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal, or external triggers
- DMA and interrupt request support

1.6.20.4 eTimer module

Three 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Ability to operate up to platform frequency
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality is not in use
- DMA support

1.6.21 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to enable high diagnostic coverage (check of checker)
- Replicated IP to be used as checkers on the PBRIDGE output, Flash Controller output, SRAM output, DMA Channel Mux inputs

1.6.22 Software Watchdog Timer (SWT)

This module implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Fault-tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog

VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc DQS[1]	dramc DM[1]	dramc D[13]	dramc D[12]	N
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc D[14]	dramc D[15]	VSS_HV_ DRAM	VDD_HV_ DRAM	P
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		VDD_HV_ DRAM_VREF	dramc ADD[3]	dramc CKE	dramc CLKB	R
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ADD[8]	dramc ADD[9]	dramc ADD[1]	dramc CLK	T
VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VDD_ LV_COR		dramc ADD[6]	dramc ADD[12]	VDD_HV_ DRAM	dramc ADD[0]	U
VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR		lin0 TXD	dramc ADD[13]	VSS_HV_ DRAM	dramc ADD[2]	V
							lin0 RXD	dramc ADD[14]	dramc ADD[7]	dramc ADD[4]	W
VDD_ HV_IO	adc0_adc1 AN[11]	etimer1 ETC[5]	etimer1 ETC[4]	adc1 AN[8]	adc1 AN[6]	TCK	VDD_HV_IO	dramc ADD[15]	dramc ADD[11]	dramc ADD[5]	Y
adc0 AN[8]	adc0_adc1 AN[12]	adc1 AN[0]	adc1 AN[2]	adc1 AN[5]	adc1 AN[7]	TDI	etimer1 ETC[0]	VSS_HV_IO	lin1 TXD	dramc ADD[10]	AA
adc0 AN[7]	adc0_adc1 AN[13]	adc1 AN[1]	adc1 AN[3]	adc1 AN[4]	TDO	TMS	RESERVED	lin1 RXD	VDD_ HV_IO	VSS_ HV_IO	AB
VSS_ HV_ADR_0	adc0_adc1 AN[14]	VDD_ HV_ADR_1	VSS_ HV_ADR_1	VDD_ HV_PMU	VREG_CTRL	VSS_ HV_PMU	$\overline{\text{RESET}}$_ $\overline{\text{SUP}}$	VREG_INT_ ENABLE	VSS_ HV_IO	VSS_ HV_IO	AC
13	14	15	16	17	18	19	20	21	22	23	

Figure 6. MPC5675K 473 MAPBGA pinout (southeast, viewed from above)

2.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration for this device.

2.2.1 Pad types

Table 2 lists the pad types used on the MPC5675K.

Table 2. Pad types

Pad Type	Description
GP Slow	Slow buffer with CMOS Schmitt trigger and pullup/pulldown.
GP Slow/Fast	Programmable slow/fast buffer with CMOS Schmitt trigger, pullup/pulldown.
GP Slow/Medium	Programmable slow/medium buffer with CMOS Schmitt trigger, pullup/pulldown. Programmable slow/medium buffer with CMOS Schmitt trigger, pullup/pulldown and Injection proof analog switch.
GP Slow/Symmetric	Programmable slow/symmetric buffer with CMOS Schmitt trigger, pullup/pulldown.
PDI Medium	Medium slew-rate output with four selectable slew rates. Contains an input buffer and weak pullup/pulldown.
PDI Fast	Fast slew-rate output with four selectable slew rates. Contains an input buffer and weak pullup/pulldown.

Table 2. Pad types (continued)

Pad Type	Description
DRAM ACC	Bidirectional DDR pad. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM CLK	Differential clock driver.
DRAM DQ	Bidirectional DDR pad with integrated ODT. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM ODT CTL	Enable On Die Termination control.
Analog	CMOS Schmitt trigger cell with injection proof analog switch.
Analog Shared	CMOS Schmitt trigger cell with two injection-proof analog switches.

2.2.2 Power supply and reference voltage pins

Table 3 shows the supply pins for the MPC5675K in the 257 MAPBGA package. Table 5 shows the supply pins for the MPC5675K in the 473 MAPBGA package.

Table 4 and Table 6 show the pins not populated on the MPC5675K 257 MAPBGA and 473 MAPBGA packages, respectively.

Table 3. 257 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F9	VDD_LV_COR	VDD_LV
A9	VDD_HV_IO	VDD_HV	F10	VDD_LV_COR	VDD_LV
B16	VDD_HV_IO	VDD_HV	F11	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F12	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	G12	VDD_LV_COR	VDD_LV
P10	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
P14	VDD_HV_IO	VDD_HV	H12	VDD_LV_COR	VDD_LV
T2	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T16	VDD_HV_IO	VDD_HV	J12	VDD_LV_COR	VDD_LV
L14	VDD_HV_DRAM_VREF	VDD_HV	K6	VDD_LV_COR	VDD_LV
D8	VDD_HV_FLA	VDD_HV	K12	VDD_LV_COR	VDD_LV
M1	VDD_HV_OSC	VDD_HV	L6	VDD_LV_COR	VDD_LV
D14	VDD_HV_PDI	VDD_HV	L12	VDD_LV_COR	VDD_LV
H16	VDD_HV_PDI	VDD_HV	M6	VDD_LV_COR	VDD_LV
U14	VDD_HV_PMU	VDD_HV	M7	VDD_LV_COR	VDD_LV
R7	VDD_HV_ADR_13	VDD_HV_A	M8	VDD_LV_COR	VDD_LV

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
D1	GPIO	nexus MDO[2][1]	A0: siul_GPIO[85] A1: _ A2: npc_wrapper_MDO[2] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D2	GPIO	nexus MDO[3][1]	A0: siul_GPIO[84] A1: _ A2: npc_wrapper_MDO[3] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D3	GPIO	can1 RXD	A0: siul_GPIO[15] A1: _ A2: _ A3: _	I: can1_RXD I: can0_RXD I: siul_EIRQ[14]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D4	GPIO	dspi0 SOUT	A0: siul_GPIO[38] A1: dspi0_SOUT A2: _ A3: sscm_DEBUG[6]	I: _ I: _ I: siul_EIRQ[24]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D6	GPIO	etimer0 ETC[5]	A0: siul_GPIO[44] A1: etimer0_ETC[5] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D7	GPIO	etimer0 ETC[4]	A0: siul_GPIO[43] A1: etimer0_ETC[4] A2: _ A3: _	I: _ I: mc_rgm_ABS[0] I: _	—	pulldown	GP Slow/ Medium	VDD_HV_IO
D10	GPIO	fec TXD[2]	A0: siul_GPIO[203] A1: fec_TXD[2] A2: _ A3: _	I: flexpwm1_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D11	GPIO	fec TXD[1]	A0: siul_GPIO[202] A1: fec_TXD[1] A2: _ A3: dspi2_SCK	I: flexpwm1_FAULT[0] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D12	GPIO	fec RX_DV	A0: siul_GPIO[210] A1: flexray_DBG3 A2: etimer2_ETC[0] A3: dspi0_CS7	I: fec_RX_DV I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
J17	GPIO	flexpwm0 X[1]	A0: siul_GPIO[195] A1: flexpwm0_X[1] A2: ebi_AD29 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K1	GPIO	nexus MSEO_B[0][1]	A0: siul_GPIO[89] A1: _ A2: npc_wrapper_MSEO_B[0] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K2	GPIO	nexus MSEO_B[1][1]	A0: siul_GPIO[88] A1: _ A2: npc_wrapper_MSEO_B[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K3	GPIO	nexus RDY_B	A0: siul_GPIO[216] A1: _ A2: nexus_RDY_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
K4	GPIO	dspi0 SIN	A0: siul_GPIO[39] A1: _ A2: _ A3: sscm_DEBUG[7]	I: dspi0_SIN I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
K14	GPIO	flexpwm0 X[2]	A0: siul_GPIO[196] A1: flexpwm0_X[2] A2: ebi_AD30 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K15	GPIO	flexpwm0 X[3]	A0: siul_GPIO[197] A1: flexpwm0_X[3] A2: ebi_AD31 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K16	GPIO	flexpwm0 A[1]	A0: siul_GPIO[149] A1: _ A2: ebi_RD_WR A3: flexpwm0_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
K17	GPIO	flexpwm0 B[0]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
B4	GPIO	can1 TXD	A0: siul_GPIO[14] A1: can1_TXD A2: _ A3: _	I: _ I: _ I: siul_EIRQ[13]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B5	GPIO	nexus MDO[14][1]	A0: siul_GPIO[219] A1: _ A2: npc_wrapper_MDO[14] A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
B6	GPIO	dspi2 CS1	A0: siul_GPIO[9] A1: dspi2_CS1 A2: _ A3: _	I: flexpwm0_FAULT[0] I: lin3_RXD I: can2_RXD	—	disabled	GP Slow/ Medium	VDD_HV_IO
B7	GPIO	flexray CB_TR_EN	A0: siul_GPIO[52] A1: flexray_CB_TR_EN A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B8	GPIO	flexray CA_TX	A0: siul_GPIO[48] A1: flexray_CA_TX A2: _ A3: _	I: ctu1_EXT_IN I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B9	GPIO	fec RXD[3]	A0: siul_GPIO[214] A1: i2c1_data A2: _ A3: _	I: fec_RXD[3] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B10	GPIO	fec RX_ER	A0: siul_GPIO[215] A1: _ A2: _ A3: dspi0_CS1	I: fec_RX_ER I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B11	GPIO	fec TXD[0]	A0: siul_GPIO[201] A1: fec_TXD[0] A2: etimer2_ETC[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B12	GPIO	fec RXD[0]	A0: siul_GPIO[211] A1: i2c1_clock A2: _ A3: _	I: fec_RXD[0] I: _ I: siul_EIRQ[27]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
U20	GPIO	dramc ADD[6]	A0: siul_GPIO[164] A1: dramc_ADD[6] A2: ebi_ADD14 A3: flexpwm1_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U21	GPIO	dramc ADD[12]	A0: siul_GPIO[170] A1: dramc_ADD[12] A2: ebi_AD4 A3: ebi_ADD20	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U23	GPIO	dramc ADD[0]	A0: siul_GPIO[158] A1: dramc_ADD[0] A2: ebi_ADD8 A3: ebi_CS2	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V3	GPIO	flexpwm1 B[2]	A0: siul_GPIO[124] A1: flexpwm1_B[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V4	GPIO	dspi1 CS2	A0: siul_GPIO[56] A1: dspi1_CS2 A2: _ A3: dspi0_CS5	I: flexpwm0_FAULT[3] I: lin2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
V20	GPIO	lin0 TXD	A0: siul_GPIO[18] A1: lin0_TXD A2: i2c0_clock A3: sscm_DEBUG[2]	I: _ I: _ I: siul_EIRQ[17]	—	disabled	GP Slow/ Medium	VDD_HV_IO
V21	GPIO	dramc ADD[13]	A0: siul_GPIO[171] A1: dramc_ADD[13] A2: ebi_AD5 A3: ebi_ADD21	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
V23	GPIO	dramc ADD[2]	A0: siul_GPIO[160] A1: dramc_ADD[2] A2: ebi_ADD10 A3: ebi_TA	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
W3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AB15	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR1
AB16	ANA	adc1 AN[3]	—	siul_GPI[32]	AN: adc1_AN[3]	—	Analog	VDD_HV_ADR1
AB17	ANA	adc1 AN[4]	—	siul_GPI[75]	AN: adc1_AN[4]	—	Analog	VDD_HV_ADR1
AB18	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
AB21	GPIO	lin1 RXD	A0: siul_GPIO[95] A1: _ A2: i2c1_data A3: _	I: lin1_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC3	GPIO	dspi2 SIN	A0: siul_GPIO[13] A1: _ A2: _ A3: _	I: dspi2_SIN I: flexpwm0_FAULT[0] I: siul_EIRQ[12]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC4	GPIO	flexpwm1 A[3]	A0: siul_GPIO[126] A1: flexpwm1_A[3] A2: etimer2_ETC[4] A3: dspi0_CS7	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC5	GPIO	flexpwm1 B[3]	A0: siul_GPIO[127] A1: flexpwm1_B[3] A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC6	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	GP Slow/ Medium	VDD_HV_ADR23
AC9	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR23

In case of only narrow band disturbances the maximum of the results will not change. In case of broadband signals the emission has to be below the limits.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	750 (corners) 500	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Power Management Controller (PMC) electrical characteristics

3.8.1 PMC electrical specifications

This section contains electrical characteristics for the PMC.

Table 18. VRC SMPS recommended external devices

Reference designator	Part description	Part type	Nominal	Description
Ca	—	capacitor	20 µF, 20 V	Filter capacitor
Cb	—	capacitor	0.1 µF, 20 V	Filter capacitor
Cd	—	capacitor	20 µF, 20 V	Supply decoupling cap, ESR < 50 mΩ, as close to PMOS source as possible
Ce	—	capacitor	0.1 µF, 16 V	Ceramic
Cl	—	capacitor	20 µF, 16 V	Buck capacitor, total ESR < 100 mΩ, as close to the coil as possible
D	SS8P3L	Schottky	—	Vishay low Vf Schottky diode
L	—	inductor	4 µH, 1.5 A	Buck shielded coil low ESR
Q	FDC642P or SQ2301ES or SI3443DV	pMOS	2 A, 10 V	Low threshold PMOS V_{th} < 1.5 V, R_{dson}@4.5 V < 120 mΩ, Q_g < 16 nC
R	—	resistor	50–100 kΩ	Pullup for power PMOS gate

3.9 Supply current characteristics

Table 19. Current consumption characteristics[1]

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	I_{DD_LV}	CC	Maximum run I_{DD} (incl. digital core logic and analog block of the LV rail)	V_{DD_LV} = 1.36 V, f_{Core} = 180 MHz, 1:2 mode, DPM, both cores executing EMC test code, internal VREG mode, all caches enabled, code execution of core 0 from code flash 0, code execution of core 1 from code flash 1, FMPLL_1 active at 120 MHz.	—	600	900	mA
2	$I_{DD\_LV\_PLL}$	CC	Maximum run I_{DD} for each PLL[2]	$V_{DD\_LV\_PLL}$ = 1.36 V, f_{VCO} running at maximum frequency.	—	1.5	2	mA
3	$I_{DD\_HV\_FLA}$[3]	CC	Maximum run I_{DD} Flash	$V_{DD\_HV\_FLA}$ = 3.6 V, DPM, both cores executing EMC test code, code execution of core 0 from code flash 0, code execution of core 1 from code flash 1.	—	20	30	mA
4	$I_{DD\_HV\_OSC}$	CC	Maximum run I_{DD} OSC	f_{OSC} 4 MHz to 40 MHz, $V_{DD\_HV\_OSC}$ 3.6 V	—	1	3	mA
5	$I_{DD\_HV\_ADV}$	CC	Maximum run I_{DD} for each ADC[4]	$V_{DD\_HV\_ADV}$ = 3.6 V	—	2	4	mA
6	$I_{DD\_HV\_ADR02}$[5]	CC	Maximum reference I_{DD}[6]	ADC0 powered on[7]	—	—	2	mA
				ADC2 powered on	—	—	1.2	mA
7	$I_{DD\_HV\_ADR13}$[5]	CC	Maximum reference I_{DD}[6]	ADC1 powered on	—	—	1.2	mA
				ADC3 powered on	—	—	1.2	mA
8	$I_{DD\_HV\_ADR0}$[8]	CC	Maximum reference I_{DD}	ADC0 powered on[7]	—	—	2	mA

Table 19. Current consumption characteristics[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
9	$I_{DD\_HV\_ADR1}$[8]	CC	Maximum reference I_{DD}	ADC1 powered on	—	—	1.2	mA
10	$I_{DD\_HV\_ADR23}$[8]	CC	Maximum reference I_{DD}[6]	ADC2 powered on	—	—	1.2	mA
				ADC3 powered on	—	—	1.2	mA

1 Applies to T_J = –40 °C to 150 °C.
2 Total current on $I_{DD\_LV\_PLL}$ needs to be multiplied with the number of active PLLs.
3 The current specified for Idd_HV_FLA includes current consumed during programming and erase operations.
4 Total current on $I_{DD\_HV\_ADV}$ needs to be multiplied with the number of active ADCs.
5 257 MAPBGA only.
6 Total current on $I_{DD\_HV\_ADRxx}$ is the sum of both references if both ADCs are powered on.
7 ADC0 includes 0.7 mA dissipation for the temperature sensor (TSENS).
8 473 MAPBGA only.

3.10 Temperature sensor electrical characteristics

Table 20. Temperature sensor electrical characteristics

Symbol			Parameter	Conditions	Min	Max	Unit
1	—	P	Accuracy	T_J = –40 °C to T_A = 125 °C	–10	10	°C
2	T_S	D	Minimum sampling period	—	4	—	µs

3.11 Main oscillator electrical characteristics

The MPC5675K provides an oscillator/resonator driver.

Table 21. Main oscillator electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
1	F_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
2a	$T_{XOSCHSSU}$	CC	Oscillator start-up time	f_{OSC} < 16 MHz	—	6	10	ms
2b				f_{OSC} = 16 MHz to 40 MHz	—	2	4	
3	V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
4	V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1 V_{DD} = 3.0 V to 3.6 V, T_J = –40 to 150 °C, unless otherwise specified.

3.15.2 Read access timing

Table 28. Code flash read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{READ}	CC	Maximum frequency for Flash reading (system clock frequency SYS_CLK)	4 wait states	90	MHz
2				3 wait states	60	MHz

Table 29. Data flash read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{READ}	CC	Maximum frequency for Flash reading (system clock frequency SYS_CLK)	12 wait states	90	MHz
2				8 wait states	60	MHz

3.15.3 Write access timing

Table 30. Code flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	—	90	MHz

Table 31. Data flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	—	90	MHz

3.16 SRAM memory electrical characteristics

Table 32. System SRAM memory read/write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	$s_{READ/WRITE}$	CC	Maximum frequency for system SRAM reading/writing (system clock frequency SYS_CLK)	1 wait state	90	MHz

Table 38. PDI pads AC electrical characteristics

No.	Name	Prop. Delay (ns) L → H/H → L[1]		Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	PDI Medium	0.8/0.7 -------- 1.1/1.08	5.5/4.5	1.02/1	—	50	11
			12/8.3	3.5/2.3		200	
			49/22	9.1/6		50	10
			60/31	14/9.2		200	
			102/44	18/12		50	01
			119/53	24/16		200	
			722/302	126/85		50	00
			772/325	136/90		200	
2	PDI Fast	0.8/0.7 -------- 1.1/1.08	10/10	1.1/1.1	—	50	11
			15/15	2.6/2.6		200	
			15/15	2.4/2.4		50	10
			22/22	5/5		200	
			24/24	5/5		50	01
			33/33	8/8		200	
			66/66	16/16		50	00
			84/84	21/21		200	

[1] L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19 DRAM pad specifications

This section specifies the electrical characteristics of the DRAM pads. Please refer to the tables in Section 2.2, Pin descriptions, for a cross reference between package pins and pad types.

DRAM pads feature list:

- Driver
  - Configurable to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR modes.
  - VDD_HV_DRAM range of
    - 1.8 V nominal
    - 2.5 V nominal
    - 3.3 V nominal
- Receiver
  - Differential or pseudo-differential input buffer in all DRAM pads
  - All inputs are tolerant up to their VDD_HV_DRAM absolute maximum rating
  - Data and strobe pads can be configured to support four signal termination options
    - Infinite/no termination
    - 50 Ω
    - 75 Ω

3.21.2 Reset sequence description

The figures in this section show the internal states of the MPC5675K during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 52. The start point and end point conditions as well as the reset trigger mapping to the different reset sequences is specified in Section 3.21.3, Reset sequence trigger mapping.

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the MPC5675K during the execution of the reset sequence and the possible states of the $\overline{\text{RESET}}$ signal pin.

NOTE

$\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the MPC5675K internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 52 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

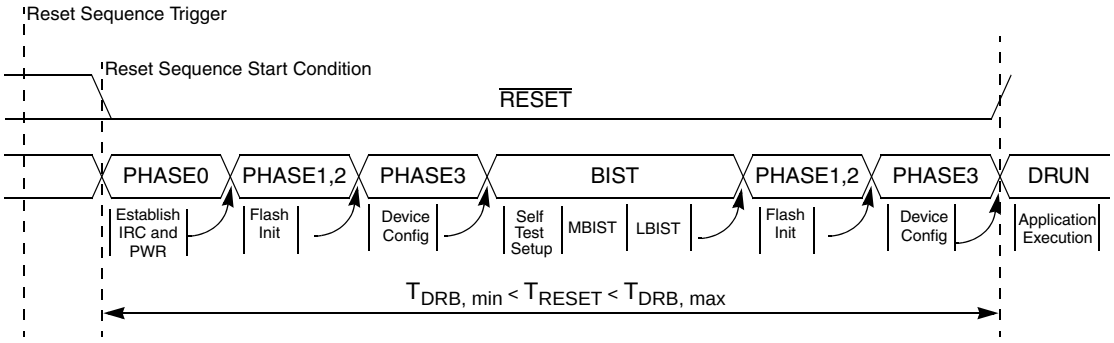

Figure 12. Destructive reset sequence, BIST enabled

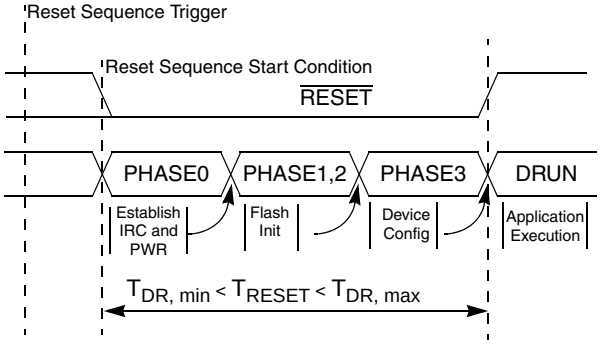

Figure 13. Destructive reset sequence, BIST disabled

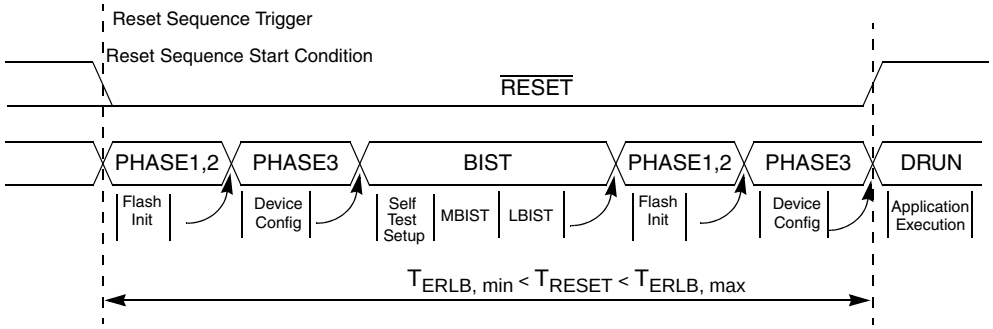

Figure 14. External reset sequence long, BIST enabled

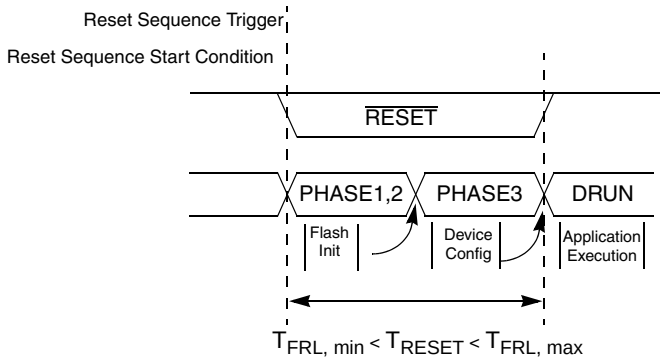

Figure 15. Functional reset sequence long

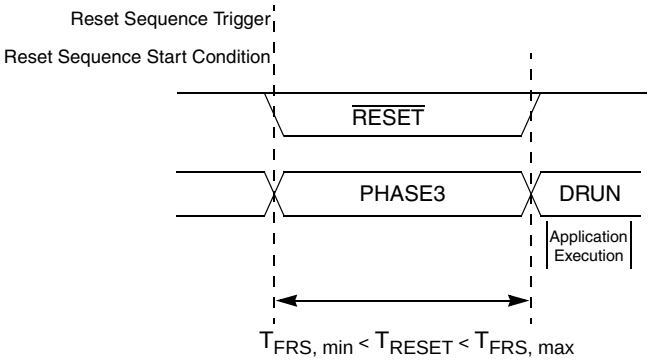

Figure 16. Functional reset sequence short

The reset sequences shown in Figure 15 and Figure 16 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence. See the RGM_FBRE register in the *MPC5675K Reference Manual* for more information.

3.21.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences, depending on the VREG mode (external or internal). It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 52.

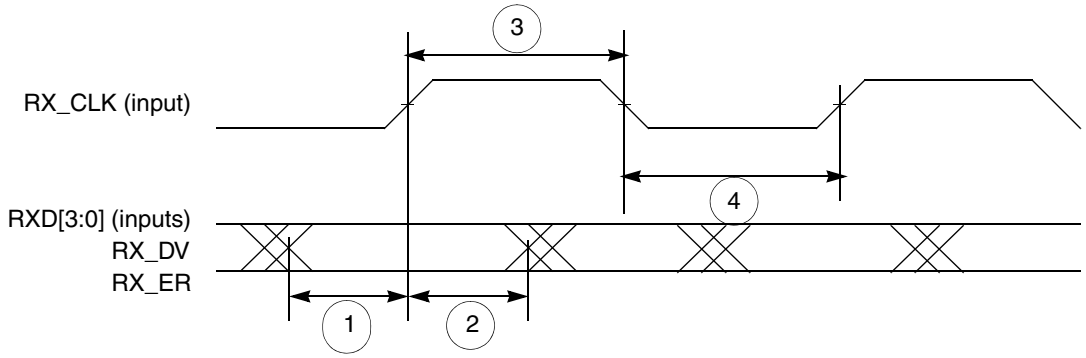

Figure 45. MII receive signal timing diagram

3.22.8.2 MII transmit signal timing (TXD[3:0], TX_EN, TX_ER, TX_CLK)

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency.

The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 67. MII transmit signal timing[1]

No.	Parameter	Min	Max	Unit
5	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
7	TX_CLK pulse width high	40%	60%	TX_CLK period
8	TX_CLK pulse width low	40%	60%	TX_CLK period

[1] Output pads configured with SRC = 0b11.

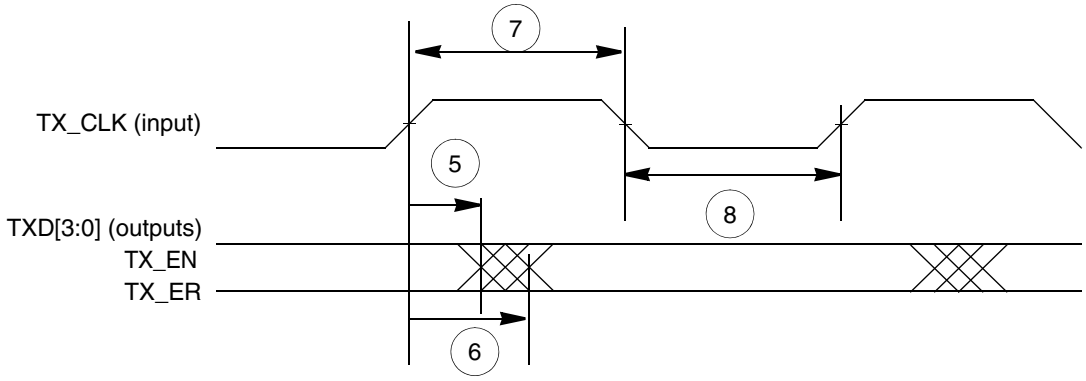

Figure 46. MII transmit signal timing diagram

3.22.8.3 MII async inputs signal timing (CRS and COL)

Table 68. MII async inputs signal timing[1]

No.	Parameter	Min	Max	Unit
9	CRS, COL minimum pulse width	1.5	—	TX_CLK period

[1] Output pads configured with SRC = 0b11.

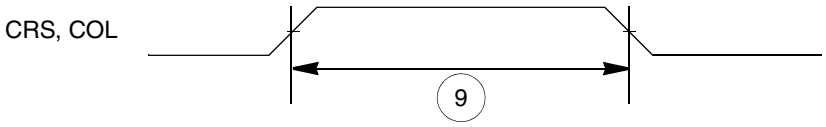

Figure 47. MII async inputs timing diagram

3.22.8.4 MII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 5 MHz.

Table 69. MII serial management channel timing[1]

No.	Parameter	Min	Max	Unit
10	MDC falling edge to MDIO output invalid (minimum propagation delay)	0	—	ns
11	MDC falling edge to MDIO output valid (max prop delay)	—	25	ns
12	MDIO (input) to MDC rising edge setup	10	—	ns
13	MDIO (input) to MDC rising edge hold	0	—	ns
14	MDC pulse width high	40%	60%	MDC period
15	MDC pulse width low	40%	60%	MDC period

[1] Output pads configured with SRC = 0b11.

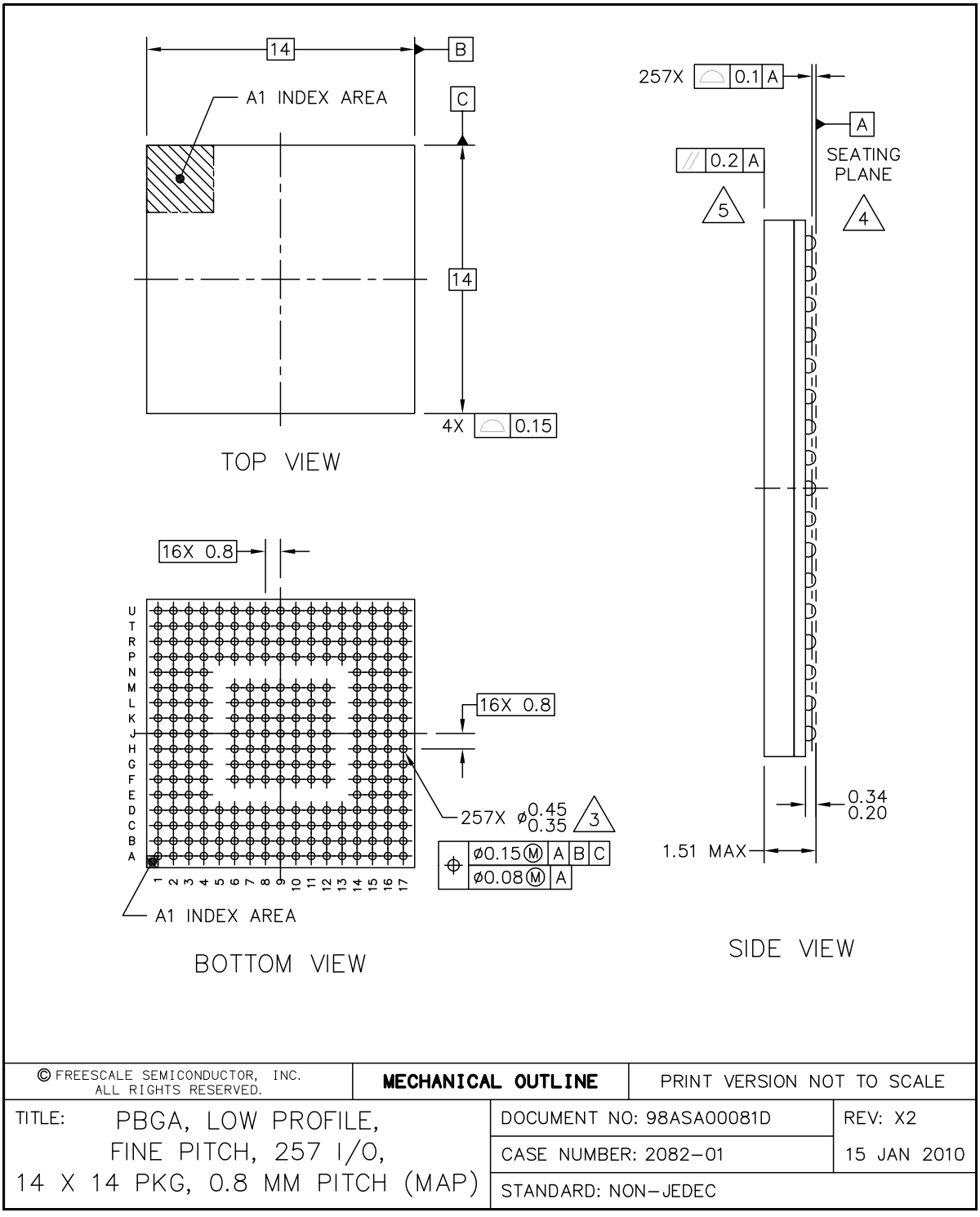

Figure 54. 257 MAPBGA mechanical data (1 of 2)