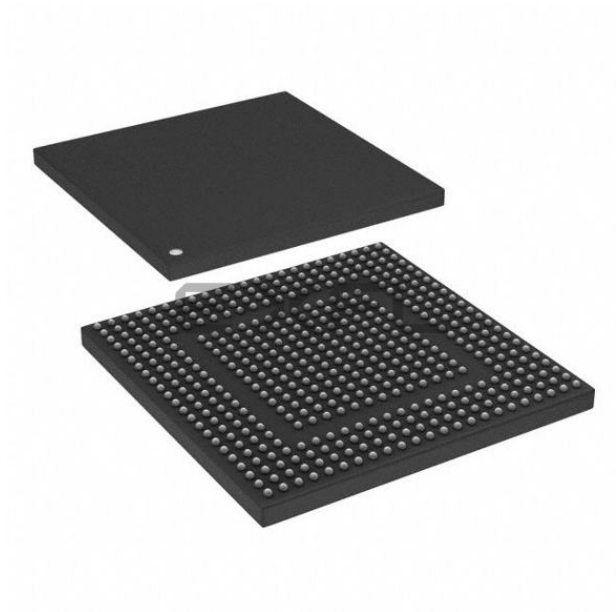

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5674kff0vms2r

Table 1. MPC5675K family device comparison (continued)

Features		MPC5673K	MPC5674K	MPC5675K
Packages	MAPBGA	257 pins 473 pins		
Temperature	Ambient	See the T_A recommended operating condition in the device data sheet		

1 Sphere of Replication.

2 Does not include Test or Shadow Flash memory space.

3 DSPI_0 and DSPI_1.

4 DSPI_0 has 8 chip selects; DSPI_1 and DSPI_2 have 4 chip selects each.

5 Available only on 473-pin package.

6 I2C_0 and I2C_1.

7 LinFlex_0, LinFlex_1, and LinFlex_2.

8 DDR available only on 473 package. Other modules available as follows:
EBI or DDR on 473 package
EBI + PDI on 473 package
DDR + PDI on 473 package
PDI only on 257 package

- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM is supported
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for:
  - buffered output compare functions
  - input capture functions
- Enhanced dual-edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high and low limit registers
- Supports safety measures using DMA

1.6.20.2 Cross Triggering Unit (CTU)

The CTU provides automatic generation of ADC conversion requests on user-selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double-buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Maximum operating frequency lower than or equal to platform
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low-pass filter
- Double-buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double-buffered ADC command list pointers to minimize ADC trigger unit update
- Double-buffered ADC conversion command list with as many as twenty-four ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows controlling ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.6.26 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter is available to support high priority core exceptions.

1.6.27 System Status and Configuration Module (SSCM)

The SSCM on the MPC5675K features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid reset configuration halfword
- Sets up the MMU to allow user boot code to execute as either Classic Power Architecture Book E code (default) or as Freescale VLE code out of flash
- Supports serial bootloading of either Classic Power Architecture Book E code (default) or Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid

1.6.28 Nexus Development Interface (NDI)

- Per IEEE-ISTO 5001-2008
- Real-time development support for Power Architecture core through Nexus class 3 (some class 4 support)
- Nexus support to snoop system SRAM traffic
- Data trace of FlexRay accesses
- Read and write access
- Configured via the IEEE 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

1.6.29 IEEE 1149.1 JTAG Controller (JTAGC)

- IEEE 1149.1-2001 Test Access Port (TAP) interface
- JCOMP input that provides the ability to share the TAP —selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
- 5-bit instruction register that supports additional public instructions
- Three test data registers:
  - Bypass register
  - Boundary scan register
  - Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register, and associated circuitry

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_ HV_IO	VSS_ HV_IO	VDD_ HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	fec RX_DV	fec MDIO	fec TX_CLK	fec TX_EN
B	VSS_ HV_IO	VSS_ HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO[14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	fec RXD[3]	fec RX_ER	fec TXD[0]	fec RXD[0]
C	VDD_ HV_IO	nexus MDO[15]	VSS_ HV_IO	FCCU_ F[1]	flexray CB_RX	etimer0 ETC[4]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	fec TXD[2]	fec TXD[1]	fec CRS
D	nexus MDO[1]	nexus MDO[3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[0]	VDD_ HV_IO	VSS_ HV_IO	JCOMP	VSS_ HV_IO	VSS_ HV_FLA
E	nexus MDO[0]	nexus MDO[2]	flexray CA_RX	NMI								
F	nexus MDO[10]	nexus MDO[11]	nexus MDO[6]	nexus MDO[4]		VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR	VDD_ LV_COR
G	nexus MCKO	VDD_ HV_IO	nexus MDO[8]	nexus MSEO_B[1]		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
H	nexus EVTO_B	VSS_ HV_IO	nexus MSEO_B[0]	nexus EVTI_B		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
J	nexus RDY_B	nexus MDO[13]	nexus MDO[12]	dspi1 SIN		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
K	dspi0 SCK	dspi1 CS0	dspi1 SCK	dspi1 SOUT		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
L	dspi0 CS0	dspi2 CS2	dspi2 CS0	VSS_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR
M	flexpwm0 X[0]	VDD_ HV_IO	dspi0 SIN	VDD_ HV_IO		VDD_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR	VSS_ LV_COR

Figure 3. MPC5675K 473 MAPBGA pinout (northwest, viewed from above)

2.2.4 Multiplexed pins

Table 9 shows the pin multiplexing for the MPC5675K in the 257 MAPBGA package. Table 10 shows the pin multiplexing for the MPC5675K in the 473 MAPBGA package.

Table 9. 257 MAPBGA pin multiplexing

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
A4	GPIO	nexus MDO[5][1]	A0: siul_GPIO[114] A1: _ A2: npc_wrapper_MDO[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A5	GPIO	nexus MDO[7][1]	A0: siul_GPIO[112] A1: _ A2: npc_wrapper_MDO[7] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A6	GPIO	nexus MDO[9][1]	A0: siul_GPIO[110] A1: _ A2: npc_wrapper_MDO[9] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A7	GPIO	flexray CB_TX	A0: siul_GPIO[51] A1: flexray_CB_TX A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A8	GPIO	flexray CA_TR_EN	A0: siul_GPIO[47] A1: flexray_CA_TR_EN A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A10	GPIO	fec RXD[2]	A0: siul_GPIO[213] A1: _ A2: _ A3: dspi2_SOUT	I: fec_RXD[2] I: _ I: siul_EIRQ[21]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A11	GPIO	fec RX_CLK	A0: siul_GPIO[209] A1: flexray_DBG2 A2: etimer2_ETC[2] A3: dspi0_CS6	I: fec_RX_CLK I: _ I: siul_EIRQ[25]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A12	GPIO	fec RXD[0]	A0: siul_GPIO[211] A1: i2c1_clock A2: _ A3: _	I: fec_RXD[0] I: _ I: siul_EIRQ[27]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
A13	GPIO	fec MDIO	A0: siul_GPIO[198] A1: fec_MDIO A2: _ A3: dspi2_CS0	I: _ I: _ I: siul_EIRQ[28]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A14	GPIO	fec TX_EN	A0: siul_GPIO[200] A1: fec_TX_EN A2: _ A3: lin0_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO
B4	GPIO	can1 TXD	A0: siul_GPIO[14] A1: can1_TXD A2: _ A3: _	I: _ I: _ I: siul_EIRQ[13]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B5	GPIO	nexus MDO[14][1]	A0: siul_GPIO[219] A1: _ A2: npc_wrapper_MDO[14] A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
B6	GPIO	dspi2 CS1	A0: siul_GPIO[9] A1: dspi2_CS1 A2: _ A3: _	I: flexpwm0_FAULT[0] I: lin3_RXD I: can2_RXD	—	disabled	GP Slow/ Medium	VDD_HV_IO
B7	GPIO	flexray CB_TR_EN	A0: siul_GPIO[52] A1: flexray_CB_TR_EN A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B8	GPIO	flexray CA_TX	A0: siul_GPIO[48] A1: flexray_CA_TX A2: _ A3: _	I: ctu1_EXT_IN I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
G3	GPIO	dspi0 SCK	A0: siul_GPIO[37] A1: dspi0_SCK A2: _ A3: sscm_DEBUG[5]	I: flexpwm0_FAULT[3] I: _ I: siul_EIRQ[23]	—	disabled	GP Slow/ Medium	VDD_HV_IO
G4	GPIO	dspi1 SCK	A0: siul_GPIO[6] A1: dspi1_SCK A2: _ A3: _	I: _ I: _ I: siul_EIRQ[6]	—	disabled	GP Slow/ Medium	VDD_HV_IO
G14	GPIO	pdi DATA[9]	A0: siul_GPIO[140] A1: flexpwm2_X[2] A2: _ A3: _	I: pdi_DATA[9] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G15	GPIO	pdi DATA[10]	A0: siul_GPIO[141] A1: flexpwm2_X[3] A2: _ A3: _	I: pdi_DATA[10] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G16	GPIO	pdi DATA[11]	A0: siul_GPIO[142] A1: flexpwm2_X[0] A2: _ A3: _	I: pdi_DATA[11] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G17	GPIO	pdi FRAME_V	A0: siul_GPIO[130] A1: _ A2: _ A3: _	I: pdi_FRAME_V I: lin2_RXD I: flexpwm2_FAULT[1]	—	disabled	PDI Medium	VDD_HV_PDI
H1	GPIO	nexus MDO[10][1]	A0: siul_GPIO[109] A1: _ A2: npc_wrapper_MDO[10] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
H3	GPIO	dspi0 CS0	A0: siul_GPIO[36] A1: dspi0_CS0 A2: _ A3: sscm_DEBUG[4]	I: _ I: _ I: siul_EIRQ[22]	—	disabled	GP Slow/ Medium	VDD_HV_IO
H4	GPIO	dspi1 CS0	A0: siul_GPIO[5] A1: dspi1_CS0 A2: _ A3: dspi0_CS7	I: _ I: _ I: siul_EIRQ[5]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
A13	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	pdi DATA[3]	A0: siul_GPIO[134] A1: flexpwm2_X[1] A2: _ A3: _	I: pdi_DATA[3] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A16	GPIO	pdi DATA[1]	A0: siul_GPIO[132] A1: flexpwm2_B[3] A2: _ A3: _	I: pdi_DATA[1] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A17	GPIO	pdi CLOCK	A0: siul_GPIO[128] A1: flexpwm2_B[1] A2: _ A3: etimer1_ETC[3]	I: pdi_CLOCK I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A18	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A19	GPIO	pdi DATA[10]	A0: siul_GPIO[141] A1: flexpwm2_X[3] A2: _ A3: _	I: pdi_DATA[10] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A20	GPIO	pdi DATA[13]	A0: siul_GPIO[144] A1: pdi_SENS_SEL[2] A2: ctu1_EXT_TGR A3: _	I: pdi_DATA[13] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
A21	GPIO	pdi DATA[15]	A0: siul_GPIO[146] A1: pdi_SENS_SEL[0] A2: i2c2_data A3: _	I: pdi_DATA[15] I: ctu1_EXT_IN I: _	—	disabled	PDI Medium	VDD_HV_PDI
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
D1	GPIO	nexus MDO[1][1]	A0: siul_GPIO[86] A1: _ A2: npc_wrapper_MDO[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D2	GPIO	nexus MDO[3][1]	A0: siul_GPIO[84] A1: _ A2: npc_wrapper_MDO[3] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
D3	GPIO	can1 RXD	A0: siul_GPIO[15] A1: _ A2: _ A3: _	I: can1_RXD I: can0_RXD I: siul_EIRQ[14]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D4	GPIO	dspi0 SOUT	A0: siul_GPIO[38] A1: dspi0_SOUT A2: _ A3: sscm_DEBUG[6]	I: _ I: _ I: siul_EIRQ[24]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D6	GPIO	etimer0 ETC[5]	A0: siul_GPIO[44] A1: etimer0_ETC[5] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D7	GPIO	etimer0 ETC[0]	A0: siul_GPIO[0] A1: etimer0_ETC[0] A2: _ A3: _	I: dspi2_SIN I: _ I: siul_EIRQ[0]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D14	GPIO	fec RXD[2]	A0: siul_GPIO[213] A1: _ A2: _ A3: dspi2_SOUT	I: fec_RXD[2] I: _ I: siul_EIRQ[21]	—	disabled	GP Slow/ Medium	VDD_HV_IO
D15	GPIO	fec MDC	A0: siul_GPIO[199] A1: fec_MDC A2: _ A3: _	I: _ I: lin1_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D18	GPIO	pdi DATA[11]	A0: siul_GPIO[142] A1: flexpwm2_X[0] A2: _ A3: _	I: pdi_DATA[11] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
Y9	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y10	GPIO	etimer1 ETC[2]	A0: siul_GPIO[46] A1: etimer1_ETC[2] A2: ctu0_EXT_TGR A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y11	GPIO	etimer1 ETC[3]	A0: siul_GPIO[92] A1: etimer1_ETC[3] A2: _ A3: _	I: ctu1_EXT_IN I: mc_rgm_FAB I: siul_EIRQ[30]	—	pulldown	GP Slow/ Medium	VDD_HV_IO
Y14	ANA	adc0_adc1 AN[11]	—	siul_GPI[25]	AN: adc0_adc1_AN[11]	—	Analog Shared	VDD_HV_ADR0
Y15	GPIO	etimer1 ETC[5]	A0: siul_GPIO[78] A1: etimer1_ETC[5] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[26]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y16	GPIO	etimer1 ETC[4]	A0: siul_GPIO[93] A1: etimer1_ETC[4] A2: ctu1_EXT_TGR A3: _	I: _ I: _ I: siul_EIRQ[31]	—	disabled	GP Slow/ Medium	VDD_HV_IO
Y17	ANA	adc1 AN[8]	—	siul_GPI[74]	AN: adc1_AN[8]	—	Analog	VDD_HV_ADR1
Y18	ANA	adc1 AN[6]	—	siul_GPI[76]	AN: adc1_AN[6]	—	Analog	VDD_HV_ADR1
Y21	GPIO	dramc ADD[15]	A0: siul_GPIO[173] A1: dramc_ADD[15] A2: ebi_AD7 A3: ebi_ADD23	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AA14	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR0
AA15	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR1
AA16	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR1
AA17	ANA	adc1 AN[5]	—	siul_GPI[64]	AN: adc1_AN[5]	—	Analog	VDD_HV_ADR1
AA18	ANA	adc1 AN[7]	—	siul_GPI[73]	AN: adc1_AN[7]	—	Analog	VDD_HV_ADR1
AA19	GPIO	TDI	A0: siul_GPIO[21] A1: _ A2: _ A3: _	I: jtagc_TDI I: _ I: _	—	pullup	GP Slow/ Medium	VDD_HV_IO
AA20	GPIO	etimer1 ETC[0]	A0: siul_GPIO[4] A1: etimer1_ETC[0] A2: _ A3: _	I: _ I: _ I: siul_EIRQ[4]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA22	GPIO	lin1 TXD	A0: siul_GPIO[94] A1: lin1_TXD A2: i2c1_clock A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AA23	GPIO	dramc ADD[10]	A0: siul_GPIO[168] A1: dramc_ADD[10] A2: ebi_AD2 A3: ebi_ADD18	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
AB3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO

In case of only narrow band disturbances the maximum of the results will not change. In case of broadband signals the emission has to be below the limits.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	750 (corners) 500	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Power Management Controller (PMC) electrical characteristics

3.8.1 PMC electrical specifications

This section contains electrical characteristics for the PMC.

Table 18. VRC SMPS recommended external devices

Reference designator	Part description	Part type	Nominal	Description
Ca	—	capacitor	20 µF, 20 V	Filter capacitor
Cb	—	capacitor	0.1 µF, 20 V	Filter capacitor
Cd	—	capacitor	20 µF, 20 V	Supply decoupling cap, ESR < 50 mΩ, as close to PMOS source as possible
Ce	—	capacitor	0.1 µF, 16 V	Ceramic
Cl	—	capacitor	20 µF, 16 V	Buck capacitor, total ESR < 100 mΩ, as close to the coil as possible
D	SS8P3L	Schottky	—	Vishay low Vf Schottky diode
L	—	inductor	4 µH, 1.5 A	Buck shielded coil low ESR
Q	FDC642P or SQ2301ES or SI3443DV	pMOS	2 A, 10 V	Low threshold PMOS V_{th} < 1.5 V, R_{dson}@4.5 V < 120 mΩ, Q_g < 16 nC
R	—	resistor	50–100 kΩ	Pullup for power PMOS gate

3.9 Supply current characteristics

Table 19. Current consumption characteristics[1]

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	I_{DD_LV}	CC	Maximum run I_{DD} (incl. digital core logic and analog block of the LV rail)	V_{DD_LV} = 1.36 V, f_{Core} = 180 MHz, 1:2 mode, DPM, both cores executing EMC test code, internal VREG mode, all caches enabled, code execution of core 0 from code flash 0, code execution of core 1 from code flash 1, FMPLL_1 active at 120 MHz.	—	600	900	mA
2	$I_{DD\_LV\_PLL}$	CC	Maximum run I_{DD} for each PLL[2]	$V_{DD\_LV\_PLL}$ = 1.36 V, f_{VCO} running at maximum frequency.	—	1.5	2	mA
3	$I_{DD\_HV\_FLA}$[3]	CC	Maximum run I_{DD} Flash	$V_{DD\_HV\_FLA}$ = 3.6 V, DPM, both cores executing EMC test code, code execution of core 0 from code flash 0, code execution of core 1 from code flash 1.	—	20	30	mA
4	$I_{DD\_HV\_OSC}$	CC	Maximum run I_{DD} OSC	f_{OSC} 4 MHz to 40 MHz, $V_{DD\_HV\_OSC}$ 3.6 V	—	1	3	mA
5	$I_{DD\_HV\_ADV}$	CC	Maximum run I_{DD} for each ADC[4]	$V_{DD\_HV\_ADV}$ = 3.6 V	—	2	4	mA
6	$I_{DD\_HV\_ADR02}$[5]	CC	Maximum reference I_{DD}[6]	ADC0 powered on[7]	—	—	2	mA
				ADC2 powered on	—	—	1.2	mA
7	$I_{DD\_HV\_ADR13}$[5]	CC	Maximum reference I_{DD}[6]	ADC1 powered on	—	—	1.2	mA
				ADC3 powered on	—	—	1.2	mA
8	$I_{DD\_HV\_ADR0}$[8]	CC	Maximum reference I_{DD}	ADC0 powered on[7]	—	—	2	mA

3.17.2 GP pads AC specifications

Table 34. GP pads AC electrical characteristics[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	7	—	40	50
		1	—	6	3	—	12	—	—	40	7	—	40	100
		1	—	6	5	—	18	—	—	25	7	—	40	200
4	Symmetric	1	—	8	1	—	5	—	—	50	3	—	25	25
5	Pullup/down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

3.18 PDI pads specifications

This section specifies the electrical characteristics of the PDI pads. Please refer to the tables in Section 2.2, Pin descriptions, for a cross reference between package pins and pad types.

PDI pads feature list:

- Direction
  - Input
  - Output
  - Bidirectional
- Driver
  - Push/Pull/Open Drain
  - Configurable Four Drive Strengths on Fast driver pads
  - Configurable No Slew-Rate, Slow Slew-Rate, and Fast Slew-Rate on Slow, Medium, and SLR driver pads
  - VDD_HV_PDI NOTE: All pads are NOT 5 V TOLERANT. Pads are not capable of driving to or from voltages above their respective VDD_HV_PDI. In other words, you cannot connect a 3.3V external device to a pad

Table 41. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V) (continued)

No.	Symbol		Parameter	Condition	Min	Max	Unit
5	V_{IL}	CC	Input low voltage	—		$V_{DD\_HV\_DRAM\_VREF}$ – 0.2	V
6	V_{OH}	CC	Output high voltage	—	$V_{DD\_HV\_DRAM\_VTT}$ + 0.8	—	V
7	V_{OL}	CC	Output low voltage	—	—	$V_{DD\_HV\_DRAM\_VTT}$ – 0.8	V

1 BGA473: Termination voltage can be supplied via package pins. BGA257 termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT.

Table 42. Output drive current @ V_{DDE} = 3.3 V (±10%)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	111	–16	16
2	DRAM DQ			
3	DRAM CLK			

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.

2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 43. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Output Slew rate Rise/Fall (V/ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
2	DRAM DQ	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
3	DRAM CLK	1.4/1.4	2.4/2.4	3.1/2.5	5.7/5.7	5	111
		1.6/1.6	2.6/2.6	1.1/1.3	2.3/2.3	20	111

1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19.2 DRAM pads electrical specification ($V_{DD\_HV\_DRAM}$ = 2.5 V)

Table 44. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 2.5 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	2.3	2.7	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	0.49 × $V_{DD\_HV\_DRAM}$	0.51 × $V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V

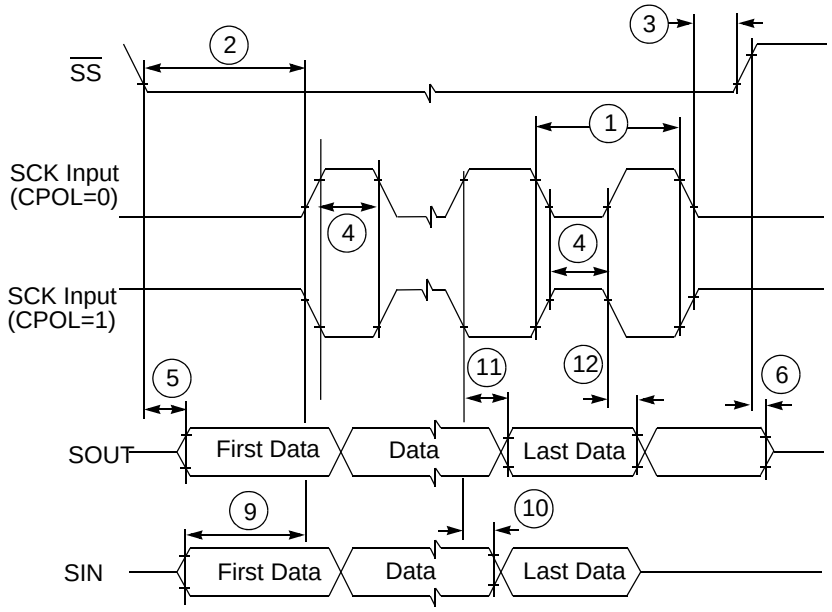

Figure 39. DSPI modified transfer format timing—slave, CPHA = 0

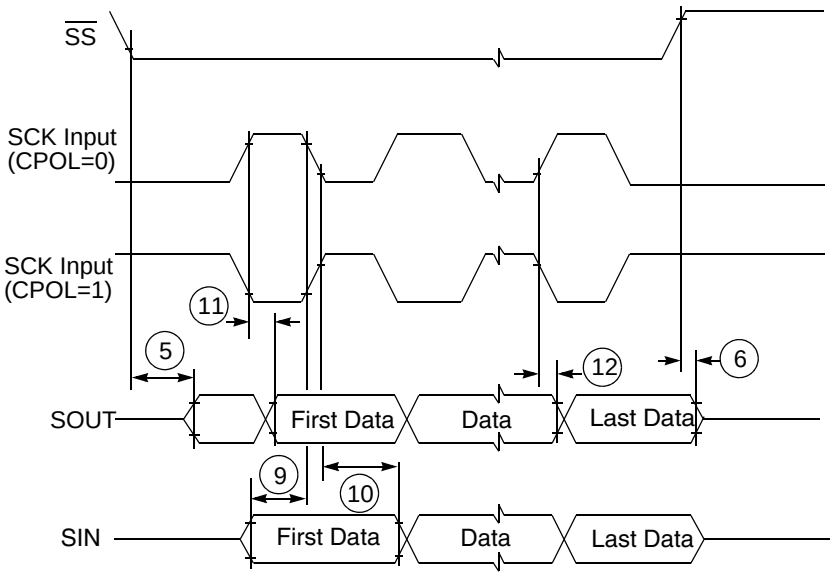

Figure 40. DSPI modified transfer format timing—slave, CPHA = 1

4 Package characteristics

4.1 Package mechanical data

4.1.1 257 MAPBGA

Table 73. Revision history

Revision	Date	Description of Changes
1	6 Oct 2009	Initial release.
2	6 Dec 2009	Updated ball map tables, pin mux tables, supply and system pin tables. Added PMC specifications.
3	2 Jul 2010	Updated ball map tables, pin mux tables, supply and system pin tables. Updated pad specifications. Added reset specifications section.
4	30 Apr 2011	Removed thickness dimension from package diagrams on cover page. Added footnote “Do not connect pin directly to a power supply or ground” for MDO[0:15] and MSEO[0:1] pins to Table 9 (257 MAPBGA pin multiplexing) and Table 10 (473 MAPBGA pin multiplexing). In Table 17 (PMC electrical specifications): • Added minimum and maximum slew rate specifications for LvdReg. • Removed LvdC minimum and maximum hysteresis specifications • Removed HvdC minimum and maximum hysteresis specifications • Corrected HvcD nominal hysteresis from 1.32 to 1.36 In Table 18 (VRC SMPS recommended external devices), updated specifications for device Q (FET). Renamed Section 3.9, Supply current characteristics (was “Power dissipation and current consumption”). Renamed Table 19 (Current consumption characteristics) (was “Power dissipation characteristics”). In Table 19 (Current consumption characteristics): • Updated ADC current consumption to 1.2 mA per ADC plus 0.7 mA (2.0 mA total) for ADC0. • Updated Run I_{DD} to 900 mA max. Updated Accuracy specification in Table 20 (Temperature sensor electrical characteristics): changed “T_J = –40 °C to T_A = 25 °C” to “T_J = –40 °C to T_A = 125 °C,” removed row “T_J = T_A to 125 °C”. In Table 21 (Main oscillator electrical characteristics), added symbol name F_{XOSCHS} for Oscillator frequency specification. Removed “Typical” figures for these specifications. Added footnote “ADC0 includes 0.7 mA dissipation for the temperature sensor (TSENS).” In Table 22 (FMPLL electrical characteristics), added minimum and maximum values for specification f_{FREE}, “Free running frequency.” In Table 23 (RC oscillator electrical characteristics): • Added specification $\Delta_{IRCTRIM}$ “Internal RC oscillator trimming step.” • Removed specification Δ_{RCTRIM} “Post trim accuracy: The variation of the PTF from the 16 MHz” (specification replaced by $\Delta_{IRCTRIM}$ “Internal RC oscillator trimming step”). In Table 24 (ADC conversion characteristics), updated Gain Error (GNE) to “min = –4 max = +4 LSB“ . Added Table 30 (Code flash write access timing) and Table 31 (Data flash write access timing).

Table 73. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.2, Absolute maximum ratings, Table 11 (Absolute maximum ratings), • Deleted footnote to the Max value "Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined." • Added footnote to $V_{DD\_HV\_DRAM}$: "As the $V_{DD\_HV\_DRAM\_VREF}$ supply should always be constrained by the $V_{DD\_HV\_DRAM}$ supply for example through a voltage divider network per the JEDEC specification, the maximum ratings for the $V_{DD\_HV\_DRAM}$ supply should be used for the $V_{DD\_HV\_DRAM\_VREF}$ reference as well." • Changed absolute max rating for $V_{DD\_LV\_PLL}$ from 1.4 to 1.32. • Added footnote to Min value of T_{STG}: "If the ambient temperature is at or above the minimum storage temperature and below the recommended minimum operating temperature, power may be applied to the device safely. However, functionality is not guaranteed and a power cycle must be administered if in internal regulation mode or an assertion of RESET_SUP_B must be administered if in external regulation mode once device enters into the recommended operating temperature range." In Section 3.3, Recommended operating conditions, Table 12 (Recommended operating conditions), • For T_A and T_J, added footnote "When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition." • For T_A, changed the Max temperature spec for the 257 package from 105 to 125 and deleted footnote: "Preliminary data." In Section 3.8.1, PMC electrical specifications, Table 17 (PMC electrical specifications), • No. 4 LvdC and No. 5 HvdC threshold were specified as rising edge and hysteresis. The specification is changed to rising edge / falling edge. • Removed No. 6, VddStepC, and renumbered subsequent lines. In Section 3.9, Supply current characteristics, Table 19 (Current consumption characteristics), added a footnote to No. 3. Idd_HV_FLA. "The current specified for Idd_HV_FLA includes current consumed during programming and erase operations." In Section 3.12, FMPLL electrical characteristics, Table 22 (FMPLL electrical characteristics), replaced "f_{sys}" with "$f_{FMPLLOUT}$" in rows for C_{JITTER}, f_{LCK}, f_{UL}, f_{CS}/f_{DS}, and footnote 9. In Section 3.14.1, Input impedance and ADC accuracy: • Changed "C_S being substantially a switched capacitance..." to "C_S and C_{P2} being substantially a switched capacitance..." • Changed "and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, ..." to "and the sum of $R_S + R_F$, ..." • Changed the equation $$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ to $$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ In Section 3.14.1, Input impedance and ADC accuracy, Table 24 (ADC conversion characteristics), added new spec after line 3 for $t_{ADC\_S\_PMC}$, C: Parameter: Sample time of internal PMC channels. Conditions: - , Min : 717, Typ : - , Max : - , Unit : nS. In Section 3.17.1, GP pads DC specifications, Table 33 (GP pads DC electrical characteristics), added new spec for "Input pad capacitance", No. 21.

Table 73. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.18, PDI pads specifications, Table 36 (PDI pads DC electrical characteristics), added footnote to table: “Over- and undershoots occurring due to impedance mismatch of the external driver and the transmission line at PDI pads in input mode can be allowed up to 0.7 V repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.” In Section 5, Orderable parts, • Removed “3 = 220 MHz” under Operating frequency heading and changed the Operating frequency of the example from “3” to “2”. • Deleted Table 73 (Orderable part number summary**)**.