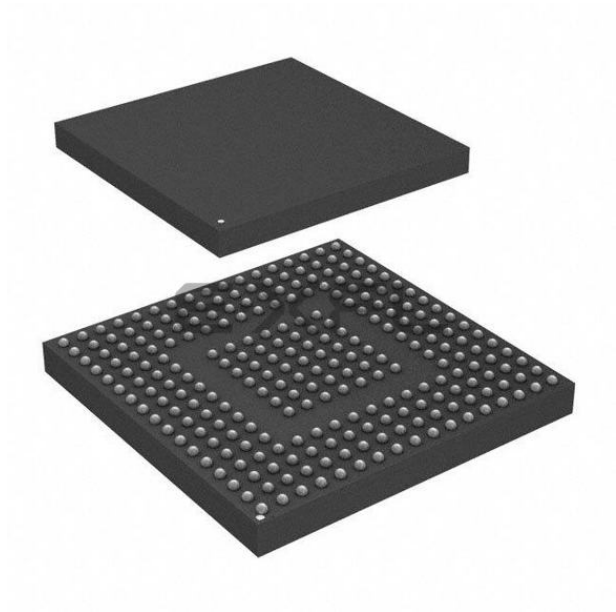

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kff0mmm2

1.6.11 DRAM controller

The DRAM controller (available only on 473-pin devices) is a multi-port controller that monitors incoming requests on the three AHB slave ports and decides (at each rising clock edge) what command needs to be sent to the external DRAM.

The DRAM controller on this device supports the following types of memories:

- Mobile DDR (mDDR)
- DDR 1
- DDR 2 (optional)
- SDR

The controller has the following features:

- Optimized timing for 32-byte bursts and single read accesses on the AHB interface
- Optimized timing for 8-byte and 16-byte bursts on the DRAMC interface
- Supports priority elevation on the slave ports for single accesses
- 16-bit wide DRAM interface
- One chip select (CS)
- mDDR memory controller
  - 16-bit external interface
  - Address range up to 8 MB

1.6.12 Boot Assist Module (BAM)

- Enables booting via serial mode (FlexCAN, LINFlex)
- Handles static mode in case of an erroneous boot procedure
- Implemented in 8 KB ROM
- Supports Lock Step Mode (LSM) and Decoupled Parallel Mode (DPM)

1.6.13 Parallel Data Interface (PDI)

- Support for external ADC and CMOS image sensors
- Parallel interface operation up to MCU system bus frequency
- Selectable data capture from rising or falling edge
- Receive FIFO with adjustable trigger thresholds
- Data width for 8, 10, 12, 14, and 16 bits
- Data Packing Unit to pack input data on 64-bit words — data packed on 8- or 16- bit boundary, depending on input data width
- Binary increasing channel select that allows as many as eight channels to be selected
- Frame synchronization through Vsync, Hsync, PIXCLK

1.6.14 Deserial Serial Peripheral Interface (DSPI) modules

- Three serial peripheral interfaces
  - Full duplex communication ports with interrupt and eDMA request support
  - Support for all functional modes from QSPI submodule of QSMCM (MPC5xx family)
  - Support for queues in RAM
  - Six chip selects, expandable to 64 with external demultiplexers
  - Programmable frame size, baud rate, clock delay, and clock phase on a per-frame basis

- Reception queue possible by setting more than one Rx message buffer with the same ID
- Backwards compatible with previous FlexCAN modules
- Safety CAN features on 1 CAN module as implemented on MPC5604P

1.6.17 Dual-channel FlexRay controller

- Full implementation of FlexRay Protocol Specification 2.1
- Sixty-four configurable message buffers can be handled
- Message buffers configurable as Tx, Rx, or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count, and message ID
- Programmable acceptance filters for RxFIFO message buffers
- Dual channel, each at up to 10 Mbit/s data rate

1.6.18 Periodic Interrupt Timer (PIT)

The PIT module implements the features below:

- Four general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for real time interrupt, clocked from main external oscillator
- Can be used for software tick or DMA trigger operation

1.6.19 System Timer Module (STM)

The STM implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Up-counter with four output compare registers
- OS task protection and hardware tick implementation as per current state-of-the-art AUTOSAR requirement

1.6.20 Motor control (MOTC) peripherals

The peripherals in this section can be used for general-purpose applications, but are specifically designed for motor control (MOTC) applications.

1.6.20.1 FlexPWM

The pulse width modulator module (FlexPWM) contains three PWM channels, each of which is configured to control a single half-bridge power stage. There may also be one or more fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency lower than or equal to platform frequency
- Clock source not modulated and independent from system clock (generated via auxiliary PLL)
- Fine granularity control for enhanced resolution of the PWM period

1.6.26 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter is available to support high priority core exceptions.

1.6.27 System Status and Configuration Module (SSCM)

The SSCM on the MPC5675K features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid reset configuration halfword
- Sets up the MMU to allow user boot code to execute as either Classic Power Architecture Book E code (default) or as Freescale VLE code out of flash
- Supports serial bootloading of either Classic Power Architecture Book E code (default) or Freescale VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid

1.6.28 Nexus Development Interface (NDI)

- Per IEEE-ISTO 5001-2008
- Real-time development support for Power Architecture core through Nexus class 3 (some class 4 support)
- Nexus support to snoop system SRAM traffic
- Data trace of FlexRay accesses
- Read and write access
- Configured via the IEEE 1149.1 (JTAG) port
- High bandwidth mode for fast message transmission
- Reduced bandwidth mode for reduced pin usage

1.6.29 IEEE 1149.1 JTAG Controller (JTAGC)

- IEEE 1149.1-2001 Test Access Port (TAP) interface
- JCOMP input that provides the ability to share the TAP —selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
- 5-bit instruction register that supports additional public instructions
- Three test data registers:
  - Bypass register
  - Boundary scan register
  - Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register, and associated circuitry

Table 5. 473 MAPBGA supply pins (continued)

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
AA21	VSS_HV_IO	VSS_HV	M15	VSS_LV_COR	VSS_LV
AB1	VSS_HV_IO	VSS_HV	M16	VSS_LV_COR	VSS_LV
AB23	VSS_HV_IO	VSS_HV	M17	VSS_LV_COR	VSS_LV
AC1	VSS_HV_IO	VSS_HV	N7	VSS_LV_COR	VSS_LV
AC2	VSS_HV_IO	VSS_HV	N8	VSS_LV_COR	VSS_LV
AC22	VSS_HV_IO	VSS_HV	N9	VSS_LV_COR	VSS_LV
AC23	VSS_HV_IO	VSS_HV	N10	VSS_LV_COR	VSS_LV
AC13	VSS_HV_ADR_0	VSS_HV_A	N11	VSS_LV_COR	VSS_LV
AC16	VSS_HV_ADR_1	VSS_HV_A	N12	VSS_LV_COR	VSS_LV
AC8	VSS_HV_ADR_23	VSS_HV_A	N13	VSS_LV_COR	VSS_LV
AA10	VSS_HV_ADV	VSS_HV_A	N14	VSS_LV_COR	VSS_LV
H23	VSS_HV_DRAM	VSS_HV	N15	VSS_LV_COR	VSS_LV
L22	VSS_HV_DRAM	VSS_HV	N16	VSS_LV_COR	VSS_LV
P22	VSS_HV_DRAM	VSS_HV	N17	VSS_LV_COR	VSS_LV
V22	VSS_HV_DRAM	VSS_HV	P7	VSS_LV_COR	VSS_LV
D12	VSS_HV_FLA	VSS_HV	P8	VSS_LV_COR	VSS_LV
Y1	VSS_HV_OSC	VSS_HV	P9	VSS_LV_COR	VSS_LV
C21	VSS_HV_PDI	VSS_HV	P10	VSS_LV_COR	VSS_LV
D17	VSS_HV_PDI	VSS_HV	P11	VSS_LV_COR	VSS_LV
G7	VSS_LV_COR	VSS_LV	P12	VSS_LV_COR	VSS_LV
G8	VSS_LV_COR	VSS_LV	P13	VSS_LV_COR	VSS_LV
G9	VSS_LV_COR	VSS_LV	P14	VSS_LV_COR	VSS_LV
G10	VSS_LV_COR	VSS_LV	P15	VSS_LV_COR	VSS_LV
G11	VSS_LV_COR	VSS_LV	P16	VSS_LV_COR	VSS_LV
G12	VSS_LV_COR	VSS_LV	P17	VSS_LV_COR	VSS_LV
G13	VSS_LV_COR	VSS_LV	R7	VSS_LV_COR	VSS_LV
G14	VSS_LV_COR	VSS_LV	R8	VSS_LV_COR	VSS_LV
G15	VSS_LV_COR	VSS_LV	R9	VSS_LV_COR	VSS_LV
G16	VSS_LV_COR	VSS_LV	R10	VSS_LV_COR	VSS_LV
G17	VSS_LV_COR	VSS_LV	R11	VSS_LV_COR	VSS_LV
H7	VSS_LV_COR	VSS_LV	R12	VSS_LV_COR	VSS_LV
H8	VSS_LV_COR	VSS_LV	R13	VSS_LV_COR	VSS_LV
H9	VSS_LV_COR	VSS_LV	R14	VSS_LV_COR	VSS_LV
H10	VSS_LV_COR	VSS_LV	R15	VSS_LV_COR	VSS_LV

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
A13	GPIO	fec MDIO	A0: siul_GPIO[198] A1: fec_MDIO A2: _ A3: dspi2_CS0	I: _ I: _ I: siul_EIRQ[28]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A14	GPIO	fec TX_EN	A0: siul_GPIO[200] A1: fec_TX_EN A2: _ A3: lin0_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
A15	GPIO	fec TXD[3]	A0: siul_GPIO[204] A1: fec_TXD[3] A2: _ A3: dspi2_CS2	I: flexpwm1_FAULT[2] I: _ I: siul_EIRQ[29]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B3	GPIO	mc_cgl clk_out	A0: siul_GPIO[22] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: siul_EIRQ[18]	—	disabled	GP Slow/ Fast	VDD_HV_IO
B4	GPIO	can1 TXD	A0: siul_GPIO[14] A1: can1_TXD A2: _ A3: _	I: _ I: _ I: siul_EIRQ[13]	—	disabled	GP Slow/ Medium	VDD_HV_IO
B5	GPIO	nexus MDO[14][1]	A0: siul_GPIO[219] A1: _ A2: npc_wrapper_MDO[14] A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
B6	GPIO	dspi2 CS1	A0: siul_GPIO[9] A1: dspi2_CS1 A2: _ A3: _	I: flexpwm0_FAULT[0] I: lin3_RXD I: can2_RXD	—	disabled	GP Slow/ Medium	VDD_HV_IO
B7	GPIO	flexray CB_TR_EN	A0: siul_GPIO[52] A1: flexray_CB_TR_EN A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
B8	GPIO	flexray CA_TX	A0: siul_GPIO[48] A1: flexray_CA_TX A2: _ A3: _	I: ctu1_EXT_IN I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
B10	GPIO	fec RXD[3]	A0: siul_GPIO[214] A1: i2c1_data A2: _ A3: _	I: fec_RXD[3] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B11	GPIO	fec RX_ER	A0: siul_GPIO[215] A1: _ A2: _ A3: dspi0_CS1	I: fec_RX_ER I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B12	GPIO	fec RXD[1]	A0: siul_GPIO[212] A1: dspi1_CS1 A2: etimer2_ETC[5] A3: _	I: fec_RXD[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B13	GPIO	fec TX_ER	A0: siul_GPIO[205] A1: fec_TX_ER A2: dspi2_CS3 A3: _	I: flexpwm1_FAULT[3] I: lin0_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B14	GPIO	fec TX_CLK	A0: siul_GPIO[207] A1: flexray_DBG0 A2: etimer2_ETC[4] A3: dspi0_CS4	I: fec_TX_CLK I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
B15	GPIO	can0 TXD	A0: siul_GPIO[16] A1: can0_TXD A2: _ A3: sscm_DEBUG[0]	I: _ I: _ I: siul_EIRQ[15]	—	disabled	GP Slow/ Medium	VDD_HV_IO
C2	GPIO	nexus MDO[15][1]	A0: siul_GPIO[220] A1: _ A2: npc_wrapper_MDO[15] A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
C5	GPIO	flexray CB_RX	A0: siul_GPIO[50] A1: _ A2: ctu1_EXT_TGR A3: _	I: flexray_CB_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
C6	GPIO	etimer0 ETC[0]	A0: siul_GPIO[0] A1: etimer0_ETC[0] A2: _ A3: _	I: dspi2_SIN I: _ I: siul_EIRQ[0]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
D13	GPIO	fec MDC	A0: siul_GPIO[199] A1: fec_MDC A2: _ A3: _	I: _ I: lin1_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
D16	GPIO	pdi DATA[0]	A0: siul_GPIO[131] A1: _ A2: lin3_TXD A3: _	I: pdi_DATA[0] I: _ I: flexpwm2_FAULT[2]	—	disabled	PDI Medium	VDD_HV_PDI
D17	GPIO	pdi DATA[1]	A0: siul_GPIO[132] A1: flexpwm2_B[3] A2: _ A3: _	I: pdi_DATA[1] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
E2	GPIO	nexus MDO[1][1]	A0: siul_GPIO[86] A1: _ A2: npc_wrapper_MDO[1] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
E3	GPIO	flexray CA_RX	A0: siul_GPIO[49] A1: _ A2: ctu0_EXT_TGR A3: _	I: flexray_CA_RX I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
E14	GPIO	pdi LINE_V	A0: siul_GPIO[129] A1: _ A2: lin2_TXD A3: _	I: pdi_LINE_V I: _ I: flexpwm2_FAULT[0]	—	disabled	PDI Medium	VDD_HV_PDI
E15	GPIO	pdi DATA[2]	A0: siul_GPIO[133] A1: flexpwm2_A[1] A2: _ A3: etimer1_ETC[2]	I: pdi_DATA[2] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
E16	GPIO	pdi DATA[3]	A0: siul_GPIO[134] A1: flexpwm2_X[1] A2: _ A3: _	I: pdi_DATA[3] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
E17	GPIO	pdi DATA[4]	A0: siul_GPIO[135] A1: flexpwm2_A[2] A2: _ A3: etimer1_ETC[4]	I: pdi_DATA[4] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
F1	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
F14	GPIO	mc_cgl clk_out	A0: siul_GPIO[233] A1: mc_cgl_clk_out A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	PDI Fast	VDD_HV_PDI
F15	GPIO	pdi DATA[6]	A0: siul_GPIO[137] A1: flexpwm2_B[0] A2: _ A3: etimer1_ETC[1]	I: pdi_DATA[6] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F16	GPIO	pdi DATA[7]	A0: siul_GPIO[138] A1: flexpwm2_B[2] A2: _ A3: etimer1_ETC[5]	I: pdi_DATA[7] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
F17	GPIO	pdi DATA[8]	A0: siul_GPIO[139] A1: flexpwm2_A[3] A2: _ A3: _	I: pdi_DATA[8] I: _ I: _	—	disabled	PDI Medium	VDD_HV_PDI
G1	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
P4	GPIO	flexpwm0 A[3]	A0: siul_GPIO[102] A1: flexpwm0_A[3] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P20	GPIO	dramc D[14]	A0: siul_GPIO[188] A1: dramc_D[14] A2: ebi_AD22 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
P21	GPIO	dramc D[15]	A0: siul_GPIO[189] A1: dramc_D[15] A2: ebi_AD23 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
R1	GPIO	flexpwm0 X[2]	A0: siul_GPIO[98] A1: flexpwm0_X[2] A2: lin3_TXD A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R2	GPIO	flexpwm0 X[3]	A0: siul_GPIO[101] A1: flexpwm0_X[3] A2: _ A3: _	I: lin3_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R3	GPIO	flexpwm0 A[1]	A0: siul_GPIO[80] A1: flexpwm0_A[1] A2: _ A3: _	I: _ I: etimer0_ETC[2] I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
R21	GPIO	dramc ADD[3]	A0: siul_GPIO[161] A1: dramc_ADD[3] A2: ebi_ADD11 A3: ebi_TEA	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
R22	GPIO	dramc CKE	A0: siul_GPIO[147] A1: dramc_CKE A2: ebi_OE A3: flexpwm0_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T1	GPIO	flexpwm0 B[3]	A0: siul_GPIO[103] A1: flexpwm0_B[3] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

In case of only narrow band disturbances the maximum of the results will not change. In case of broadband signals the emission has to be below the limits.

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 15. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	750 (corners) 500	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply over voltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 16. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	CC	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Power Management Controller (PMC) electrical characteristics

3.8.1 PMC electrical specifications

This section contains electrical characteristics for the PMC.

3.12 FMPLL electrical characteristics

Table 22. FMPLL electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Typ	Max	Unit
1	$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range[1, 2]	Crystal reference	4	—	120	MHz
2	f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
3	$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	See the FMPLL chapter in the chip reference manual for more details on PLL configuration.	16	—	256	MHz
4	f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	19	—	60	MHz
5	f_{sys}	D	On-chip FMPLL frequency[2]	—	—	—	180	MHz
6	t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
7a	f_{LORL} f_{LORH}	D	Loss of reference frequency window[3]	Lower limit	1.6	—	3.7	MHz
7b				Upper limit	24	—	56	
8	f_{SCM}	D	Self-clocked mode frequency[4,5]	—	20	—	150	MHz
9	t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
10	t_{lpll}	D	FMPLL lock time [6, 7]	—	—	—	200	µs
11	t_{dc}	D	Duty cycle of reference	—	20	—	80	%
12a	C_{JITTER}	T	CLKOUT period jitter[8,9,10,11]	Peak-to-peak (clock edge to clock edge), $f_{FMPLLOUT}$ maximum[12]	—	—	160	ps
12b				Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	—	—	6	ns
13	Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±500	ps
14	Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
15	f_{LCK}	D	Frequency LOCK range	—	–4	—	+4	% $f_{FMPLLOUT}$
16	f_{UL}	D	Frequency un-LOCK range	—	–16	—	+16	% $f_{FMPLLOUT}$
17a	f_{CS} f_{DS}	D	Modulation Depth	Center spread	±0.25	—	±4	% $f_{FMPLLOUT}$
17b				Down Spread	–0.5	—	–8	
18	f_{MOD}	D	Modulation frequency[13]	31 < LDF[14] < 63 LDF > 63	—	—	(2240/LDF) 35	kHz

1 Considering operation with FMPLL not bypassed.

2 PFD clock range is 4– 16 MHz. An appropriate PLL Input division factor (IDF) should be chosen to divide the reference frequency to this range.

3.17.2 GP pads AC specifications

Table 34. GP pads AC electrical characteristics[1]

No.	Pad	Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	3	—	40	4	—	40	—	—	4	0.01	—	2	25
		3	—	40	6	—	50	—	—	2	0.01	—	2	50
		3	—	40	10	—	75	—	—	2	0.01	—	2	100
		3	—	40	14	—	100	—	—	2	0.01	—	2	200
2	Medium	1	—	15	2	—	12	—	—	40	2.5	—	7	25
		1	—	15	4	—	25	—	—	20	2.5	—	7	50
		1	—	15	8	—	40	—	—	13	2.5	—	7	100
		1	—	15	14	—	70	—	—	7	2.5	—	7	200
3	Fast	1	—	6	1	—	4	—	—	72	3	—	40	25
		1	—	6	1.5	—	7	—	—	55	7	—	40	50
		1	—	6	3	—	12	—	—	40	7	—	40	100
		1	—	6	5	—	18	—	—	25	7	—	40	200
4	Symmetric	1	—	8	1	—	5	—	—	50	3	—	25	25
5	Pullup/down (3.6 V max)	—	—	—	—	—	7500	—	—	—	—	—	—	50

1 The values provided in this table are not applicable for PDI and EBI/DRAM interface.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

3.18 PDI pads specifications

This section specifies the electrical characteristics of the PDI pads. Please refer to the tables in Section 2.2, Pin descriptions, for a cross reference between package pins and pad types.

PDI pads feature list:

- Direction
  - Input
  - Output
  - Bidirectional
- Driver
  - Push/Pull/Open Drain
  - Configurable Four Drive Strengths on Fast driver pads
  - Configurable No Slew-Rate, Slow Slew-Rate, and Fast Slew-Rate on Slow, Medium, and SLR driver pads
  - VDD_HV_PDI NOTE: All pads are NOT 5 V TOLERANT. Pads are not capable of driving to or from voltages above their respective VDD_HV_PDI. In other words, you cannot connect a 3.3V external device to a pad

3.21.4.3 External reset via $\overline{\text{RESET}}$

Figure 20 shows the voltage thresholds that determine the start of the reset sequences initiated by the assertion of $\overline{\text{RESET}}$ as specified in Table 53.

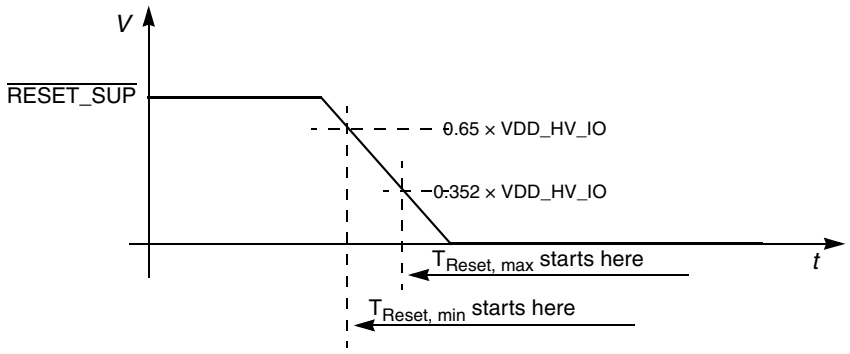

Figure 20. Reset sequence start via $\overline{\text{RESET}}$ assertion

3.21.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in Section 3.21, Reset sequence can be used to determine the correct positioning of the trigger window for the external watchdog. Figure 21 shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

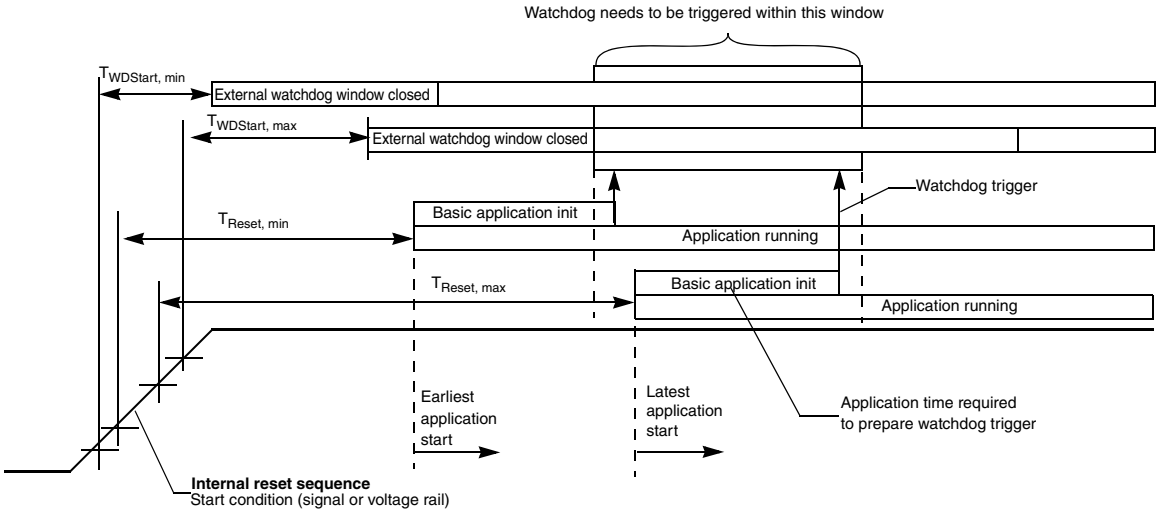

Figure 21. Reset sequence—external watchdog trigger window position

3.22 Peripheral timing characteristics

3.22.1 SDRAM (DDR)

The MPC5675K memory controller supports three types of DDR devices:

- DDR-1 (SSTL_2 class II interface)
- DDR-2 (SSTL_18 interface)
- LPDDR/Mobile-DDR (1.8V I/O supply voltage)

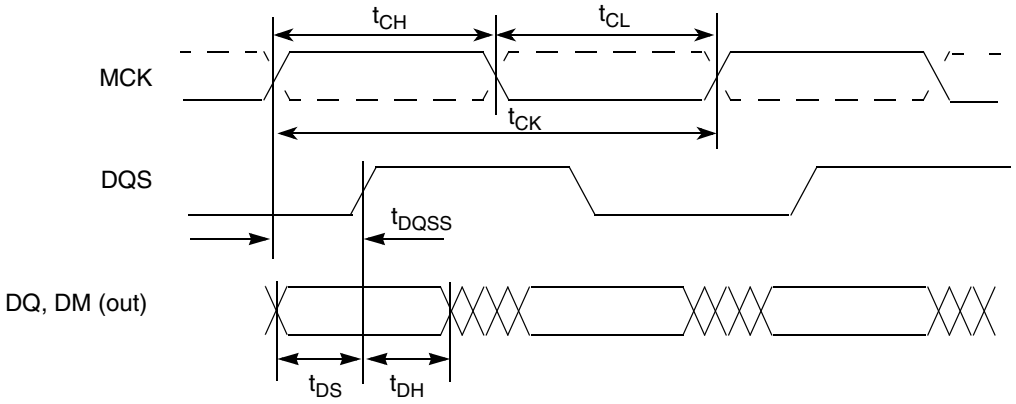

Figure 22. DDR write timing

Figure 23 and Figure 24 show the DDR SDRAM read timing.

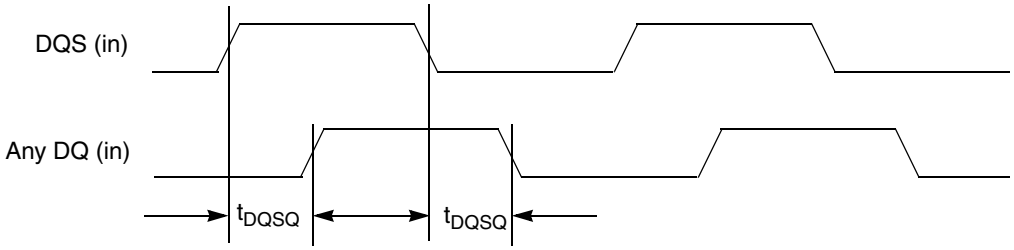

Figure 23. DDR read timing, DQ vs. DQS

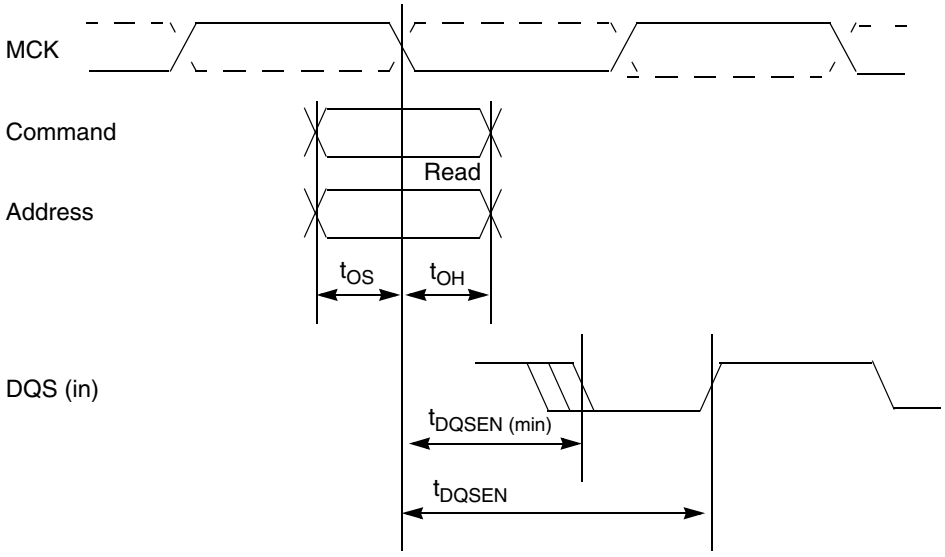

Figure 24. DDR read timing, DQSEN

Figure 25 provides the AC test load for the DDR bus.

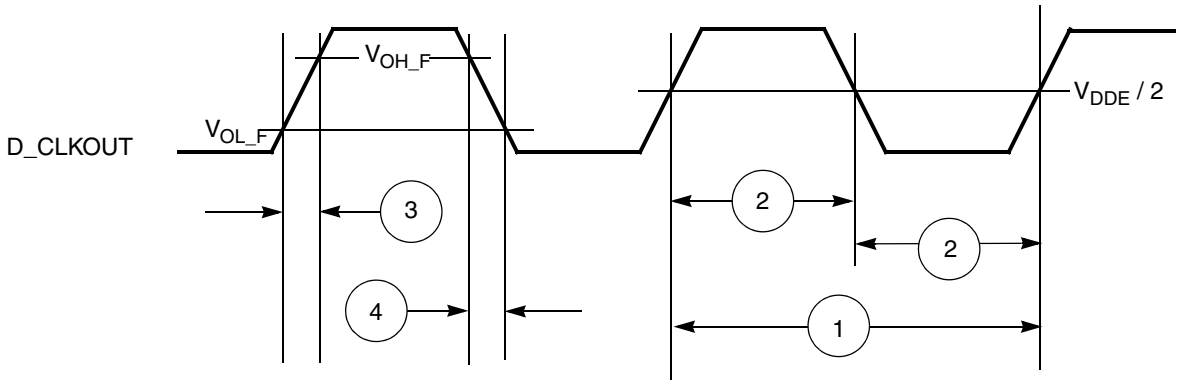

Figure 49. D_CLKOUT timing

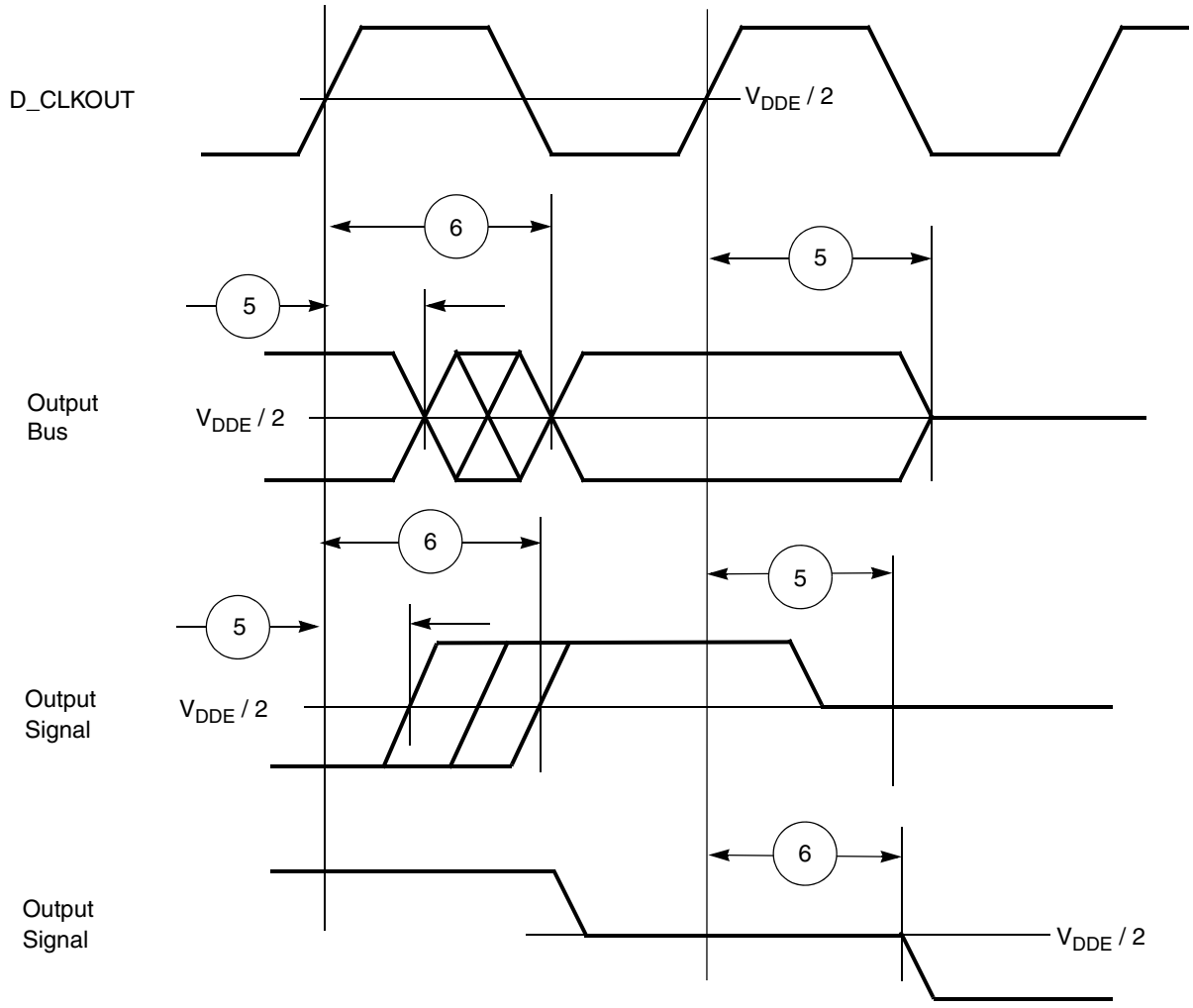

Figure 50. Synchronous output timing

3.22.10 I²C timing

Table 71. I²C SCL and SDA input timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1	—	D	Start condition hold time	2	—	IP bus cycle[1]
2	—	D	Clock low time	8	—	IP bus cycle[1]
3	—	D	Data hold time	0.0	—	ns
4	—	D	Clock high time	4	—	IP bus cycle[1]
5	—	D	Data setup time	0.0	—	ns
6	—	D	Start condition setup time (for repeated start condition only)	2	—	IP bus cycle[1]
7	—	D	Stop condition setup time	2	—	IP bus cycle[1]

1 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

Table 72. I²C SCL and SDA output timing specifications

No.	Symbol		Parameter	Value		Unit
				Min	Max	
1[1]	—	D	Start condition hold time	6	—	IP bus cycle[2]
2[1]	—	D	Clock low time	10	—	IP bus cycle[1]
3[3]	—	D	SCL/SDA rise time	—	99.6	ns
4[1]	—	D	Data hold time	7	—	IP bus cycle[1]
5[1]	—	D	SCL/SDA fall time	—	99.5	ns
6[1]	—	D	Clock high time	10	—	IP bus cycle[1]
7[1]	—	D	Data setup time	2	—	IP bus cycle[1]
8[1]	—	D	Start condition setup time (for repeated start condition only)	20	—	IP bus cycle[1]
9[1]	—	D	Stop condition setup time	10	—	IP bus cycle[1]

1 Programming IBFD (I²C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Inter Peripheral Clock is the clock at which the I²C peripheral is working in the device.

3 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pullup resistor values.

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00081D	REV: X2
	CASE NUMBER: 2082–01	15 JAN 2010
	STANDARD: NON–JEDEC	

Figure 55. 257 MAPBGA mechanical data (2 of 2)

Table 73. Revision history

Revision	Date	Description of Changes
1	6 Oct 2009	Initial release.
2	6 Dec 2009	Updated ball map tables, pin mux tables, supply and system pin tables. Added PMC specifications.
3	2 Jul 2010	Updated ball map tables, pin mux tables, supply and system pin tables. Updated pad specifications. Added reset specifications section.
4	30 Apr 2011	Removed thickness dimension from package diagrams on cover page. Added footnote “Do not connect pin directly to a power supply or ground” for MDO[0:15] and MSEO[0:1] pins to Table 9 (257 MAPBGA pin multiplexing) and Table 10 (473 MAPBGA pin multiplexing). In Table 17 (PMC electrical specifications): • Added minimum and maximum slew rate specifications for LvdReg. • Removed LvdC minimum and maximum hysteresis specifications • Removed HvdC minimum and maximum hysteresis specifications • Corrected HvcD nominal hysteresis from 1.32 to 1.36 In Table 18 (VRC SMPS recommended external devices), updated specifications for device Q (FET). Renamed Section 3.9, Supply current characteristics (was “Power dissipation and current consumption”). Renamed Table 19 (Current consumption characteristics) (was “Power dissipation characteristics”). In Table 19 (Current consumption characteristics): • Updated ADC current consumption to 1.2 mA per ADC plus 0.7 mA (2.0 mA total) for ADC0. • Updated Run I_{DD} to 900 mA max. Updated Accuracy specification in Table 20 (Temperature sensor electrical characteristics): changed “T_J = –40 °C to T_A = 25 °C” to “T_J = –40 °C to T_A = 125 °C,” removed row “T_J = T_A to 125 °C”. In Table 21 (Main oscillator electrical characteristics), added symbol name F_{XOSCHS} for Oscillator frequency specification. Removed “Typical” figures for these specifications. Added footnote “ADC0 includes 0.7 mA dissipation for the temperature sensor (TSENS).” In Table 22 (FMPLL electrical characteristics), added minimum and maximum values for specification f_{FREE}, “Free running frequency.” In Table 23 (RC oscillator electrical characteristics): • Added specification $\Delta_{IRCTRIM}$ “Internal RC oscillator trimming step.” • Removed specification Δ_{RCTRIM} “Post trim accuracy: The variation of the PTF from the 16 MHz” (specification replaced by $\Delta_{IRCTRIM}$ “Internal RC oscillator trimming step”). In Table 24 (ADC conversion characteristics), updated Gain Error (GNE) to “min = –4 max = +4 LSB“ . Added Table 30 (Code flash write access timing) and Table 31 (Data flash write access timing).

Table 73. Revision history (continued)

Revision	Date	Description of Changes
7 (cont.)	18 May 2012	In Section 3.2, Absolute maximum ratings, Table 11 (Absolute maximum ratings), • Deleted footnote to the Max value "Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined." • Added footnote to $V_{DD\_HV\_DRAM}$: "As the $V_{DD\_HV\_DRAM\_VREF}$ supply should always be constrained by the $V_{DD\_HV\_DRAM}$ supply for example through a voltage divider network per the JEDEC specification, the maximum ratings for the $V_{DD\_HV\_DRAM}$ supply should be used for the $V_{DD\_HV\_DRAM\_VREF}$ reference as well." • Changed absolute max rating for $V_{DD\_LV\_PLL}$ from 1.4 to 1.32. • Added footnote to Min value of T_{STG}: "If the ambient temperature is at or above the minimum storage temperature and below the recommended minimum operating temperature, power may be applied to the device safely. However, functionality is not guaranteed and a power cycle must be administered if in internal regulation mode or an assertion of RESET_SUP_B must be administered if in external regulation mode once device enters into the recommended operating temperature range." In Section 3.3, Recommended operating conditions, Table 12 (Recommended operating conditions), • For T_A and T_J, added footnote "When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition." • For T_A, changed the Max temperature spec for the 257 package from 105 to 125 and deleted footnote: "Preliminary data." In Section 3.8.1, PMC electrical specifications, Table 17 (PMC electrical specifications), • No. 4 LvdC and No. 5 HvdC threshold were specified as rising edge and hysteresis. The specification is changed to rising edge / falling edge. • Removed No. 6, VddStepC, and renumbered subsequent lines. In Section 3.9, Supply current characteristics, Table 19 (Current consumption characteristics), added a footnote to No. 3. Idd_HV_FLA. "The current specified for Idd_HV_FLA includes current consumed during programming and erase operations." In Section 3.12, FMPLL electrical characteristics, Table 22 (FMPLL electrical characteristics), replaced "f_{sys}" with "$f_{FMPLLOUT}$" in rows for C_{JITTER}, f_{LCK}, f_{UL}, f_{CS}/f_{DS}, and footnote 9. In Section 3.14.1, Input impedance and ADC accuracy: • Changed "C_S being substantially a switched capacitance..." to "C_S and C_{P2} being substantially a switched capacitance..." • Changed "and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, ..." to "and the sum of $R_S + R_F$, ..." • Changed the equation $$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ to $$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2}\mathrm{LSB}$$ In Section 3.14.1, Input impedance and ADC accuracy, Table 24 (ADC conversion characteristics), added new spec after line 3 for $t_{ADC\_S\_PMC}$, C: Parameter: Sample time of internal PMC channels. Conditions: - , Min : 717, Typ : - , Max : - , Unit : nS. In Section 3.17.1, GP pads DC specifications, Table 33 (GP pads DC electrical characteristics), added new spec for "Input pad capacitance", No. 21.

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Document Number: MPC5675K
Rev. 7
5/2012