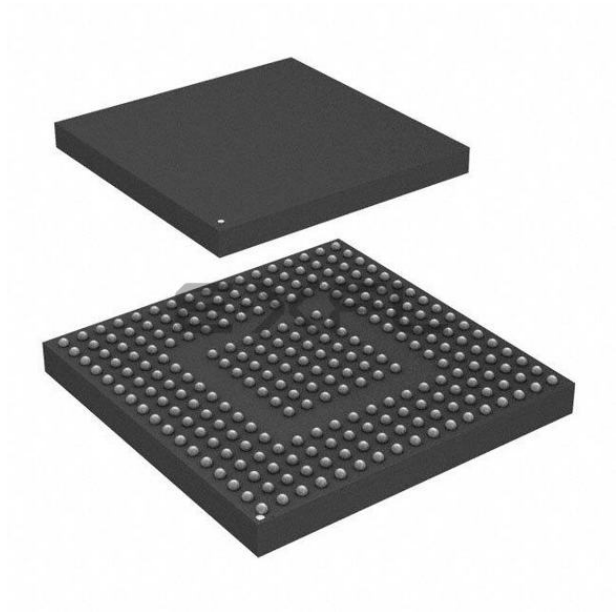

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 22x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	257-LFBGA
Supplier Device Package	257-LFBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kff0mmm2r

Table 1. MPC5675K family device comparison (continued)

Features		MPC5673K	MPC5674K	MPC5675K
Modules (cont.)	External Bus Interface (EBI)	1 module[5] 16-bit Data + Address or 32-bit Data with Address bus muxed[8]		
	Fast Ethernet Controller (FEC)	1 module		
	Fault Collection and Control Unit (FCCU)	1 module		
	FlexCAN	4 modules (32 message buffers each)		
	FlexPWM	3 modules (each 4 × 3 channels)		
	FlexRay	Optional		Yes
	I^2C	2 modules[6]	3 modules	
	Interrupt Controller (INTC)	Yes (SoR)		
	LINFlex	3 modules[7]	4 modules	
	Parallel Data Interface (PDI)	1 module[8]		
	Periodic Interrupt Timer (PIT)	1 module, 4 channels		
	Software Watchdog Timer (SWT)	Yes (SoR)		
	System Timer Module (STM)	Yes (SoR)		
	Temperature sensor	1 module		
	Wakeup Unit (WKPU)	Yes		
	Crossbar switch (XBAR)	3 modules, 2 are user-configurable		
Clocking	Clock monitor unit (CMU)	3 modules		
	Frequency-modulated phase-locked loop (FMPLL)	2 modules (system and auxiliary)		
	IRCOSC – 16 MHz	1		
	XOSC 4–40 MHz	1		
Supply	Power management unit (PMU)	Yes		
	1.2 V low-voltage detector (LVD12)	1		
	1.2 V high-voltage detector (HVD12)	1		
	2.7 V low-voltage detector (LVD27)	4		
Debug	Nexus	Class 3+ (for cores and SRAM ports)		

  - Modified SPI mode for interfacing to peripherals with longer setup time requirements
- Support for up to 60 Mbit/s in slave only Rx mode

1.6.15 Serial Communication Interface Module (LINFlex)

The LINFlex on this device features the following:

- Supports LIN Master mode, LIN Slave mode, and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Manages LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store as many as 8 data bytes
  - Supports messages as long as 64 bytes
  - Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and timeout errors)
  - Classic or extended checksum calculation
  - Configurable break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features (loop back, LIN bus stuck dominant detection)
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit, 9-bit, or 16-bit words)
  - Configurable parity scheme: none, odd, even, always 0
  - Speed as fast as 2 Mbit/s
  - Error detection and flagging (parity, noise, and framing errors)
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - Two receiver wake-up methods
- Support for DMA-enabled transfers

1.6.16 FlexCAN

- Thirty-two message buffers each
- Full implementation of the CAN protocol specification, Version 2.0B
- Programmable acceptance filters
- Individual Rx filtering per message buffer
- Short latency time for high priority transmit messages
- Arbitration scheme according to message ID or message buffer number
- Listen-only mode capabilities
- Programmable clock source: system clock or oscillator clock

- Reception queue possible by setting more than one Rx message buffer with the same ID
- Backwards compatible with previous FlexCAN modules
- Safety CAN features on 1 CAN module as implemented on MPC5604P

1.6.17 Dual-channel FlexRay controller

- Full implementation of FlexRay Protocol Specification 2.1
- Sixty-four configurable message buffers can be handled
- Message buffers configurable as Tx, Rx, or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count, and message ID
- Programmable acceptance filters for RxFIFO message buffers
- Dual channel, each at up to 10 Mbit/s data rate

1.6.18 Periodic Interrupt Timer (PIT)

The PIT module implements the features below:

- Four general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- 32-bit counter for real time interrupt, clocked from main external oscillator
- Can be used for software tick or DMA trigger operation

1.6.19 System Timer Module (STM)

The STM implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Up-counter with four output compare registers
- OS task protection and hardware tick implementation as per current state-of-the-art AUTOSAR requirement

1.6.20 Motor control (MOTC) peripherals

The peripherals in this section can be used for general-purpose applications, but are specifically designed for motor control (MOTC) applications.

1.6.20.1 FlexPWM

The pulse width modulator module (FlexPWM) contains three PWM channels, each of which is configured to control a single half-bridge power stage. There may also be one or more fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency lower than or equal to platform frequency
- Clock source not modulated and independent from system clock (generated via auxiliary PLL)
- Fine granularity control for enhanced resolution of the PWM period

- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM is supported
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for:
  - buffered output compare functions
  - input capture functions
- Enhanced dual-edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high and low limit registers
- Supports safety measures using DMA

1.6.20.2 Cross Triggering Unit (CTU)

The CTU provides automatic generation of ADC conversion requests on user-selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double-buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Maximum operating frequency lower than or equal to platform
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low-pass filter
- Double-buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double-buffered ADC command list pointers to minimize ADC trigger unit update
- Double-buffered ADC conversion command list with as many as twenty-four ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows controlling ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 2 shows the MPC5675K in the 257 MAPBGA package. Figure 3, Figure 4, Figure 5, and Figure 6 show the MPC5675K in the 473 MAPBGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VSS_HV_IO	VSS_HV_IO	VDD_HV_IO	nexus MDO[5]	nexus MDO[7]	nexus MDO[9]	flexray CB_TX	flexray CA_TR_EN	VDD_HV_IO	fec RXD[2]	fec RX_CLK	fec RXD[0]	fec MDIO	fec TX_EN	fec TXD[3]	VSS_HV_IO	VSS_HV_IO	A
B	VSS_HV_IO	VSS_HV_IO	mc_cgl clk_out	can1 TXD	nexus MDO [14]	dspi2 CS1	flexray CB_TR_EN	flexray CA_TX	VSS_HV_IO	fec RXD[3]	fec RX_ER	fec RXD[1]	fec TX_ER	fec TX_CLK	can0 TXD	VDD_HV_IO	VSS_HV_IO	B
C	VDD_HV_IO	nexus MDO [15]	VSS_HV_IO	FCCU_F[1]	flexray CB_RX	etimer0 ETC[0]	etimer0 ETC[1]	etimer0 ETC[2]	etimer0 ETC[3]	JCOMP	fec CRS	fec TXD[0]	fec COL	can0 RXD	VSS_HV_PDI	pdi DATA [5]	pdi CLOCK	C
D	nexus MDO [2]	nexus MDO [3]	can1 RXD	dspi0 SOUT	RESERVED	etimer0 ETC[5]	etimer0 ETC[4]	VDD_HV_FLA	VSS_HV_FLA	fec TXD[2]	fec TXD[1]	fec RX_DV	fec MDC	VDD_HV_PDI	VSS_HV_IO	pdi DATA [0]	pdi DATA [1]	D
E	nexus MDO [0]	nexus MDO [1]	flexray CA_RX	NMI										pdi LINE_V	pdi DATA [2]	pdi DATA [3]	pdi DATA [4]	E
F	nexus MDO[6]	nexus MDO [11]	dspi1 SOUT	dspi1 SIN		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		mc_cgl clk_out	pdi DATA [6]	pdi DATA [7]	pdi DATA [8]	F
G	nexus MDO [4]	VDD_HV_IO	dspi0 SCK	dspi1 SCK		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [9]	pdi DATA [10]	pdi DATA [11]	pdi FRAME_V	G
H	nexus MDO [10]	VSS_HV_IO	dspi0 CS0	dspi1 CS0		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [12]	pdi DATA [13]	VDD_HV_PDI	flexpwm 0 X[0]	H
J	nexus MCKO	nexus MDO[8]	dspi2 CS0	dspi2 CS2		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		pdi DATA [14]	pdi DATA [15]	VSS_HV_PDI	flexpwm 0 X[1]	J
K	nexus MSEO_B[0]	nexus MSEO_B[1]	nexus RDY_B	dspi0 SIN		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		flexpwm 0 X[2]	flexpwm 0 X[3]	flexpwm 0 A[1]	flexpwm 0 B[0]	K
L	nexus EVTO_B	nexus EVTI_B	dspi2 SCK	nexus MDO [13]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		VDD_HV_DRAM_VREF	TCK	flexpwm 0 B[1]	TDO	L
M	VDD_HV_OSC	VDD_HV_IO	dspi1 CS2	nexus MDO [12]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		flexpwm 0 B[2]	TDI	TMS	flexpwm 1 A[1]	M
N	XTALIN	VSS_HV_IO	dspi0 CS3	VSS_LV_PLL										flexpwm 0 B[3]	flexpwm 0 A[2]	flexpwm 1 A[0]	flexpwm 1 B[0]	N
P	VSS_HV_OSC	$\overline{\text{RESET}}$	dspi0 CS2	VDD_LV_PLL	etimer1 ETC[1]	etimer1 ETC[2]	adc0 AN[0]	etimer1 ETC[3]	VSS_HV_IO	VDD_HV_IO	adc0_adc1 AN[14]	etimer1 ETC[4]	etimer1 ETC[5]	VDD_HV_IO	flexpwm 0 A[3]	flexpwm 0 A[0]	flexpwm 1 B[1]	P
R	XTAL OUT	FCCU_F[0]	VSS_HV_IO	dspi1 CS3	adc2 AN[0]	adc2 AN[3]	VDD_HV_ADR_13	adc2_adc3 AN[14]	VDD_HV_ADR_02	adc0 AN[2]	adc0_adc1 AN[13]	adc1 AN[1]	VREG_CTRL	lin0 TXD	VSS_HV_IO	flexpwm 1 A[2]	flexpwm 1 B[2]	R
T	VSS_HV_IO	VDD_HV_IO	dspi2 SOUT	adc3 AN[0]	adc3 AN[3]	adc2 AN[2]	VSS_HV_ADR_13	adc2_adc3 AN[13]	VSS_HV_ADR_02	adc0 AN[1]	adc0_adc1 AN[12]	adc1 AN[0]	adc1 AN[2]	lin0 RXD	etimer1 ETC[0]	VDD_HV_IO	VSS_HV_IO	T
U	VSS_HV_IO	VSS_HV_IO	dspi2 SIN	adc3 AN[1]	adc3 AN[2]	adc2 AN[1]	adc2_adc3 AN[11]	adc2_adc3 AN[12]	VDD_HV_ADV	VSS_HV_ADV	adc0_adc1 AN[11]	VREG_INT_ENABLE	$\overline{\text{RESET\_SUP}}$	VDD_HV_PMU	VSS_HV_PMU	VSS_HV_IO	VSS_HV_IO	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2. MPC5675K 257 MAPBGA pinout (top view)

Table 2. Pad types (continued)

Pad Type	Description
DRAM ACC	Bidirectional DDR pad. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM CLK	Differential clock driver.
DRAM DQ	Bidirectional DDR pad with integrated ODT. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM ODT CTL	Enable On Die Termination control.
Analog	CMOS Schmitt trigger cell with injection proof analog switch.
Analog Shared	CMOS Schmitt trigger cell with two injection-proof analog switches.

2.2.2 Power supply and reference voltage pins

Table 3 shows the supply pins for the MPC5675K in the 257 MAPBGA package. Table 5 shows the supply pins for the MPC5675K in the 473 MAPBGA package.

Table 4 and Table 6 show the pins not populated on the MPC5675K 257 MAPBGA and 473 MAPBGA packages, respectively.

Table 3. 257 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F9	VDD_LV_COR	VDD_LV
A9	VDD_HV_IO	VDD_HV	F10	VDD_LV_COR	VDD_LV
B16	VDD_HV_IO	VDD_HV	F11	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F12	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	G12	VDD_LV_COR	VDD_LV
P10	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
P14	VDD_HV_IO	VDD_HV	H12	VDD_LV_COR	VDD_LV
T2	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T16	VDD_HV_IO	VDD_HV	J12	VDD_LV_COR	VDD_LV
L14	VDD_HV_DRAM_VREF	VDD_HV	K6	VDD_LV_COR	VDD_LV
D8	VDD_HV_FLA	VDD_HV	K12	VDD_LV_COR	VDD_LV
M1	VDD_HV_OSC	VDD_HV	L6	VDD_LV_COR	VDD_LV
D14	VDD_HV_PDI	VDD_HV	L12	VDD_LV_COR	VDD_LV
H16	VDD_HV_PDI	VDD_HV	M6	VDD_LV_COR	VDD_LV
U14	VDD_HV_PMU	VDD_HV	M7	VDD_LV_COR	VDD_LV
R7	VDD_HV_ADR_13	VDD_HV_A	M8	VDD_LV_COR	VDD_LV

2.2.4 Multiplexed pins

Table 9 shows the pin multiplexing for the MPC5675K in the 257 MAPBGA package. Table 10 shows the pin multiplexing for the MPC5675K in the 473 MAPBGA package.

Table 9. 257 MAPBGA pin multiplexing

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
A4	GPIO	nexus MDO[5][1]	A0: siul_GPIO[114] A1: _ A2: npc_wrapper_MDO[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A5	GPIO	nexus MDO[7][1]	A0: siul_GPIO[112] A1: _ A2: npc_wrapper_MDO[7] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A6	GPIO	nexus MDO[9][1]	A0: siul_GPIO[110] A1: _ A2: npc_wrapper_MDO[9] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
A7	GPIO	flexray CB_TX	A0: siul_GPIO[51] A1: flexray_CB_TX A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A8	GPIO	flexray CA_TR_EN	A0: siul_GPIO[47] A1: flexray_CA_TR_EN A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: _	—	disabled	GP Slow/ Symmetric	VDD_HV_IO
A10	GPIO	fec RXD[2]	A0: siul_GPIO[213] A1: _ A2: _ A3: dspi2_SOUT	I: fec_RXD[2] I: _ I: siul_EIRQ[21]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A11	GPIO	fec RX_CLK	A0: siul_GPIO[209] A1: flexray_DBG2 A2: etimer2_ETC[2] A3: dspi0_CS6	I: fec_RX_CLK I: _ I: siul_EIRQ[25]	—	disabled	GP Slow/ Medium	VDD_HV_IO
A12	GPIO	fec RXD[0]	A0: siul_GPIO[211] A1: i2c1_clock A2: _ A3: _	I: fec_RXD[0] I: _ I: siul_EIRQ[27]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
H4	GPIO	nexus EVTI_B	A0: siul_GPIO[91] A1: _ A2: leo_sor_proxy_EVTI_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
H20	GPIO	dramc D[2]	A0: siul_GPIO[176] A1: dramc_D[2] A2: ebi_AD10 A3: ebi_ADD26	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
J1	GPIO	nexus RDY_B	A0: siul_GPIO[216] A1: _ A2: nexus_RDY_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J2	GPIO	nexus MDO[13][1]	A0: siul_GPIO[218] A1: _ A2: npc_wrapper_MDO[13] A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J3	GPIO	nexus MDO[12][1]	A0: siul_GPIO[217] A1: _ A2: npc_wrapper_MDO[12] A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
J4	GPIO	dspi1 SIN	A0: siul_GPIO[8] A1: _ A2: _ A3: _	I: dspi1_SIN I: _ I: siul_EIRQ[8]	—	disabled	GP Slow/ Medium	VDD_HV_IO
J20	GPIO	dramc D[0]	A0: siul_GPIO[174] A1: dramc_D[0] A2: ebi_AD8 A3: ebi_ADD24	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
J21	GPIO	dramc D[1]	A0: siul_GPIO[175] A1: dramc_D[1] A2: ebi_AD9 A3: ebi_ADD25	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
J22	GPIO	dramc D[3]	A0: siul_GPIO[177] A1: dramc_D[3] A2: ebi_AD11 A3: ebi_ADD27	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM

Table 12. Recommended operating conditions[1] (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	0	0	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	3.0	3.6	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	0	0	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	3.0	3.6	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	0	0	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	3.0	3.6	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	0	0	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	1.62	3.6	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	0	0	V
11	$V_{DD\_HV\_DRAM}$	SR	DRAM interface supply voltage	—	1.62	3.6	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	0	0	V
13	$V_{DD\_HV\_ADRx}$	SR	ADC*x* high reference voltage	—	3.0	3.6	V
				Alternate input voltage	4.5	5.5	
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	0	0	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	3.0	3.6	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	0	0	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic[2]	External VREG mode	1.14	1.32	V
17a		CC		Internal VREG Mode	1.14	1.32	V
18	$V_{SS\_LV\_COR}$	SR	Core supply voltage ground digital logic	—	0	0	V
19	$V_{DD\_LV\_PLL}$	SR	PLL supply voltage[2]	External VREG mode	1.14	1.32	V
19a		CC		Internal VREG Mode	1.14	1.32	V
20	$V_{SS\_LV\_PLL}$	SR	PLL reference voltage	—	0	0	V
21	T_A	SR	Ambient temperature under bias[3,4]	257 MAPBGA	–40	125	°C
				473 MAPBGA	–40	125	°C
22	T_J	SR	Junction temperature under bias[4]	257 MAPBGA	–40	150	°C
				473 MAPBGA	–40	150	

1 These specifications are design targets and are subject to change per device characterization.

2 The jitter specifications for both PLLs holds true only up to 50 mV noise (peak to peak) on $V_{DD\_LV\_COR}$ and $V_{DD\_LV\_PLL}$.

3 See Table 1 for available frequency and package options.

4 When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is not necessary that both specifications be met at all times. However, it is critical that the junction temperature specification is not exceeded under any condition.

supplied with 2.5 V. If a pad must be connected to a 3.3V device, its local VDD_HV_PDI must be 3.3 V. Injection current is then handled by the intrinsic diodes from the pad transistors and by the ESD diodes.

  - VDD_HV_PDI range 1.8 V to 3.3 V, as specified in the following tables
- Receiver
  - Selectable hysteresis input buffer
  - CMOS Input Buffer

The electrical data provided in this section applies:

- To the pads listed in Table 35
- Over the voltage range 1.62–3.6 V

Table 35. PDI I/O pads

No.	Name	Voltage	Used for	Notes
1	PDI Fast	1.62–3.6 V	I/O	Enhanced operating voltage range fast slew-rate output with four selectable slew-rates. Contains an input buffer and weak pullup/pulldown.
2	PDI Medium			Enhanced operating voltage range medium slew-rate output with four selectable slew-rates. Contains an input buffer and weak pullup/pulldown.

Table 36. PDI pads DC electrical characteristics[1]

No.	Symbol		Parameter	Min	Max	Unit
1	$V_{DD\_HV\_PDI}$	SR	I/O supply voltage	1.62	3.6	V
2	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis enabled)	$0.65 \times V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI} + 0.3$	V
3	V_{IH_C}	CC	CMOS input buffer high voltage (hysteresis disabled)	$0.58 \times V_{DD\_HV\_PDI}$	$V_{DD\_HV\_PDI} + 0.3$	V
4	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis enabled)	$V_{SS} - 0.3$	$0.35 \times V_{DD\_HV\_PDI}$	V
5	V_{IL_C}	CC	CMOS input buffer low voltage (hysteresis disabled)	$V_{SS} - 0.3$	$0.42 \times V_{DD\_HV\_PDI}$	V
6	V_{HYS_C}	CC	CMOS input buffer hysteresis	$0.1 \times V_{DD\_HV\_PDI}$	—	V
7	I_{ACT_S}	CC	Selectable weak pullup/pulldown current	25	150	µA
8	V_{OH}	CC	Output high voltage	$0.8 \times V_{DD\_HV\_PDI}$	—	V
9	V_{OL}	CC	Output low voltage	—	$0.2 \times V_{DD\_HV\_PDI}$	V

1 Over- and undershoots occurring due to impedance mismatch of the external driver and the transmission line at PDI pads in input mode can be allowed up to 0.7 V repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.

Table 37. Drive current

Pad	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
PDI Fast	All	26.2	84.8
PDI Medium	All	19.2	52.1

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.

2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

– 150 Ω

The electrical data provided in Section 3.19, DRAM pad specifications, applies to the pads listed in Table 39.

Table 39. DRAM pads

Name	Voltage	Used For	Notes[1]
DRAM ACC	1.62 V–3.6 V	I/O	Bidirectional DDR pad
DRAM CLK	1.62 V–3.6 V	O	Output only differential clock driver pad
DRAM DQ	1.62 V–3.6 V	I/O	Bidirectional DDR pad with integrated ODT

1 All pads can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.

All three pad types can be configured to support SDR, DDR, DDR2 half and full strength, and LPDDR half and full strength modes, according to Table 40.

Table 40. Mode configuration for DRAM pads

Configuration[1]	Mode
000	1.8 V LPDDR Half Strength
001	1.8 V LPDDR Full Strength
010	1.8 V DDR2 Half Strength
011	2.5 V DDR
100	Not supported
101	Not supported
110	1.8 V DDR2 Full Strength
111	SDR

1 Configuration is selected in the corresponding PCR registers of the SIUL.

NOTE

0.7 V overshoot/undershoot can be allowed to occur repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.

3.19.1 DRAM pads electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

Table 41. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	3.0	3.6	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	1.3	1.7	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ − 0.05	$V_{DD\_HV\_DRAM\_VREF}$ + 0.05	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.20	—	V

Table 41. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V) (continued)

No.	Symbol		Parameter	Condition	Min	Max	Unit
5	V_{IL}	CC	Input low voltage	—		$V_{DD\_HV\_DRAM\_VREF}$ – 0.2	V
6	V_{OH}	CC	Output high voltage	—	$V_{DD\_HV\_DRAM\_VTT}$ + 0.8	—	V
7	V_{OL}	CC	Output low voltage	—	—	$V_{DD\_HV\_DRAM\_VTT}$ – 0.8	V

1 BGA473: Termination voltage can be supplied via package pins. BGA257 termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT.

Table 42. Output drive current @ V_{DDE} = 3.3 V (±10%)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	111	–16	16
2	DRAM DQ			
3	DRAM CLK			

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.

2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 43. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Output Slew rate Rise/Fall (V/ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
2	DRAM DQ	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
3	DRAM CLK	1.4/1.4	2.4/2.4	3.1/2.5	5.7/5.7	5	111
		1.6/1.6	2.6/2.6	1.1/1.3	2.3/2.3	20	111

1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19.2 DRAM pads electrical specification ($V_{DD\_HV\_DRAM}$ = 2.5 V)

Table 44. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 2.5 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	2.3	2.7	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	0.49 × $V_{DD\_HV\_DRAM}$	0.51 × $V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V

3.20 $\overline{\text{RESET}}$ characteristics

3.20.1 $\overline{\text{RESET}}$ pin characteristics

Table 50. $\overline{\text{RESET}}$ pin characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	W_{FRST}	SR	$\overline{\text{RESET}}$ pulse is sure to be filtered	—	—	70	ns
2	W_{NFRST}	SR	$\overline{\text{RESET}}$ pulse is sure not to be filtered	—	400	—	ns

3.20.2 $\overline{\text{RESET\_SUP\_B}}$ pin characteristics

Table 51. $\overline{\text{RESET\_SUP\_B}}$ pin characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	W_{FRST}	SR	$\overline{\text{RESET\_SUP\_B}}$ pulse is sure to be filtered (there is no internal filter on this pin)	—	—	0	ns
2	T_{RSTSUP}	SR	$\overline{\text{RESET\_SUP\_B}}$ release by an external delay/monitor circuit after all supplies are stable	—	0	—	ns

3.21 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences depending on internal or external VREG mode.

3.21.1 Reset sequence duration

Table 52 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Section 3.21.2, Reset sequence description.

Table 52. RESET sequences

No.	Symbol		Parameter	T_{Reset}			Unit
				Min	Typ	Max[1]	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled	60	65	70	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	40	400	1000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled	60	65	70	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	40	300	600	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	1	3	10	µs

1 The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

JEDEC standards define the minimum set of requirements for compliant memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, MAY 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The MPC5675K supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strength (intended for lighter loads or point-to-point environments)

The MPC5675K memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the Section 3.19, DRAM pad specifications.

3.22.1.1 DDR and DDR2 SDRAM AC timing specifications

Table 55. DDR and DDR2 (DDR2-400) SDRAM timing specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

No.	Symbol		Parameter	Min	Max	Unit
1	t_{CK}	CC	Clock cycle time, CL = *x*	—	90	MHz
2	$V_{IX\text{-}AC}$	CC	MCK AC differential crosspoint voltage[1]	$V_{DD\_MEM\_IO}$ × 0.5 – 0.1	$V_{DD\_MEM\_IO}$ × 0.5 + 0.1	V
3	t_{CH}	CC	CK HIGH pulse width[1, 2]	0.47	0.53	t_{CK}
4	t_{CL}	CC	CK LOW pulse width[1, 2]	0.47	0.53	t_{CK}
5	t_{DQSS}	CC	Skew between MCK and DQS transitions[2, 3]	–0.25	0.25	t_{CK}
6	$t_{OS(base)}$	CC	Address and control output setup time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)		ps
7	$t_{OH(base)}$	CC	Address and control output hold time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)	—	ps
8	$t_{DS1(base)}$	CC	DQ and DM output setup time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
9	$t_{DH1(base)}$	CC	DQ and DM output hold time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
10	t_{DQSQ}	CC	DQS-DQ skew for DQS and associated DQ inputs[2]	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps

1 Measured with clock pin loaded with differential 100 Ω termination resistor.

2 All transitions measured at mid-supply ($V_{DD\_MEM\_IO}$/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

Figure 22 shows the DDR SDRAM write timing.

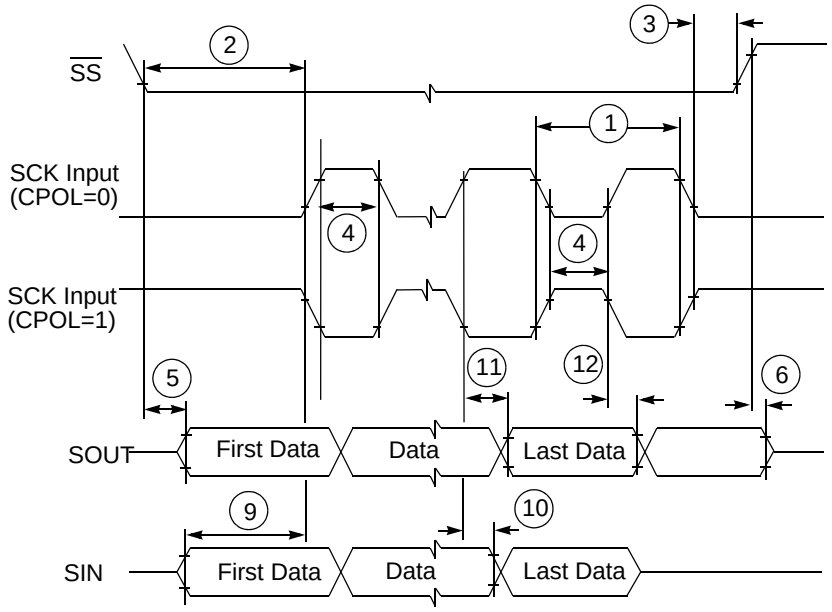

Figure 39. DSPI modified transfer format timing—slave, CPHA = 0

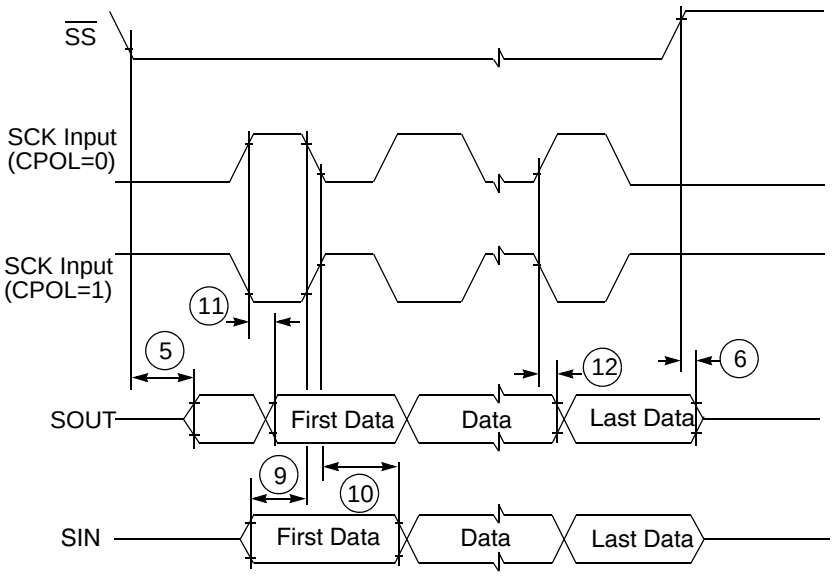

Figure 40. DSPI modified transfer format timing—slave, CPHA = 1

Table 70. EBI timing (continued)

No.	Symbol		Parameter	45 MHz (Ext. Bus Freq)[1]		Unit	Notes
				Min	Max		
6	t_{COV}	CC	D_CLKOUT posedge to output signal valid (output delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE $\overline{\text{D\_RD\_WR}}$ D_TA D_TS $\overline{\text{D\_WE}}$[0:3]/$\overline{\text{D\_BE}}$[0:3]	—	10	ns	—
7	t_{CIS}	CC	Input signal valid to D_CLKOUT posedge (setup time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	7.5	—	ns	—
8	t_{CIH}	CC	D_CLKOUT posedge to input signal invalid (hold time) D_ADD[9:30] D_DAT[0:15] $\overline{\text{D\_RD\_WR}}$ D_TA D_TS	1.0	—	ns	—
9	t_{APW}	CC	D_ALE pulse width	6.5	—	ns	The timing is for asynchronous external memory system.
10	t_{AAI}	CC	D_ALE negated to address invalid	1.5	—	ns	• The timing is for asynchronous external memory system. • ALE is measured at 50% of VDDE.

[1] Speed is the nominal maximum frequency. Maximum core speed allowed is 180 MHz plus frequency modulation (FM).

4 Package characteristics

4.1 Package mechanical data

4.1.1 257 MAPBGA

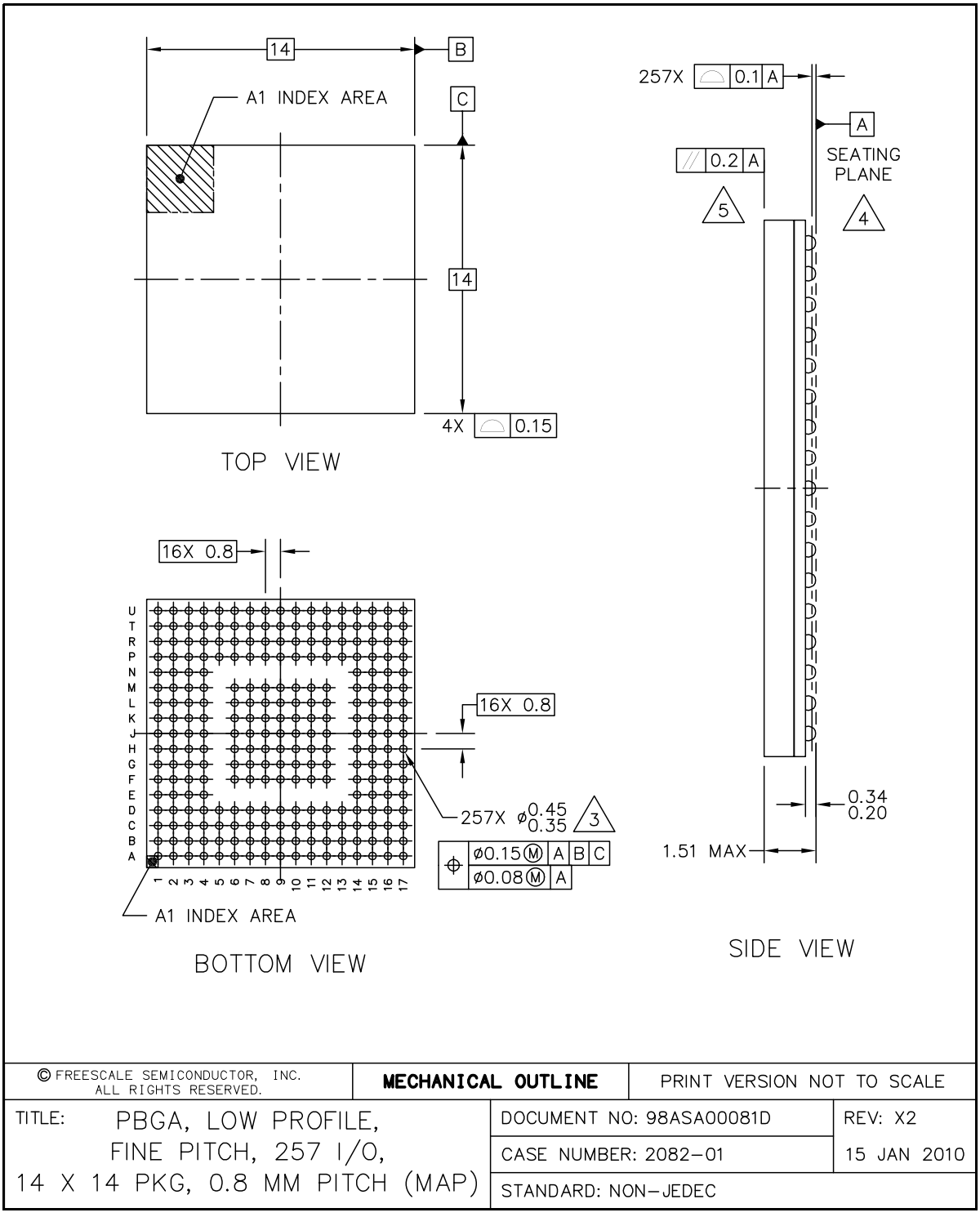

Figure 54. 257 MAPBGA mechanical data (1 of 2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00081D	REV: X2
	CASE NUMBER: 2082–01	15 JAN 2010
	STANDARD: NON–JEDEC	

Figure 55. 257 MAPBGA mechanical data (2 of 2)

Table 73. Revision history (continued)

Revision	Date	Description of Changes
6 (cont.)	6 Feb 2012	In Table 62 (External interrupt timing (GPIO IRQ)): • Changed T_{IPWL} min value from TBD to 3. • Changed T_{IPWH} min value from TBD to 3. • Changed T_{ICYC} min value from TBD to 6. • Changed all units from ns to t_{CYC}. In Table 71 (I^2C SCL and SDA input timing specifications), corrected the line numbering.
6.1	30 Mar 2012	No content changes, technical or editorial, were made in this revision. Change bars are identical to those in Rev. 6. Removed the “preliminary” footers throughout. Changed “Data Sheet: Advance Information” to “Data Sheet: Technical Data” on page 1. Removed the “product under development” disclaimer on page 1.
7	18 May 2012	Minor editorial changes and improvements throughout. In Section 1.3, Device comparison, Table 1 (MPC5675K family device comparison), changed the CPU/Data Cache entry from "16 KB, 4-way with EDC (SoR)" to "16 KB, 4-way with Parity (SoR)". In Section 1.3, Device comparison, Table 1 (MPC5675K family device comparison), added footnotes to stipulate the peripheral instances that are used on derivative devices: • Added footnote to **MPC5673K** DSPI module: “DSPI_0 and DSPI_1.“ • Added footnote to **MPC5673K** I2C module: “I2C_0 and I2C_1.“ • Added footnote to **MPC5673K** LinFlex module: “LinFlex_0, LinFlex_1, and LinFlex_2“ In Section 1.4, Block diagram: • Added missing modules (PMC, SPE2, VLE, and flash. • Added an arrow each from Core_0 and Core_1 to the XBAR modules to represent the data path. • Updated the Redundancy Checkers to reflect the actual implementation. • Renamed the “JTAG/Nexus” block to “Debug”, with JTAG and Nexus shown as submodules. In Section 1.5, Feature list, changed “Junction temperature sensor” to “Silicon substrate (die) temperature sensor”. In Section 1.6.1, High-performance e200z7d core processor and Section 1.6.9, Cache memory, removed the bullet “Supports tag and data parity" and added the following bullets: — Supports tag and data cache parity — Supports EDC for instruction cache In Section 1.6.19, System Timer Module (STM), changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)” In Section 1.6.20.2, Cross Triggering Unit (CTU), changed “DMA support with safety features” to “Supports safety measures using DMA”. In Section 1.6.21, Redundancy Control and Checker Unit (RCCU), changed “Duplicated module to guarantee highest possible diagnostic coverage (check of checker)” to “Duplicated module to enable high diagnostic coverage (check of checker)”. In Section 1.6.22, Software Watchdog Timer (SWT), • Changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)”. • Changed “Allows high level of safety (SIL3 monitor)” to “Provides measures to target high safety integrity levels (for example, SIL 3, ASIL D)”. In Section 1.6.25, Cyclic Redundancy Checker (CRC) unit, in the sentence “Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol”, changed “allow” to “support”.