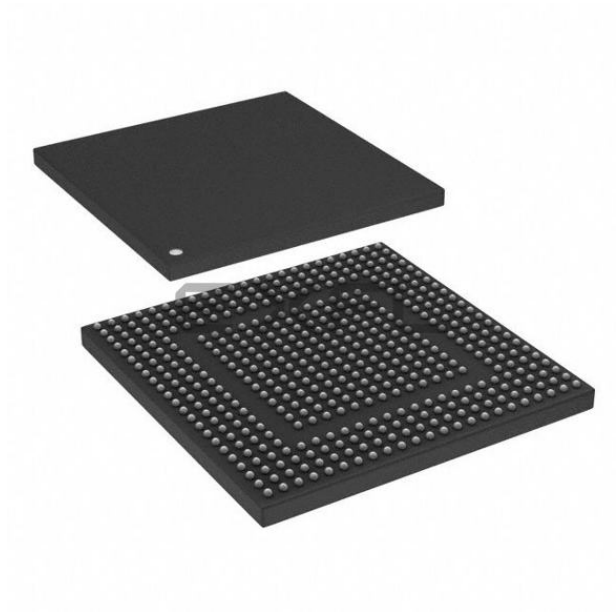

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7d
Core Size	32-Bit Dual-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexRay, I²C, LINbus, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	-
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.5V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	473-LFBGA
Supplier Device Package	473-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5675kff0vms2

- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM is supported
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for:
  - buffered output compare functions
  - input capture functions
- Enhanced dual-edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high and low limit registers
- Supports safety measures using DMA

1.6.20.2 Cross Triggering Unit (CTU)

The CTU provides automatic generation of ADC conversion requests on user-selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double-buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Maximum operating frequency lower than or equal to platform
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low-pass filter
- Double-buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double-buffered ADC command list pointers to minimize ADC trigger unit update
- Double-buffered ADC conversion command list with as many as twenty-four ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows controlling ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.6.20.3 Analog-To-Digital Converter (ADC)

- Four independent ADCs with 12-bit A/D resolution
- Common mode conversion range of 0–5 V or 0–3.3 V
- Twenty-two single-ended input channels
- Supports eight FIFO queues with fixed priority
- Queue modes with priority-based preemption; initiated by software command, internal, or external triggers
- DMA and interrupt request support

1.6.20.4 eTimer module

Three 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Ability to operate up to platform frequency
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - Equals peripheral clock/2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality is not in use
- DMA support

1.6.21 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

- Duplicated module to enable high diagnostic coverage (check of checker)
- Replicated IP to be used as checkers on the PBRIDGE output, Flash Controller output, SRAM output, DMA Channel Mux inputs

1.6.22 Software Watchdog Timer (SWT)

This module implements the features below:

- Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)
- Fault-tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog

Table 2. Pad types (continued)

Pad Type	Description
DRAM ACC	Bidirectional DDR pad. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM CLK	Differential clock driver.
DRAM DQ	Bidirectional DDR pad with integrated ODT. Can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.
DRAM ODT CTL	Enable On Die Termination control.
Analog	CMOS Schmitt trigger cell with injection proof analog switch.
Analog Shared	CMOS Schmitt trigger cell with two injection-proof analog switches.

2.2.2 Power supply and reference voltage pins

Table 3 shows the supply pins for the MPC5675K in the 257 MAPBGA package. Table 5 shows the supply pins for the MPC5675K in the 473 MAPBGA package.

Table 4 and Table 6 show the pins not populated on the MPC5675K 257 MAPBGA and 473 MAPBGA packages, respectively.

Table 3. 257 MAPBGA supply pins

Ball number	Ball name	Pad type	Ball number	Ball name	Pad type
V_{DD}					
A3	VDD_HV_IO	VDD_HV	F9	VDD_LV_COR	VDD_LV
A9	VDD_HV_IO	VDD_HV	F10	VDD_LV_COR	VDD_LV
B16	VDD_HV_IO	VDD_HV	F11	VDD_LV_COR	VDD_LV
C1	VDD_HV_IO	VDD_HV	F12	VDD_LV_COR	VDD_LV
G2	VDD_HV_IO	VDD_HV	G6	VDD_LV_COR	VDD_LV
M2	VDD_HV_IO	VDD_HV	G12	VDD_LV_COR	VDD_LV
P10	VDD_HV_IO	VDD_HV	H6	VDD_LV_COR	VDD_LV
P14	VDD_HV_IO	VDD_HV	H12	VDD_LV_COR	VDD_LV
T2	VDD_HV_IO	VDD_HV	J6	VDD_LV_COR	VDD_LV
T16	VDD_HV_IO	VDD_HV	J12	VDD_LV_COR	VDD_LV
L14	VDD_HV_DRAM_VREF	VDD_HV	K6	VDD_LV_COR	VDD_LV
D8	VDD_HV_FLA	VDD_HV	K12	VDD_LV_COR	VDD_LV
M1	VDD_HV_OSC	VDD_HV	L6	VDD_LV_COR	VDD_LV
D14	VDD_HV_PDI	VDD_HV	L12	VDD_LV_COR	VDD_LV
H16	VDD_HV_PDI	VDD_HV	M6	VDD_LV_COR	VDD_LV
U14	VDD_HV_PMU	VDD_HV	M7	VDD_LV_COR	VDD_LV
R7	VDD_HV_ADR_13	VDD_HV_A	M8	VDD_LV_COR	VDD_LV

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
L1	GPIO	nexus EVTO_B	A0: siul_GPIO[90] A1: _ A2: npc_wrapper_EVTO_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
L2	GPIO	nexus EVTI_B	A0: siul_GPIO[91] A1: _ A2: leo_sor_proxy_EVTI_B A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
L3	GPIO	dspi2 SCK	A0: siul_GPIO[11] A1: dspi2_SCK A2: _ A3: _	I: can3_RXD I: _ I: siul_EIRQ[10]	—	disabled	GP Slow/ Medium	VDD_HV_IO
L4	GPIO	nexus MDO[13][1]	A0: siul_GPIO[218] A1: _ A2: npc_wrapper_MDO[13] A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
L16	GPIO	flexpwm0 B[1]	A0: siul_GPIO[150] A1: dramc_CS0 A2: ebi_TS A3: flexpwm0_B[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
L17	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
M3	GPIO	dspi1 CS2	A0: siul_GPIO[56] A1: dspi1_CS2 A2: _ A3: dspi0_CS5	I: flexpwm0_FAULT[3] I: lin2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
M4	GPIO	nexus MDO[12][1]	A0: siul_GPIO[217] A1: _ A2: npc_wrapper_MDO[12] A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
M14	GPIO	flexpwm0 B[2]	A0: siul_GPIO[152] A1: dramc_CAS A2: ebi_WE_BE_1 A3: flexpwm0_B[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
M15	GPIO	TDI	A0: siul_GPIO[21] A1: _ A2: _ A3: _	I: jtagc_TDI I: _ I: _	—	pullup	GP Slow/ Medium	VDD_HV_IO
M17	GPIO	flexpwm1 A[1]	A0: siul_GPIO[157] A1: dramc_ODT A2: ebi_CS1 A3: flexpwm1_A[1]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N3	GPIO	dspi0 CS3	A0: siul_GPIO[53] A1: dspi0_CS3 A2: i2c2_clock A3: _	I: flexpwm0_FAULT[2] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
N14	GPIO	flexpwm0 B[3]	A0: siul_GPIO[154] A1: dramc_BA[0] A2: ebi_WE_BE_3 A3: flexpwm0_B[3]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N15	GPIO	flexpwm0 A[2]	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N16	GPIO	flexpwm1 A[0]	A0: siul_GPIO[155] A1: dramc_BA[1] A2: ebi_BDIP A3: flexpwm1_A[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
N17	GPIO	flexpwm1 B[0]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_IO
P3	GPIO	dspi0 CS2	A0: siul_GPIO[54] A1: dspi0_CS2 A2: i2c2_data A3: _	I: flexpwm0_FAULT[1] I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
P5	GPIO	etimer1 ETC[1]	A0: siul_GPIO[45] A1: etimer1_ETC[1] A2: _ A3: _	I: ctu0_EXT_IN I: flexpwm0_EXT_SYNC I: ctu1_EXT_IN	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 9. 257 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional inputs	Analog inputs	Weak pull during reset	Pad type	Power domain
T3	GPIO	dspi2 SOUT	A0: siul_GPIO[12] A1: dspi2_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[11]	—	disabled	GP Slow/ Medium	VDD_HV_IO
T4	ANA	adc3 AN[0]	—	siul_GPI[229]	AN: adc3_AN[0]	—	Analog	VDD_HV_ADR13
T5	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	Analog	VDD_HV_ADR13
T6	ANA	adc2 AN[2]	—	siul_GPI[223]	AN: adc2_AN[2]	—	Analog	VDD_HV_ADR02
T8	ANA	adc2_adc3 AN[13]	—	siul_GPI[227]	AN: adc2_adc3_AN[13]	—	Analog Shared	VDD_HV_ADR02
T10	ANA	adc0 AN[1]	—	siul_GPI[24] etimer0_ETC[5]	AN: adc0_AN[1]	—	Analog	VDD_HV_ADR02
T11	ANA	adc0_adc1 AN[12]	—	siul_GPI[26]	AN: adc0_adc1_AN[12]	—	Analog Shared	VDD_HV_ADR02
T12	ANA	adc1 AN[0]	—	siul_GPI[29] lin1_RXD	AN: adc1_AN[0]	—	Analog	VDD_HV_ADR13
T13	ANA	adc1 AN[2]	—	siul_GPI[31] siul_EIRQ[20]	AN: adc1_AN[2]	—	Analog	VDD_HV_ADR13
T14	GPIO	lin0 RXD	A0: siul_GPIO[19] A1: _ A2: i2c0_data A3: sscm_DEBUG[3]	I: lin0_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
E23	GPIO	dramc BA[2]	A0: siul_GPIO[156] A1: dramc_BA[2] A2: ebi_CS0 A3: flexpwm1_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F1	GPIO	nexus MDO[10][1]	A0: siul_GPIO[109] A1: _ A2: npc_wrapper_MDO[10] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F2	GPIO	nexus MDO[11][1]	A0: siul_GPIO[108] A1: _ A2: npc_wrapper_MDO[11] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F3	GPIO	nexus MDO[6][1]	A0: siul_GPIO[113] A1: _ A2: npc_wrapper_MDO[6] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F4	GPIO	nexus MDO[4][1]	A0: siul_GPIO[115] A1: _ A2: npc_wrapper_MDO[4] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
F20	GPIO	dramc RAS	A0: siul_GPIO[151] A1: dramc_RAS A2: ebi_WE_BE_0 A3: flexpwm0_A[2]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F21	GPIO	siul GPIO[194]	A0: siul_GPIO[194] A1: flexpwm0_X[0] A2: ebi_AD28 A3: _	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F22	GPIO	siul GPIO[148]	A0: siul_GPIO[148] A1: _ A2: ebi_CLKOUT A3: flexpwm0_B[0]	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
F23	GPIO	dramc D[5]	A0: siul_GPIO[179] A1: dramc_D[5] A2: ebi_AD13 A3: ebi_ADD29	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
J23	GPIO	dramc D[6]	A0: siul_GPIO[180] A1: dramc_D[6] A2: ebi_AD14 A3: ebi_ADD30	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K1	GPIO	dspi0 SCK	A0: siul_GPIO[37] A1: dspi0_SCK A2: _ A3: sscm_DEBUG[5]	I: flexpwm0_FAULT[3] I: _ I: siul_EIRQ[23]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K2	GPIO	dspi1 CS0	A0: siul_GPIO[5] A1: dspi1_CS0 A2: _ A3: dspi0_CS7	I: _ I: _ I: siul_EIRQ[5]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K3	GPIO	dspi1 SCK	A0: siul_GPIO[6] A1: dspi1_SCK A2: _ A3: _	I: _ I: _ I: siul_EIRQ[6]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K4	GPIO	dspi1 SOUT	A0: siul_GPIO[7] A1: dspi1_SOUT A2: _ A3: _	I: _ I: _ I: siul_EIRQ[7]	—	disabled	GP Slow/ Medium	VDD_HV_IO
K21	GPIO	dramc D[4]	A0: siul_GPIO[178] A1: dramc_D[4] A2: ebi_AD12 A3: ebi_ADD28	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K22	GPIO	dramc D[8]	A0: siul_GPIO[182] A1: dramc_D[8] A2: ebi_AD16 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
K23	GPIO	dramc D[9]	A0: siul_GPIO[183] A1: dramc_D[9] A2: ebi_AD17 A3: _	I: _ I: _ I: _	—	disabled	DRAM DQ	VDD_HV_DRAM
L1	GPIO	dspi0 CS0	A0: siul_GPIO[36] A1: dspi0_CS0 A2: _ A3: sscm_DEBUG[4]	I: _ I: _ I: siul_EIRQ[22]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
T2	GPIO	flexpwm1 A[0]	A0: siul_GPIO[117] A1: flexpwm1_A[0] A2: _ A3: can2_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T3	GPIO	flexpwm1 A[1]	A0: siul_GPIO[120] A1: flexpwm1_A[1] A2: _ A3: can3_TXD	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
T20	GPIO	dramc ADD[8]	A0: siul_GPIO[166] A1: dramc_ADD[8] A2: ebi_AD0 A3: ebi_ADD16	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T21	GPIO	dramc ADD[9]	A0: siul_GPIO[167] A1: dramc_ADD[9] A2: ebi_AD1 A3: ebi_ADD17	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
T22	GPIO	dramc ADD[1]	A0: siul_GPIO[159] A1: dramc_ADD[1] A2: ebi_ADD9 A3: ebi_CS3	I: _ I: _ I: _	—	disabled	DRAM ACC	VDD_HV_DRAM
U1	GPIO	flexpwm1 B[0]	A0: siul_GPIO[118] A1: flexpwm1_B[0] A2: _ A3: _	I: can2_RXD I: can3_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U2	GPIO	flexpwm1 B[1]	A0: siul_GPIO[121] A1: flexpwm1_B[1] A2: _ A3: _	I: can3_RXD I: can2_RXD I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U3	GPIO	flexpwm1 A[2]	A0: siul_GPIO[123] A1: flexpwm1_A[2] A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
U4	GPIO	dspi2 SCK	A0: siul_GPIO[11] A1: dspi2_SCK A2: _ A3: _	I: can3_RXD I: _ I: siul_EIRQ[10]	—	disabled	GP Slow/ Medium	VDD_HV_IO

Table 10. 473 MAPBGA pin multiplexing (continued)

Ball number	Ball type	Ball name	Alternate I/O	Additional Inputs	Analog Inputs	Weak pull during reset	Pad type	Power domain
AB15	ANA	adc1 AN[1]	—	siul_GPI[30] etimer0_ETC[4] siul_EIRQ[19]	AN: adc1_AN[1]	—	Analog	VDD_HV_ADR1
AB16	ANA	adc1 AN[3]	—	siul_GPI[32]	AN: adc1_AN[3]	—	Analog	VDD_HV_ADR1
AB17	ANA	adc1 AN[4]	—	siul_GPI[75]	AN: adc1_AN[4]	—	Analog	VDD_HV_ADR1
AB18	GPIO	TDO	A0: siul_GPIO[20] A1: jtagc_TDO A2: _ A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Fast	VDD_HV_IO
AB21	GPIO	lin1 RXD	A0: siul_GPIO[95] A1: _ A2: i2c1_data A3: _	I: lin1_RXD I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC3	GPIO	dspi2 SIN	A0: siul_GPIO[13] A1: _ A2: _ A3: _	I: dspi2_SIN I: flexpwm0_FAULT[0] I: siul_EIRQ[12]	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC4	GPIO	flexpwm1 A[3]	A0: siul_GPIO[126] A1: flexpwm1_A[3] A2: etimer2_ETC[4] A3: dspi0_CS7	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC5	GPIO	flexpwm1 B[3]	A0: siul_GPIO[127] A1: flexpwm1_B[3] A2: etimer2_ETC[5] A3: _	I: _ I: _ I: _	—	disabled	GP Slow/ Medium	VDD_HV_IO
AC6	ANA	adc3 AN[3]	—	siul_GPI[232]	AN: adc3_AN[3]	—	GP Slow/ Medium	VDD_HV_ADR23
AC9	ANA	adc2 AN[3]	—	siul_GPI[224]	AN: adc2_AN[3]	—	Analog	VDD_HV_ADR23

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

The “Symbol” column of the electrical parameter and timings tables may contain an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the *input* voltage of a voltage regulator.
- “CC” identifies specifications that define normal device operation. Where available, the letters “P”, “C”, “T”, or “D” replace the letter “CC” and apply to these controller characteristics. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 11. Absolute maximum ratings[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	$V_{DD\_HV\_PMU}$	SR	Voltage regulator supply voltage	—	–0.3	5.5[2]	V
2	$V_{SS\_HV\_PMU}$	SR	Voltage regulator supply ground	—	–0.1	0.1	V
3	$V_{DD\_HV\_IO}$	SR	Input/output supply voltage	—	–0.3	3.6[3,4]	V
4	$V_{SS\_HV\_IO}$	SR	Input/output supply ground	—	–0.1	0.1	V
5	$V_{DD\_HV\_FLA}$	SR	Flash supply voltage	—	–0.3	3.6[3,4]	V
6	$V_{SS\_HV\_FLA}$	SR	Flash supply ground	—	–0.1	0.1	V
7	$V_{DD\_HV\_OSC}$	SR	Crystal oscillator amplifier supply voltage	—	–0.3	3.6[3,4]	V
8	$V_{SS\_HV\_OSC}$	SR	Crystal oscillator amplifier supply ground	—	–0.1	0.1	V
9	$V_{DD\_HV\_PDI}$	SR	PDI interface supply voltage	—	–0.3	3.6[3,4]	V
10	$V_{SS\_HV\_PDI}$	SR	PDI interface supply ground	—	–0.1	0.1	V
11	$V_{DD\_HV\_DRAM}$[5]	SR	DRAM interface supply voltage	—	–0.3	3.6[3,4]	V
12	$V_{SS\_HV\_DRAM}$	SR	DRAM interface supply ground	—	–0.1	0.1	V
13	$V_{DD\_HV\_ADRx}$[6]	SR	ADC*x* high reference voltage	—	–0.3	6.0	V
14	$V_{SS\_HV\_ADRx}$	SR	ADC*x* low reference voltage	—	–0.1	0.1	V
15	$V_{DD\_HV\_ADV}$	SR	ADC supply voltage	—	–0.3	3.6[3,4]	V
16	$V_{SS\_HV\_ADV}$	SR	ADC supply ground	—	–0.1	0.1	V
17	$V_{DD\_LV\_COR}$	SR	Core supply voltage digital logic	—	–0.3	1.32[7]	V

3.15.2 Read access timing

Table 28. Code flash read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{READ}	CC	Maximum frequency for Flash reading (system clock frequency SYS_CLK)	4 wait states	90	MHz
2				3 wait states	60	MHz

Table 29. Data flash read access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{READ}	CC	Maximum frequency for Flash reading (system clock frequency SYS_CLK)	12 wait states	90	MHz
2				8 wait states	60	MHz

3.15.3 Write access timing

Table 30. Code flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	—	90	MHz

Table 31. Data flash write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	f_{WRITE}	CC	Maximum frequency for Flash writing (system clock frequency SYS_CLK)	—	90	MHz

3.16 SRAM memory electrical characteristics

Table 32. System SRAM memory read/write access timing

No.	Symbol		Parameter	Condition	Value	Unit
					Max	
1	$s_{READ/WRITE}$	CC	Maximum frequency for system SRAM reading/writing (system clock frequency SYS_CLK)	1 wait state	90	MHz

– 150 Ω

The electrical data provided in Section 3.19, DRAM pad specifications, applies to the pads listed in Table 39.

Table 39. DRAM pads

Name	Voltage	Used For	Notes[1]
DRAM ACC	1.62 V–3.6 V	I/O	Bidirectional DDR pad
DRAM CLK	1.62 V–3.6 V	O	Output only differential clock driver pad
DRAM DQ	1.62 V–3.6 V	I/O	Bidirectional DDR pad with integrated ODT

1 All pads can be configured to support LPDDR half strength, LPDDR full strength, DDR1, DDR2 half strength, DDR2 full strength, and SDR.

All three pad types can be configured to support SDR, DDR, DDR2 half and full strength, and LPDDR half and full strength modes, according to Table 40.

Table 40. Mode configuration for DRAM pads

Configuration[1]	Mode
000	1.8 V LPDDR Half Strength
001	1.8 V LPDDR Full Strength
010	1.8 V DDR2 Half Strength
011	2.5 V DDR
100	Not supported
101	Not supported
110	1.8 V DDR2 Full Strength
111	SDR

1 Configuration is selected in the corresponding PCR registers of the SIUL.

NOTE

0.7 V overshoot/undershoot can be allowed to occur repeatedly throughout the product expected lifetime and will not cause any long term reliability issue.

3.19.1 DRAM pads electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

Table 41. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	3.0	3.6	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	1.3	1.7	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ − 0.05	$V_{DD\_HV\_DRAM\_VREF}$ + 0.05	V
4	V_{IH}	CC	Input high voltage	—	$V_{DD\_HV\_DRAM\_VREF}$ + 0.20	—	V

Table 41. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V) (continued)

No.	Symbol		Parameter	Condition	Min	Max	Unit
5	V_{IL}	CC	Input low voltage	—		$V_{DD\_HV\_DRAM\_VREF}$ – 0.2	V
6	V_{OH}	CC	Output high voltage	—	$V_{DD\_HV\_DRAM\_VTT}$ + 0.8	—	V
7	V_{OL}	CC	Output low voltage	—	—	$V_{DD\_HV\_DRAM\_VTT}$ – 0.8	V

1 BGA473: Termination voltage can be supplied via package pins. BGA257 termination voltage internally tied as the BGA257 does not provide DRAM interface. Disable ODT.

Table 42. Output drive current @ V_{DDE} = 3.3 V (±10%)

No.	Pad Name	Drive Mode	Minimum I_{OH} (mA)[1]	Minimum I_{OL} (mA)[2]
1	DRAM ACC	111	–16	16
2	DRAM DQ			
3	DRAM CLK			

1 I_{OH} is defined as the current sourced by the pad to drive the output to V_{OH}.

2 I_{OL} is defined as the current sunk by the pad to drive the output to V_{OL}.

Table 43. DRAM pads AC electrical specifications ($V_{DD\_HV\_DRAM}$ = 3.3 V)

No.	Pad Name	Prop. Delay (ns) L → H/H → L[1]		Output Slew rate Rise/Fall (V/ns)		Drive Load (pF)	Drive/Slew Rate Select
		Min	Max	Min	Max		MSB, LSB
1	DRAM ACC	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
2	DRAM DQ	1.4/1.4	2.4/2.4	3.1/2.5	5.6/5.4	5	111
		1.7/1.7	2.7/2.7	0.9/1.1	1.7/2.0	20	111
3	DRAM CLK	1.4/1.4	2.4/2.4	3.1/2.5	5.7/5.7	5	111
		1.6/1.6	2.6/2.6	1.1/1.3	2.3/2.3	20	111

1 L → H signifies low-to-high propagation delay and H → L signifies high-to-low propagation delay.

3.19.2 DRAM pads electrical specification ($V_{DD\_HV\_DRAM}$ = 2.5 V)

Table 44. DRAM pads DC electrical specifications ($V_{DD\_HV\_DRAM}$ = 2.5 V)

No.	Symbol		Parameter	Condition	Min	Max	Unit
1	$V_{DD\_HV\_DRAM}$	SR	I/O supply voltage	—	2.3	2.7	V
2	$V_{DD\_HV\_DRAM\_VREF}$	CC	Input reference voltage	—	0.49 × $V_{DD\_HV\_DRAM}$	0.51 × $V_{DD\_HV\_DRAM}$	V
3	$V_{DD\_HV\_DRAM\_VTT}$	CC	Termination voltage[1]	—	$V_{DD\_HV\_DRAM\_VREF}$ – 0.04	$V_{DD\_HV\_DRAM\_VREF}$ + 0.04	V

8 If $\overline{\text{RESET}}$ is configured for short reset.

9 Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.21.4 Reset sequence—start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.21.4.1 Internal VREG mode

Figure 17 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*. The last voltage rail crossing the levels shown in Figure 17 determines the start of the reset times specified in Table 52.

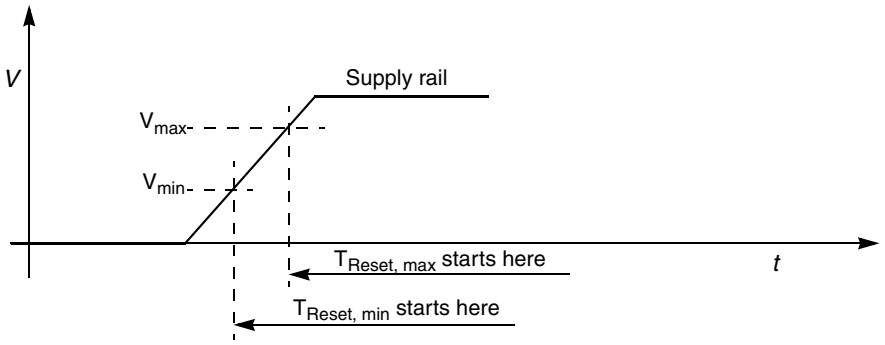


Figure 17. Reset sequence start in internal VREG mode

Table 54. Voltage thresholds

Variable name	Value
V_{min}	LvdReg – 3.5%
V_{max}	LvdReg + 3.5%
Supply Rail	VDD_HV_PMU VDD_HV_IO VDD_HV_FLASH VDD_HV_ADV

3.21.4.2 External VREG mode

Figure 18 and Figure 19 show the voltage thresholds that determine the start of the Destructive Reset Sequence, BIST enabled and the start for the Destructive Reset Sequence, BIST disabled.

NOTE

$\overline{\text{RESET\_SUP}}$ must not be released unless $V_{DD\_LV\_xxx}$ is within its valid range of operation. $\overline{\text{RESET\_SUP}}$ input circuitry needs a valid $V_{DD\_HV\_IO}$ rail in order to detect a high level on $\overline{\text{RESET\_SUP}}$.

JEDEC standards define the minimum set of requirements for compliant memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, MAY 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The MPC5675K supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strength (intended for lighter loads or point-to-point environments)

The MPC5675K memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the Section 3.19, DRAM pad specifications.

3.22.1.1 DDR and DDR2 SDRAM AC timing specifications

Table 55. DDR and DDR2 (DDR2-400) SDRAM timing specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

No.	Symbol		Parameter	Min	Max	Unit
1	t_{CK}	CC	Clock cycle time, CL = *x*	—	90	MHz
2	$V_{IX\text{-}AC}$	CC	MCK AC differential crosspoint voltage[1]	$V_{DD\_MEM\_IO}$ × 0.5 – 0.1	$V_{DD\_MEM\_IO}$ × 0.5 + 0.1	V
3	t_{CH}	CC	CK HIGH pulse width[1, 2]	0.47	0.53	t_{CK}
4	t_{CL}	CC	CK LOW pulse width[1, 2]	0.47	0.53	t_{CK}
5	t_{DQSS}	CC	Skew between MCK and DQS transitions[2, 3]	–0.25	0.25	t_{CK}
6	$t_{OS(base)}$	CC	Address and control output setup time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)		ps
7	$t_{OH(base)}$	CC	Address and control output hold time relative to MCK rising edge[2, 3]	(t_{CK}/2 – 750)	—	ps
8	$t_{DS1(base)}$	CC	DQ and DM output setup time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
9	$t_{DH1(base)}$	CC	DQ and DM output hold time relative to DQS[2, 3]	(t_{CK}/4 – 500)	—	ps
10	t_{DQSQ}	CC	DQS-DQ skew for DQS and associated DQ inputs[2]	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps

1 Measured with clock pin loaded with differential 100 Ω termination resistor.

2 All transitions measured at mid-supply ($V_{DD\_MEM\_IO}$/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

Figure 22 shows the DDR SDRAM write timing.

REVISION HISTORY

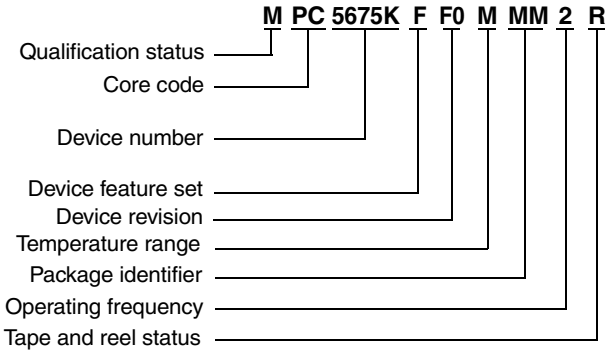
DOCUMENT NO: 98ASA00096D
PAGE: 2089
REV: O

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	D. VO	RELEASED FOR PRODUCTION	DSS	08 JUN 2009

TITLE:	CASE NUMBER: 2089–01	
473 I/O, FINE PITCH, PBGA, 19 X 19 PKG, 0.8MM PITCH (MAP)	STANDARD: NON–JEDEC	
	PACKAGE CODE:IN AGILE	SHEET: 3

Figure 58. 473 MAPBGA package mechanical data (3 of 3)

5 Orderable parts



Device feature set
F = FlexRay

Device revision
F0 = Fab and Mask

Temperature range
V = –40 °C to 105 °C
M = –40 °C to 125 °C (ambient)

Package identifier
MM = 257 BGA
MS= 473 BGA

Operating frequency
1 = 150 MHz
2 = 180 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Qualification status
P = Pre-qualification
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Note: Not all options are available on all devices.

6 Reference documents

1. Nexus (IEEE-ISTO 5001™—2008)
2. Measurement of emission of ICs—IEC 61967-2
3. Measurement of emission of ICs—IEC 61967-4
4. Measurement of immunity of ICs—IEC 62132-4
5. Semiconductor Equipment and Materials International
   3081 Zanker Road
   San Jose, CA 95134 USA
   (408) 943-6900
6. JEDEC specifications are available at http://www.jedec.org
7. MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.
8. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
9. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
10. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

7 Document revision history

Table 73 summarizes revisions to this document.

Beginning with Rev. 4, this revision history uses clickable cross-references for ease of navigation. The numbers and titles in each cross-reference are relative to the latest published release.

Table 73. Revision history (continued)

Revision	Date	Description of Changes
6 (cont.)	6 Feb 2012	In Table 62 (External interrupt timing (GPIO IRQ)): • Changed T_{IPWL} min value from TBD to 3. • Changed T_{IPWH} min value from TBD to 3. • Changed T_{ICYC} min value from TBD to 6. • Changed all units from ns to t_{CYC}. In Table 71 (I^2C SCL and SDA input timing specifications), corrected the line numbering.
6.1	30 Mar 2012	No content changes, technical or editorial, were made in this revision. Change bars are identical to those in Rev. 6. Removed the “preliminary” footers throughout. Changed “Data Sheet: Advance Information” to “Data Sheet: Technical Data” on page 1. Removed the “product under development” disclaimer on page 1.
7	18 May 2012	Minor editorial changes and improvements throughout. In Section 1.3, Device comparison, Table 1 (MPC5675K family device comparison), changed the CPU/Data Cache entry from "16 KB, 4-way with EDC (SoR)" to "16 KB, 4-way with Parity (SoR)". In Section 1.3, Device comparison, Table 1 (MPC5675K family device comparison), added footnotes to stipulate the peripheral instances that are used on derivative devices: • Added footnote to **MPC5673K** DSPI module: “DSPI_0 and DSPI_1.“ • Added footnote to **MPC5673K** I2C module: “I2C_0 and I2C_1.“ • Added footnote to **MPC5673K** LinFlex module: “LinFlex_0, LinFlex_1, and LinFlex_2“ In Section 1.4, Block diagram: • Added missing modules (PMC, SPE2, VLE, and flash. • Added an arrow each from Core_0 and Core_1 to the XBAR modules to represent the data path. • Updated the Redundancy Checkers to reflect the actual implementation. • Renamed the “JTAG/Nexus” block to “Debug”, with JTAG and Nexus shown as submodules. In Section 1.5, Feature list, changed “Junction temperature sensor” to “Silicon substrate (die) temperature sensor”. In Section 1.6.1, High-performance e200z7d core processor and Section 1.6.9, Cache memory, removed the bullet “Supports tag and data parity" and added the following bullets: — Supports tag and data cache parity — Supports EDC for instruction cache In Section 1.6.19, System Timer Module (STM), changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)” In Section 1.6.20.2, Cross Triggering Unit (CTU), changed “DMA support with safety features” to “Supports safety measures using DMA”. In Section 1.6.21, Redundancy Control and Checker Unit (RCCU), changed “Duplicated module to guarantee highest possible diagnostic coverage (check of checker)” to “Duplicated module to enable high diagnostic coverage (check of checker)”. In Section 1.6.22, Software Watchdog Timer (SWT), • Changed “Duplicated periphery to guarantee that safety targets (SIL3) are achieved” to “Replicated periphery to provide safety measures respective to high safety integrity levels (for example, SIL 3, ASIL D)”. • Changed “Allows high level of safety (SIL3 monitor)” to “Provides measures to target high safety integrity levels (for example, SIL 3, ASIL D)”. In Section 1.6.25, Cyclic Redundancy Checker (CRC) unit, in the sentence “Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol”, changed “allow” to “support”.

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