Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b84e0agf20000

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 24 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

Smart Card Interface (Max 2 Channels)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

AES Calculator

- AES (Advanced Encryption Standard) calculator is an AES common key crypto accelerator that is compliant with FIPS (Federal Information Processing Standard Publication) 197.
- Available key length: 128/192/256-bit
- CBC mode and ECB mode support

Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock: 4 MHz to 40 MHz
  - Sub clock: 32.768 kHz
  - Built-in high-speed CR clock: 4 MHz
  - Built-in low-speed CR clock: 100 kHz
  - Main PLL clock
- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

Clock Supervisor (CSV)

The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-Voltage Detector (LVD)

This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVDR: monitor Vcc and auto-reset operation
- LVD1: monitor Vcc and error reporting via an interrupt
- LVD2: selectable to monitor Vcc or LVDI and error reporting via an interrupt

Low Power Consumption Mode

This series has six low power consumption modes.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable between keeping the value of RAM and not)
- Deep standby Stop (selectable between keeping the value of RAM and not)

4. List of Pin Functions

List of Pin Numbers

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
1	1	1	VCC	-	
2	2	2	P50	Q	X
			SIN3_1		
			INT00_0		
			VV4		
3	3	3	P51	Q	X
			SOT3_1		
			INT01_0		
			VV3		
4	4	4	P52	Q	X
			SCK3_1		
			INT02_0		
			VV2		
5	5	5	P53	Q	X
			SIN6_0		
			TIOA1_2		
			INT07_2		
			VV1		
6	6	6	P54	Q	X
			SOT6_0		
			TIOB1_2		
			INT18_1		
			VV0		
7	7	7	P55	L	S
			SCK6_0		
			ADTG_1		
			INT19_1		
			SEG39		
8	8	8	P56	L	U
			MI2SMCK6_1		
			CEC1_1		
			INT08_2		
			WKUP9		
			SEG38		
	-	-	SIN1_0		
9	-	-	P57	F	I
			SOT1_0		
10	-	-	P58	F	I
			SCK1_0		
11	-	-	P59	F	J
			SIN7_0		
			INT16_1		

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-
	SIN3_1		2	2	2
	SIN3_2		94	79	63
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I^2C pin (operation mode 4).	109	-	-
	SOT3_1 (SDA3_1)		3	3	3
	SOT3_2 (SDA3_2)		92	77	61
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I^2C pin (operation mode 4).	108	-	-
	SCK3_1 (SCL3_1)		4	4	4
	SCK3_2 (SCL3_2)		96	81	65
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	102	87	67
	SIN4_1		76	66	56
	SIN4_2		97	82	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I^2C pin (operation mode 4).	99	84	66
	SOT4_1 (SDA4_1)		77	67	57
	SOT4_2 (SDA4_2)		98	83	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I^2C pin (operation mode 4).	107	92	72
	SCK4_1 (SCL4_1)		78	68	-
	SCK4_2 (SCL4_2)		99	84	66
	CTS4_0	Multi-function serial interface ch4 CTS input pin	106	91	71
	CTS4_1		79	69	-
	CTS4_2		100	85	-
	RTS4_0	Multi-function serial interface ch4 RTS input pin	105	90	70
	RTS4_1		80	70	-
	RTS4_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator controlling RTO00 to RTO05 outputs of Multi-function Timer 0.	23	18	13
	DTTI0X_1		79	69	-
	DTTI0X_2		115	95	75
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	18	13	-
	FRCK0_1		80	70	-
	FRCK0_2		63	53	43
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	22	17	-
	IC00_1		75	65	55
	IC00_2		64	54	44
	IC01_0		21	16	-
	IC01_1		76	66	56
	IC01_2		65	55	45
	IC02_0		20	15	-
	IC02_1		77	67	57
	IC02_2		66	56	46
	IC03_0		19	14	-
	IC03_1		78	68	-
	IC03_2		67	57	47
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	24	19	14
	RTO00_1 (PPG00_1)		86	71	58
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	25	20	15
	RTO01_1 (PPG00_1)		85	-	-
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	26	21	16
	RTO02_1 (PPG02_1)		84	-	-
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	27	22	17
	RTO03_1 (PPG02_1)		83	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	28	23	18
	RTO04_1 (PPG04_1)		82	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	29	24	19
	RTO05_1 (PPG04_1)		81	-	-
	IGTRG0_0	PPG IGBT mode external trigger input pin	48	43	33
	IGTRG0_1		116	96	76

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	REGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

*: PE0 is an open drain pin, cannot output high.

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

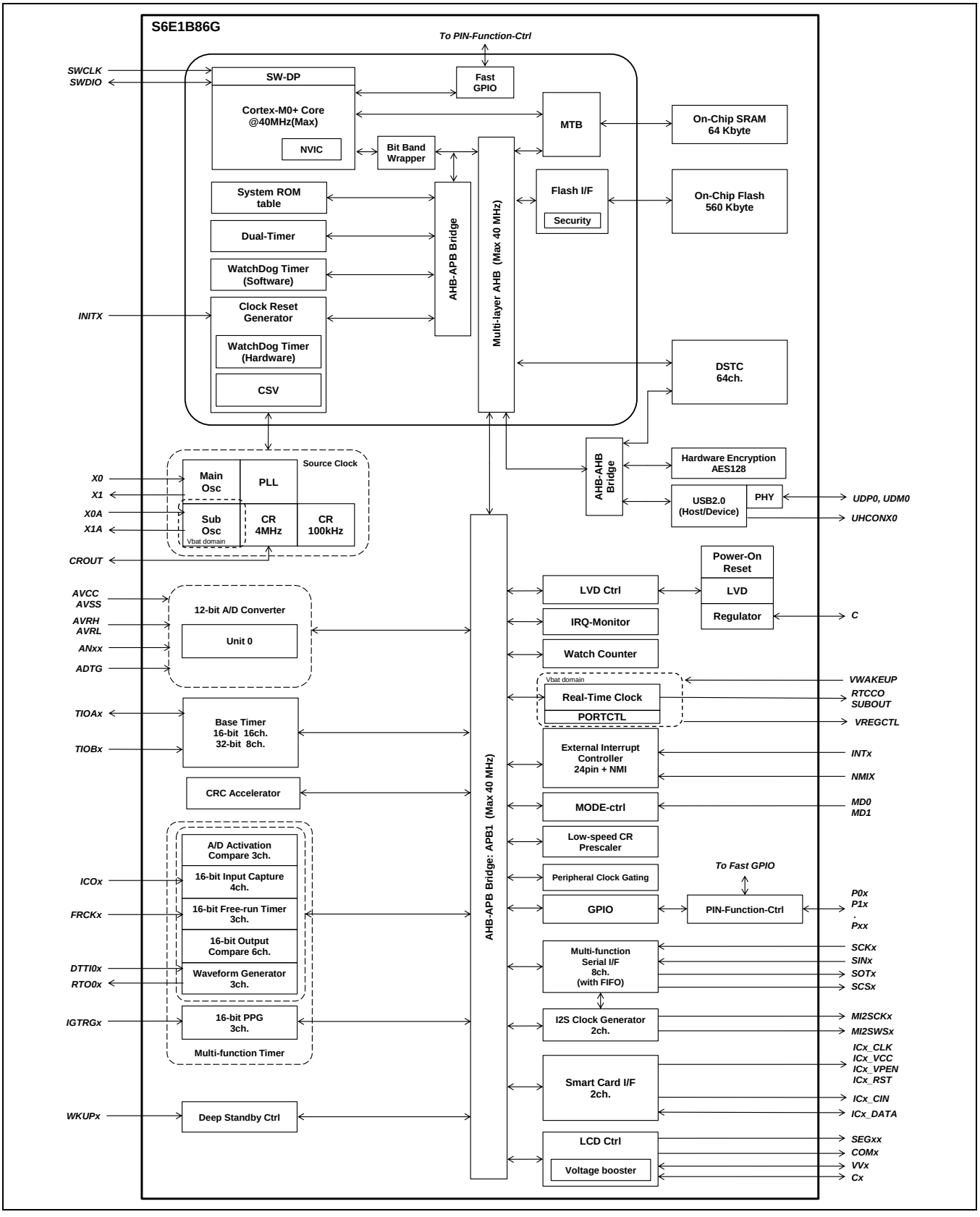
Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

8. Block Diagram



Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
U	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled						Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0
V	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCH} (VCC)	Stop mode	T_A=25°C V_{CC}=3.3 V	10	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V	9	TBD	µA	*1
			T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
	I_{CCT} (VCC)	Sub timer mode	T_A=25°C V_{CC}=3.3 V 32 kHz Crystal oscillation	13	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V 32 kHz Crystal oscillation	12	TBD	µA	*1
			T_A=105°C V_{CC}=3.6 V 32 kHz Crystal oscillation	-	TBD	µA	*1
	I_{CCR} (VCC)	RTC mode	T_A=25°C V_{CC}=3.3 V 32 kHz Crystal oscillation	10.5	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V 32 kHz Crystal oscillation	9.5	TBD	µA	*1
			T_A=105°C V_{CC}=3.6 V 32 kHz Crystal oscillation	-	TBD	µA	*1

*1: All ports are fixed. LVD off. Flash off.

11.4 AC Characteristics

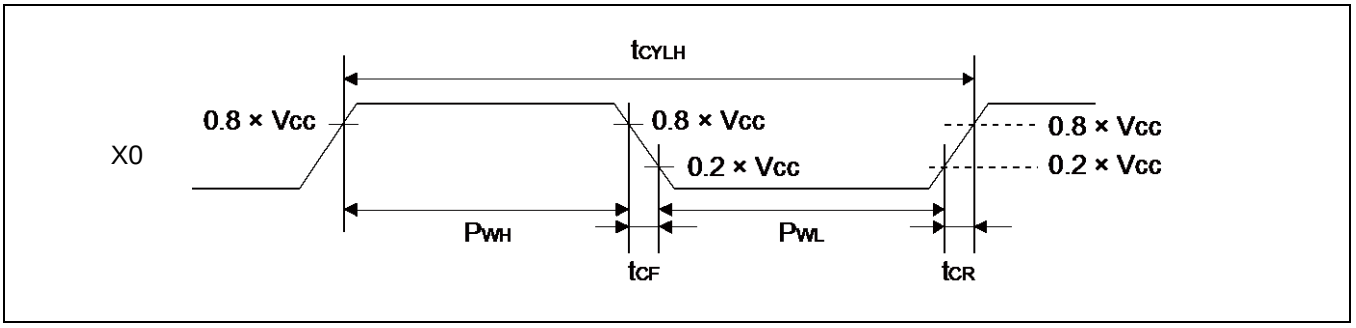
11.4.1 Main Clock Input Characteristics

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥ 2.7 V	4	48	MHz	When the crystal oscillator is connected
			V_{CC} < 2.7 V	4	20		
			-	4	48	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	f_{CM}	-	-	-	40.8	MHz	Master clock
	f_{CC}	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40.8	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40.8	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.5	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".

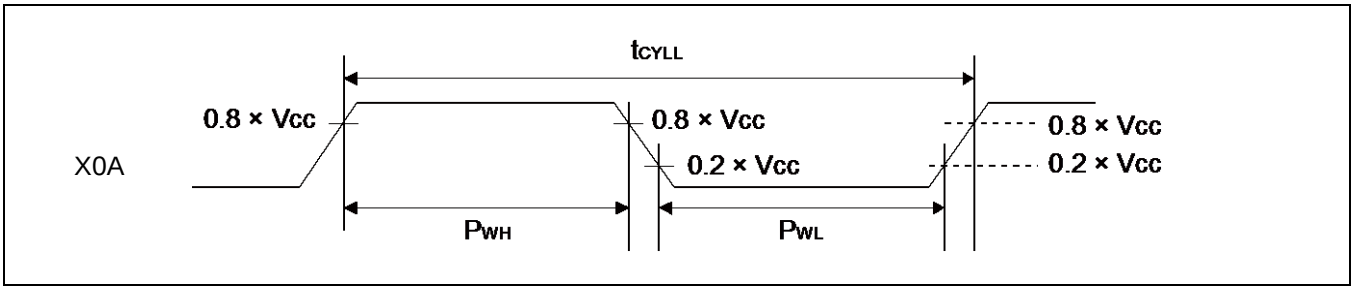


11.4.2 Sub Clock Input Characteristics

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected*
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



11.4.9 CSIO/SPI/UART Timing

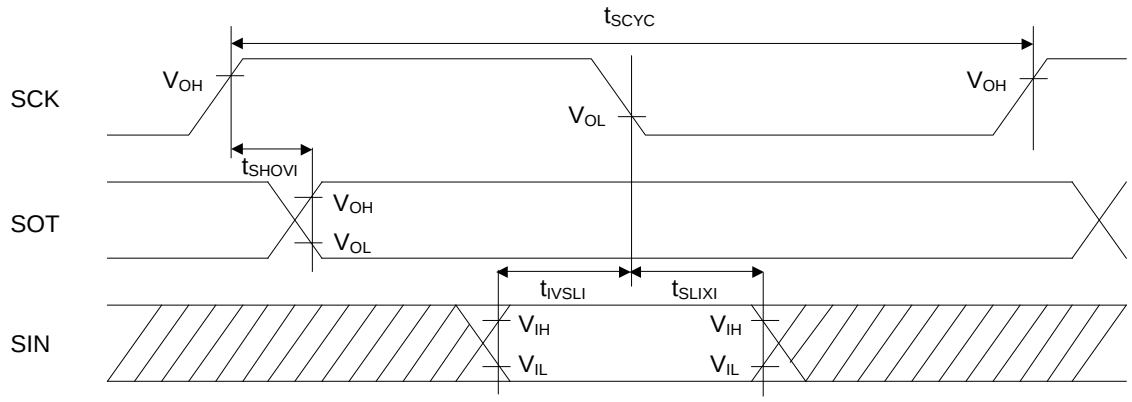
CSIO (SPI=0, SCINV=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

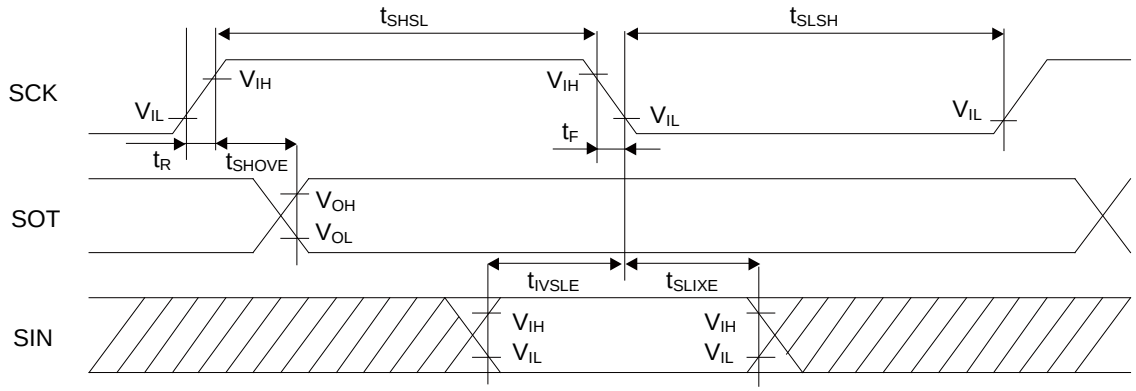
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≧ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		60	-	50	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} +10	-	t_{CYCP} +10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

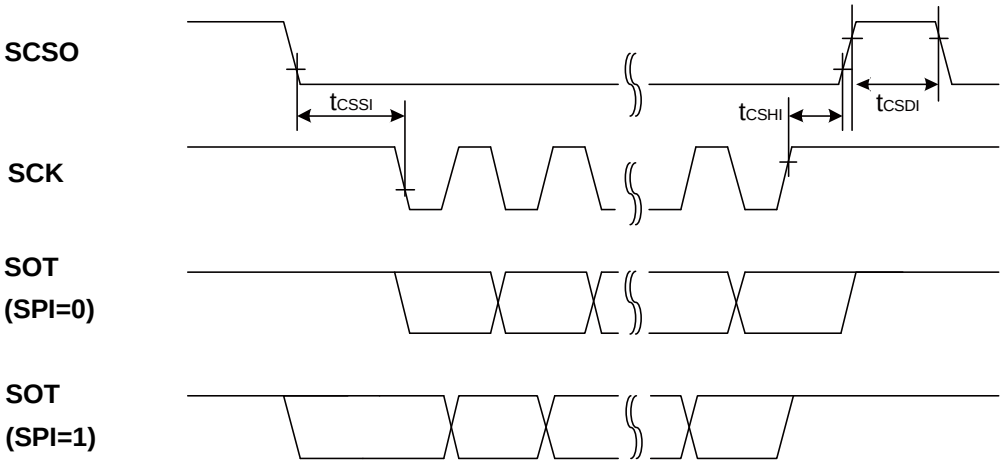
- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



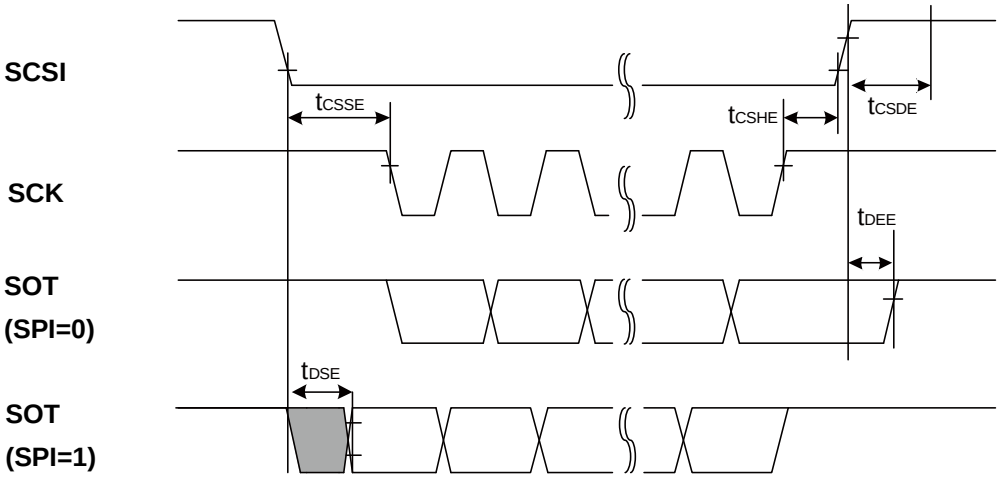
Master mode



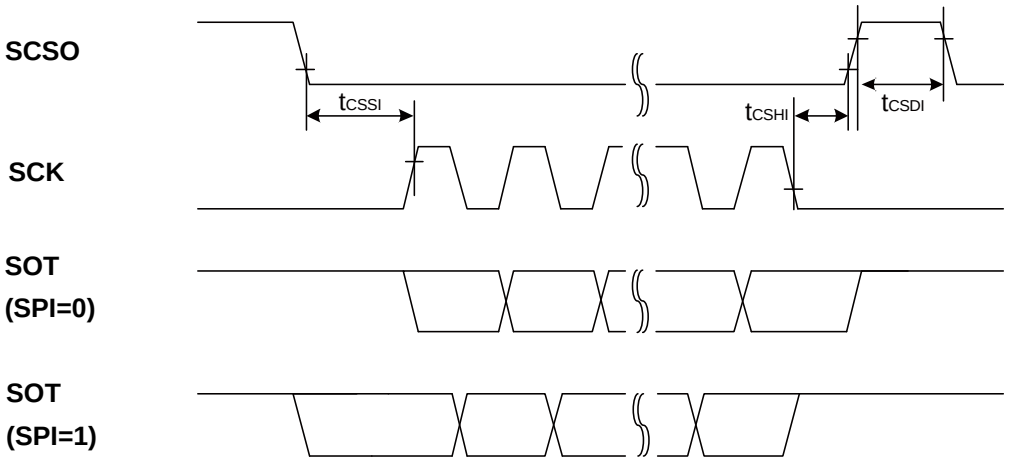
Slave mode



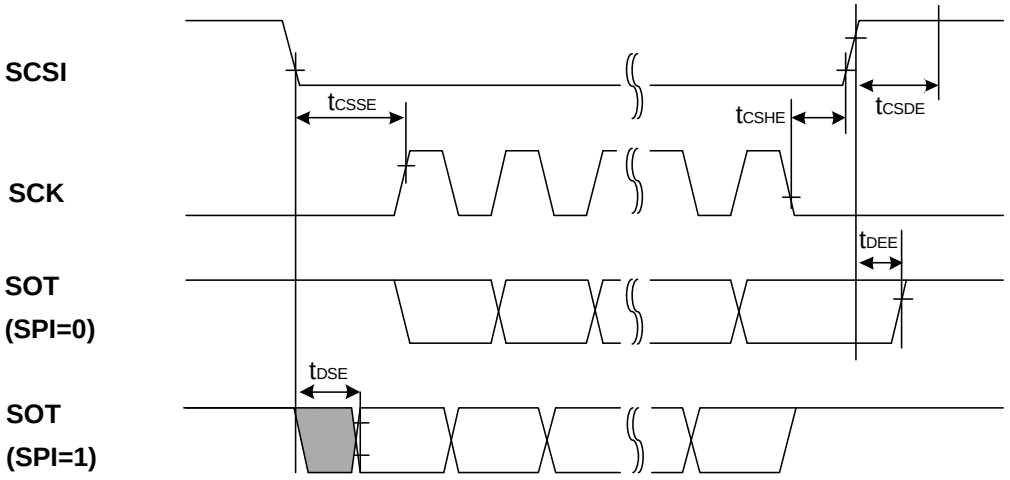
Master mode



Slave mode



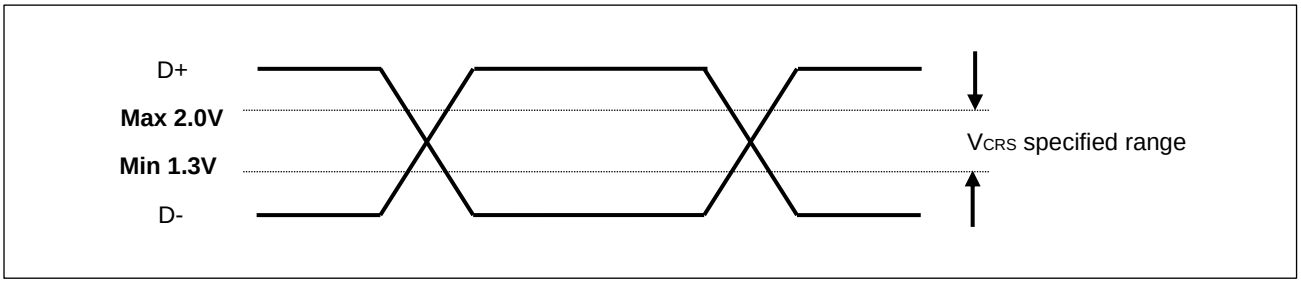
Master mode



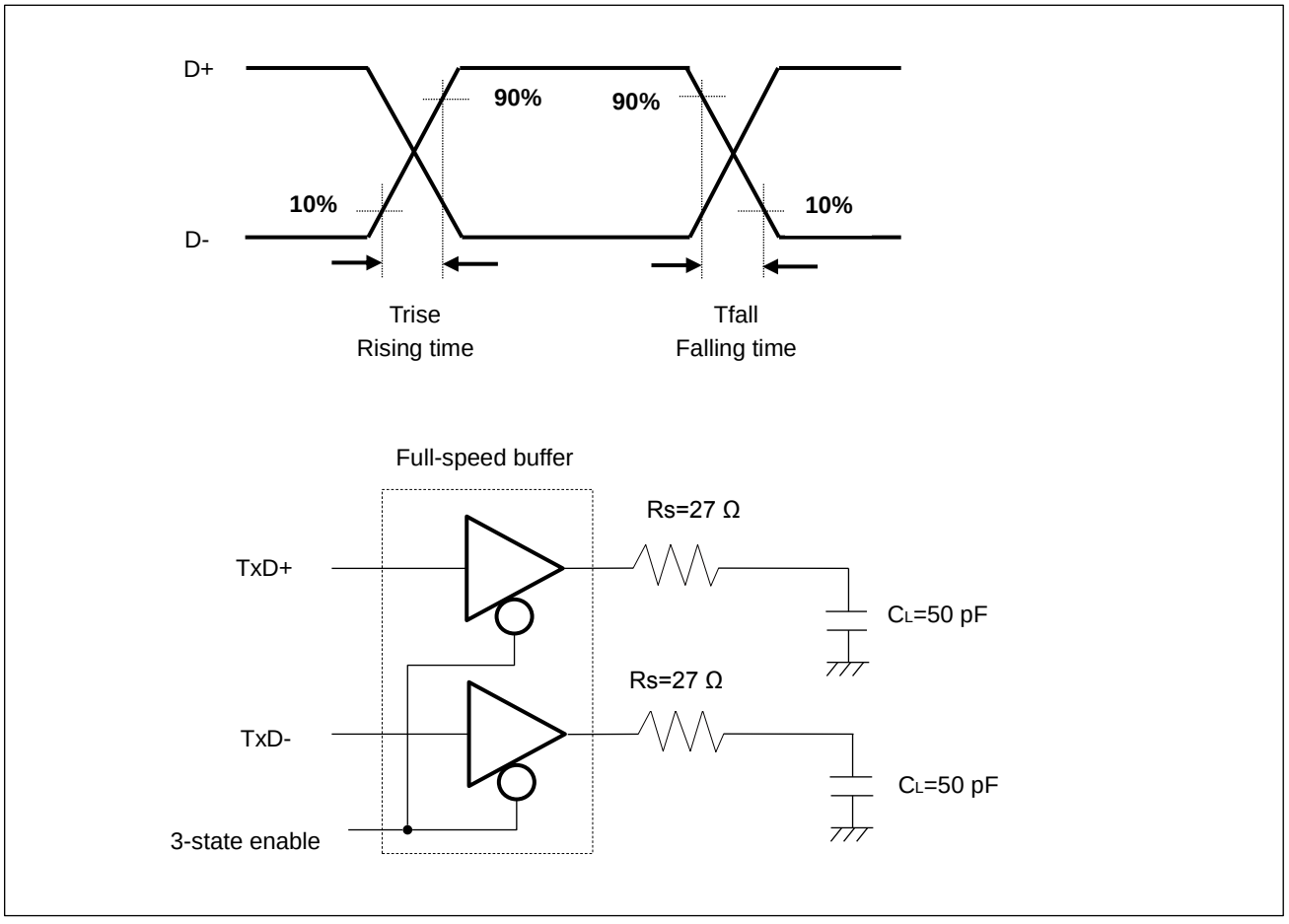
Slave mode

*3 : The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the VSS and 1.5 kΩ load) at high-state (V_{OH})

*4 : The cross voltage of the external differential output signal (D+ / D-) of USB I/O buffer is within 1.3 V to 2.0 V.

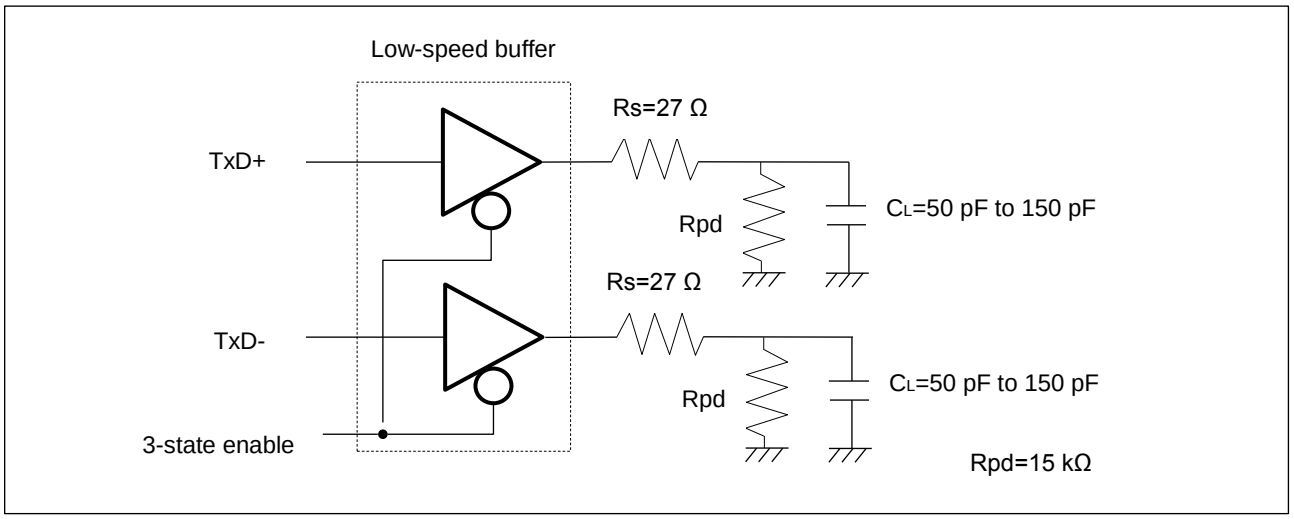


*5 : The indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ±10% to minimize RFI emission.

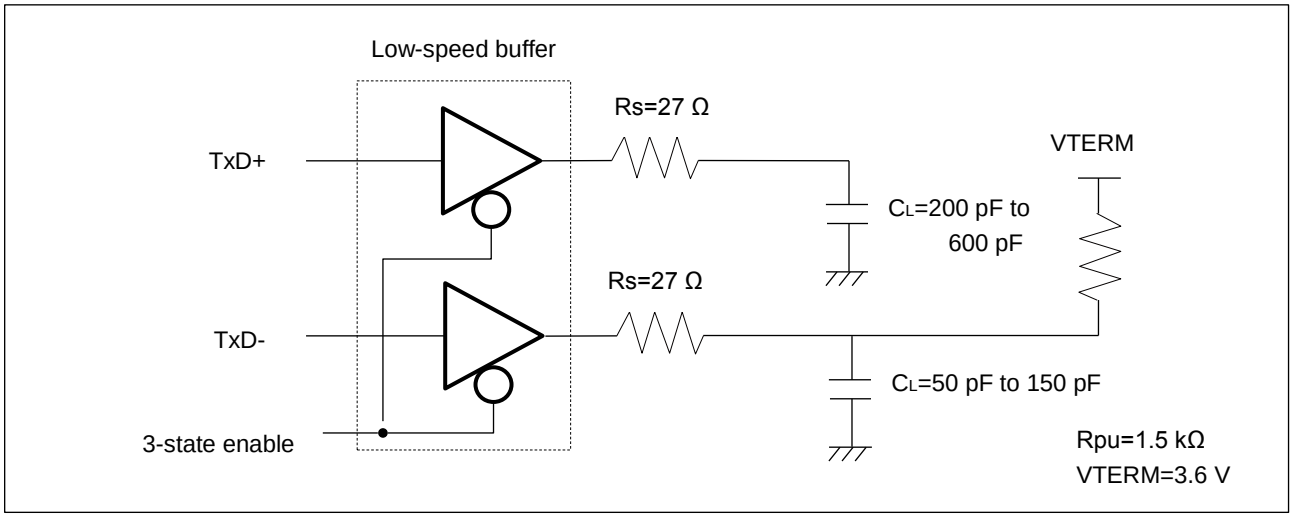


*6 : USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28Ω to 44Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 33 Ω (recommendation value : 27 Ω) series resistor Rs.

- Low-Speed Load (Upstream Port Load) – Reference 1



- Low-Speed Load (Downstream Port Load) – Reference 2



11.7.2 Low-Voltage Detection Interrupt

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH	SVHRLI=00100	1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH	SVHRLI=00101	1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH	SVHRLI=00110	1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH	SVHRLI=00111	1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH	SVHRLI=01000	1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH	SVHRLI=01001	1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH	SVHRLI=01010	1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH	SVHRLI=01011	1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH	SVHRLI=01100	2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH	SVHRLI=01101	2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH	SVHRLI=01110	2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH	SVHRLI=01111	2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH	SVHRLI=10000	2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH	SVHRLI=10001	2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH	SVHRLI=10010	2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH	SVHRLI=10011	3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} represents the APB1 bus clock cycle time.

11.8 Flash Memory Write/Erase Characteristics

(V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

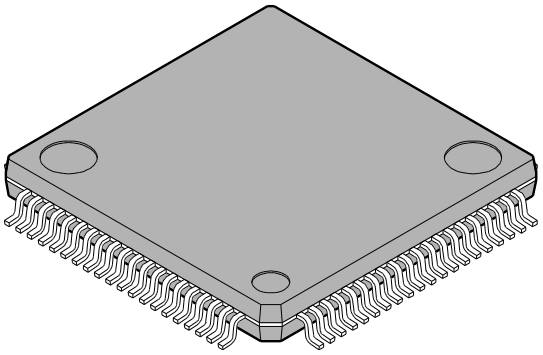
Parameter		Value			Unit	Remarks
		Min	Typ*	Max*		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time (Target Value)

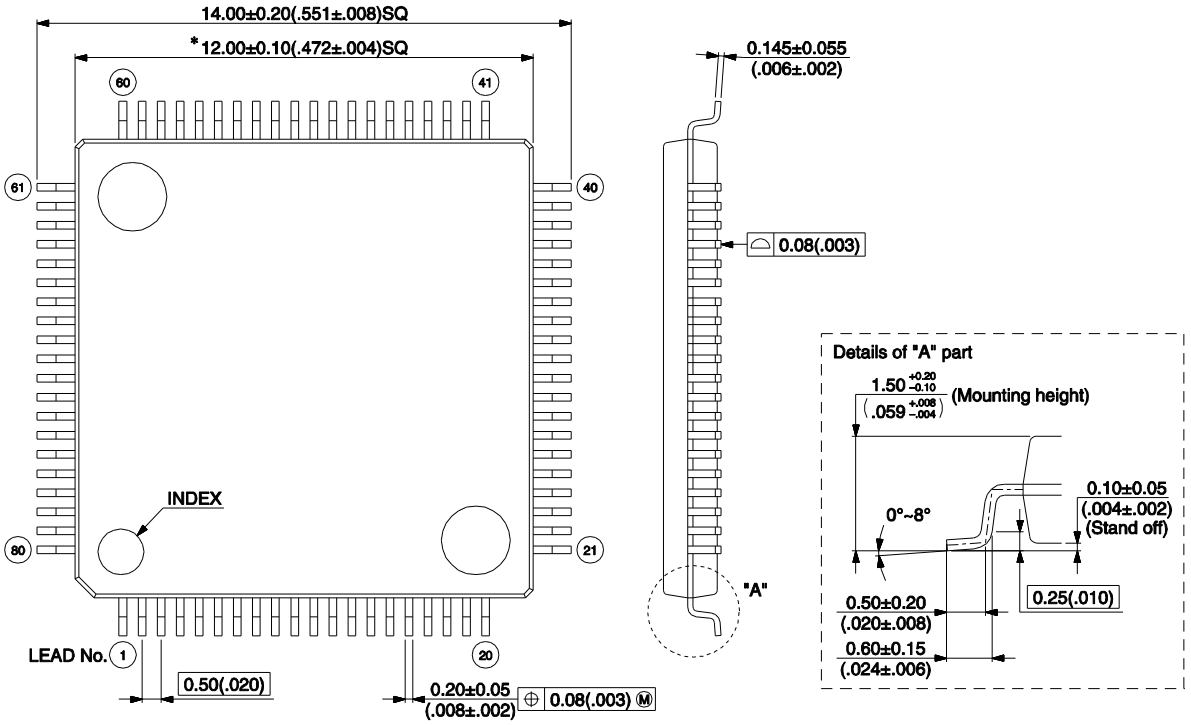
Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12×12-0.50

80-pin plastic LQFP
(FPT-80P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values