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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b84e0agv20000

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 24 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

Smart Card Interface (Max 2 Channels)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

AES Calculator

- AES (Advanced Encryption Standard) calculator is an AES common key crypto accelerator that is compliant with FIPS (Federal Information Processing Standard Publication) 197.
- Available key length: 128/192/256-bit
- CBC mode and ECB mode support

Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock: 4 MHz to 40 MHz
  - Sub clock: 32.768 kHz
  - Built-in high-speed CR clock: 4 MHz
  - Built-in low-speed CR clock: 100 kHz
  - Main PLL clock
- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

Clock Supervisor (CSV)

The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-Voltage Detector (LVD)

This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVDR: monitor Vcc and auto-reset operation
- LVD1: monitor Vcc and error reporting via an interrupt
- LVD2: selectable to monitor Vcc or LVDI and error reporting via an interrupt

Low Power Consumption Mode

This series has six low power consumption modes.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable between keeping the value of RAM and not)
- Deep standby Stop (selectable between keeping the value of RAM and not)

4. List of Pin Functions

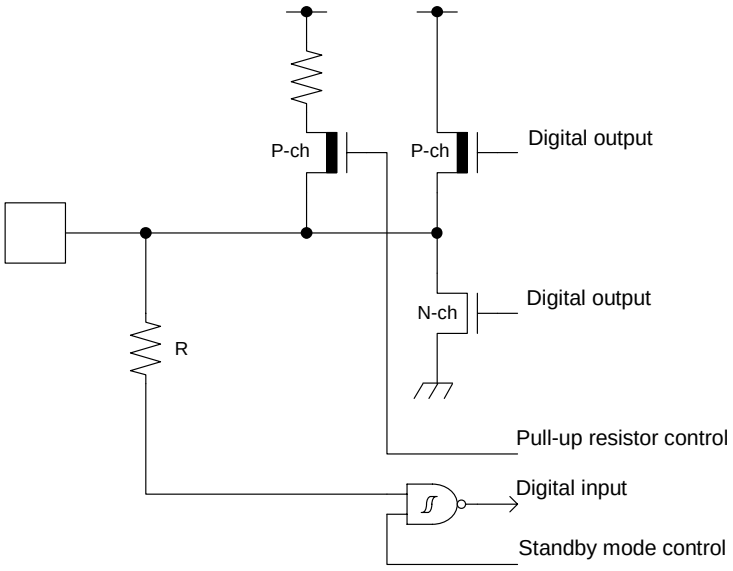
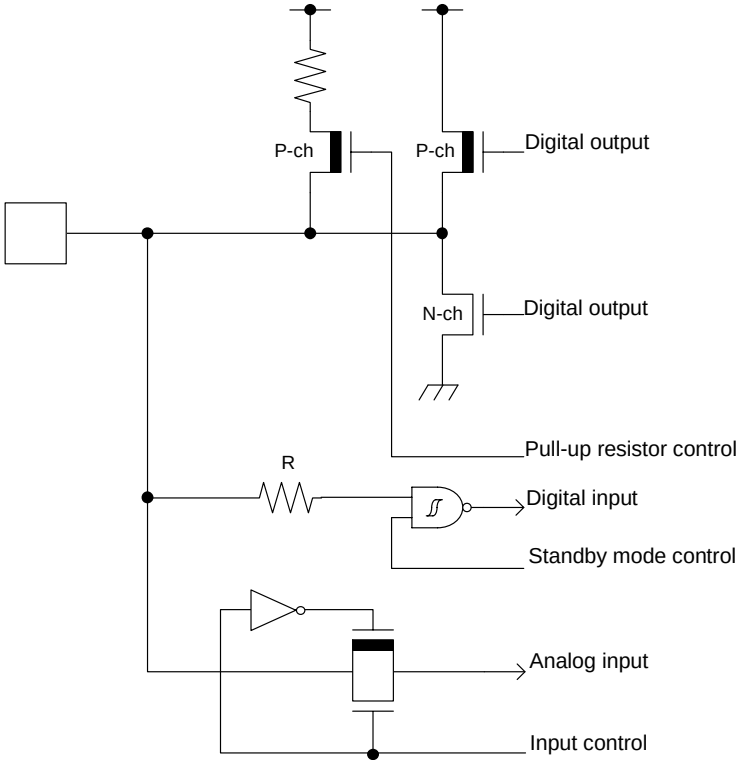
List of Pin Numbers

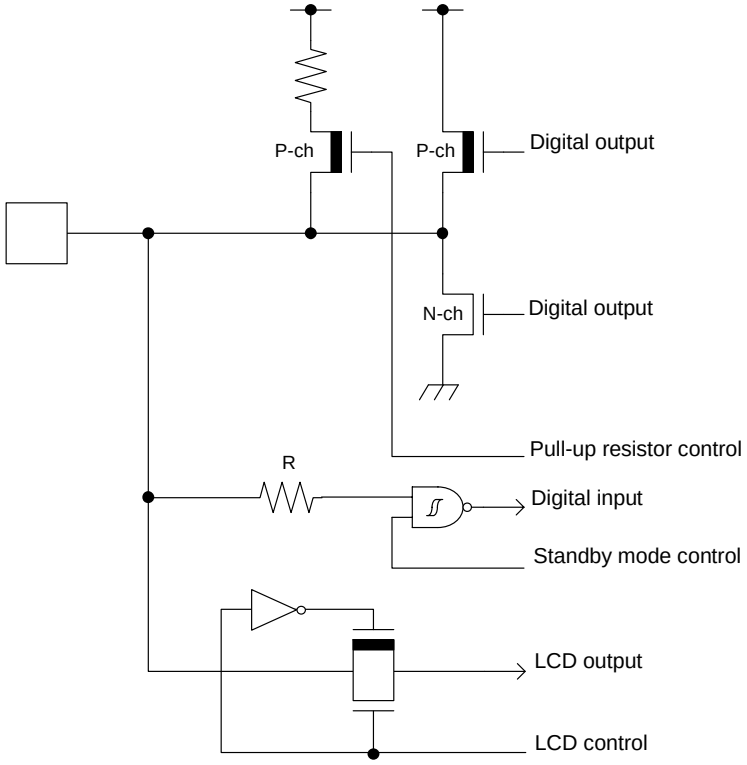
The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

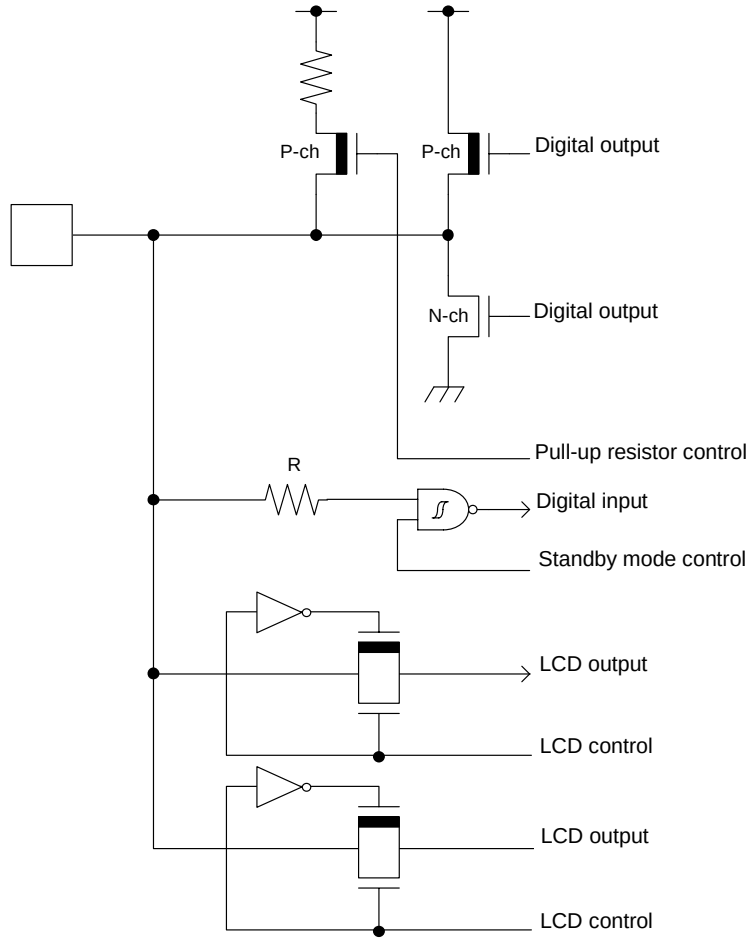
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
1	1	1	VCC	-	
2	2	2	P50	Q	X
			SIN3_1		
			INT00_0		
			VV4		
3	3	3	P51	Q	X
			SOT3_1		
			INT01_0		
			VV3		
4	4	4	P52	Q	X
			SCK3_1		
			INT02_0		
			VV2		
5	5	5	P53	Q	X
			SIN6_0		
			TIOA1_2		
			INT07_2		
			VV1		
6	6	6	P54	Q	X
			SOT6_0		
			TIOB1_2		
			INT18_1		
			VV0		
7	7	7	P55	L	S
			SCK6_0		
			ADTG_1		
			INT19_1		
			SEG39		
8	8	8	P56	L	U
			MI2SMCK6_1		
			CEC1_1		
			INT08_2		
			WKUP9		
			SEG38		
	-	-	SIN1_0		
9	-	-	P57	F	I
			SOT1_0		
10	-	-	P58	F	I
			SCK1_0		
11	-	-	P59	F	J
			SIN7_0		
			INT16_1		

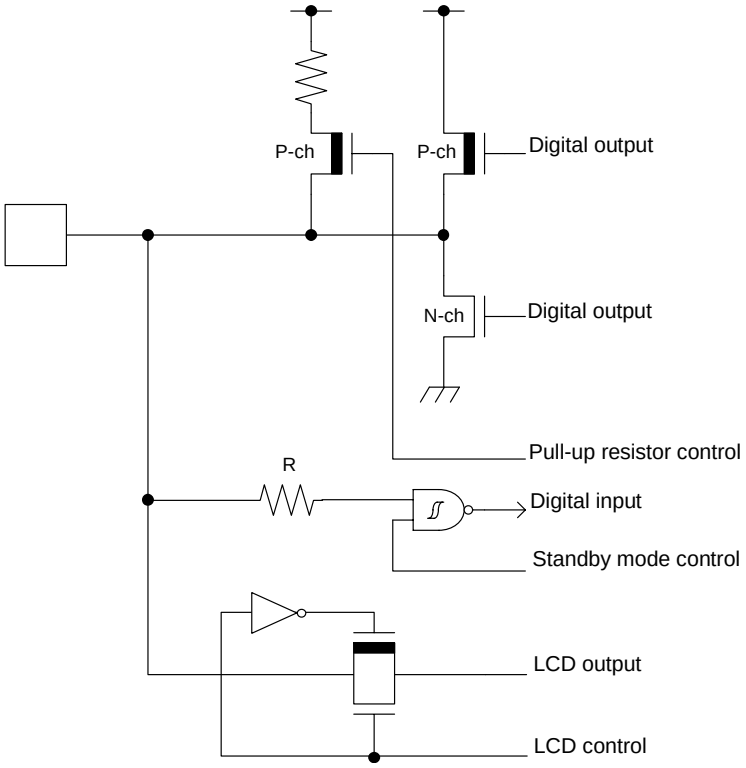
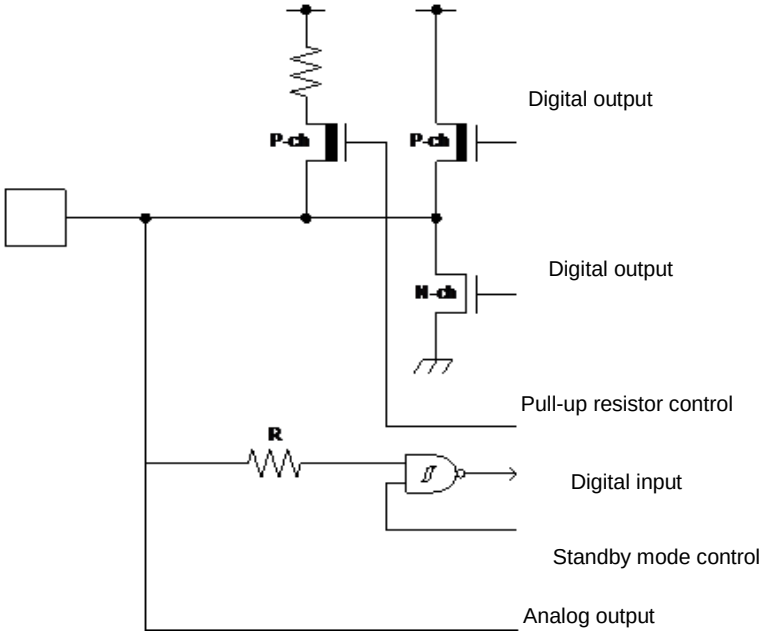
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
76	66	56	P1A SIN4_1 IC01_1 INT05_1 AN10 SEG17	P	V
77	67	57	P1B SOT4_1 IC02_1 INT20_2 AN11 SEG16	P	V
78	68	-	P1C SCK4_1 IC03_1 INT21_2 AN12 SEG15	P	V
79	69	-	P1D CTS4_1 DTTI0X_1 INT22_2 AN13 SEG14	P	V
80	70	-	P1E RTS4_1 FRCK0_1 ADTG_5 INT23_2 AN14	H	L
81	-	-	P28 RTO05_1 TIOB6_2 ADTG_4	F	I
82	-	-	P27 RTO04_1 TIOA6_2 INT02_2 AN15	G	L
83	-	-	P26 SCK2_1 RTO03_1	F	I
84	-	-	P25 SOT2_1 RTO02_1	F	I
85	-	-	P24 SIN2_1 RTO01_1 INT17_1	F	J
86	71	58	P23 SCK0_0 TIOA7_1 RTO00_1 AN16 SEG13	P	K

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	11	-	-
	SIN7_1		48	43	33
	SIN7_2		117	97	77
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I^2C pin (operation mode 4).	12	-	-
	SOT7_1 (SDA7_1)		49	44	34
	SOT7_2 (SDA7_2)		118	98	78
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I^2C pin (operation mode 4).	13	-	-
	SCK7_1 (SCL7_1)		50	45	35
	SCK7_2 (SCL7_2)		119	99	79
	SCS70_1	Multi-function serial interface ch.7 serial chip select 0 input/output pin.	47	42	32
	SCS71_1	Multi-function serial interface ch.7 serial chip select 1 input/output pin.	51	-	-
	SCS72_1	Multi-function serial interface ch.7 serial chip select 2 input/output pin.	52	-	-
Smart Card Interface 0	IC0_VCC_0	Smart card ch.0 power enable output pin	106	91	71
	IC0_VCC_1		33	28	-
	IC0_VPEN_0	Smart card ch.0 programming output pin	105	90	70
	IC0_VPEN_1		34	29	-
	IC0_RST_0	Smart card ch.0 reset output pin	114	94	74
	IC0_RST_1		35	30	-
	IC0_CIN_0	Smart card ch.0 insert detection input pin	102	87	67
	IC0_CIN_1		37	32	22
	IC0_CLK_0	Smart card ch.0 serial interface clock output pin	107	92	72
	IC0_CLK_1		32	27	-
	IC0_DATA_0	Smart card ch.0 serial interface data input/output pin	113	93	73
	IC0_DATA_1		36	31	21
Smart Card Interface 1	IC1_VCC_0	Smart card ch.1 power enable output pin	28	23	18
	IC1_VCC_1		63	53	43
	IC1_VPEN_0	Smart card ch.1 programming output pin	27	22	17
	IC1_VPEN_1		64	54	44
	IC1_RST_0	Smart card ch.1 reset output pin	26	21	16
	IC1_RST_1		65	55	45
	IC1_CIN_0	Smart card ch.1 insert detection input pin	24	19	14
	IC1_CIN_1		67	57	47
	IC1_CLK_0	Smart card ch.1 serial interface clock output pin	29	24	19
	IC1_CLK_1		62	52	42
	IC1_DATA_0	Smart card ch.1 serial interface data input/output pin	25	20	15
	IC1_DATA_1		66	56	46
USB	UDM0	USB device/host D – pin	103	88	68
	UDP0	USB device/host D + pin	104	89	69
	UHCONX0	USB external pull-up control pin	102	87	67

Type	Circuit	Remarks
F		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
G		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
L		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD segment output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
M		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD common output ・LCD segment output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
N		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD common output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}=-4 mA, I_{OL}= 4 mA ・Available to control of PZR registers.
O		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog output ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC
VCC → AVCC → AVRH
Turning off : VCC → VBAT
AVRH → AVCC → VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Handling when Using Debug Pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
H	Serial wire debug selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
J	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than the above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output Maintain previous state / Internal input fixed at 0
	GPIO selected									

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0
	Resource other than the above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
M	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
N	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

11.3 DC Characteristics

11.3.1 Current Rating

Symbol (Pin Name)	Conditions		HCLK Frequency[*4]	Value Typ[*1]	Value Max[*2]	Unit	Remarks
I_{CC} (VCC)	Run mode, code executed from Flash	4 MHz external clock input, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.7	TBD	mA	*3
			8 MHz	1.15	TBD		
			20 MHz	2.25	TBD		
			40 MHz	4.5	TBD		
		4 MHz external clock input, PLL ON[*8] Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4 MHz	0.75	TBD	mA	*3
			8 MHz	1.25	TBD		
			20 MHz	2.5	TBD		
			40 MHz	5.0	TBD		
		4 MHz crystal oscillation, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.8	TBD	mA	*3
			8 MHz	1.4	TBD		
			20 MHz	2.75	TBD		
			40 MHz	5.5	TBD		
	Run mode, code executed from RAM	4 MHz external clock input, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.2	TBD		
			20 MHz	2.4	TBD		
			40 MHz	4.8	TBD		
	Run mode, code executed from Flash	4 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHz	2.6	TBD	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR[*5] NOP code executed All peripheral clock stopped by CKENx	4 MHz	1.2	TBD	mA	*3
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHz	96	TBD	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHz	120	TBD	µA	*3
I_{CCS} (VCC)	Sleep operation	4 MHz external clock input, PLL ON[*8] All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.1	TBD		
			20 MHz	1.9	TBD		
			40 MHz	3.2	TBD		
		Built-in high speed CR[*5] All peripheral clock stopped by CKENx	4 MHz	0.5	TBD	mA	*3
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHz	94	TBD	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHz	105	TBD	µA	*3

*1 : T_A=+25°C,V_{CC}=3.3 V
*2 : T_A=+105°C,V_{CC}=3.6 V
*3 : All ports are fixed
*4 : PCLK0 is set to divided rate 8
*5 : The frequency is set to 4 MHz by trimming
*6 : Flash sync down is set to FRWTR.RWT=11 and FSYNDN.SD=1111
*7 : VCC=1.65 V
*8 : When HCLK=4 MHz, PLL OFF

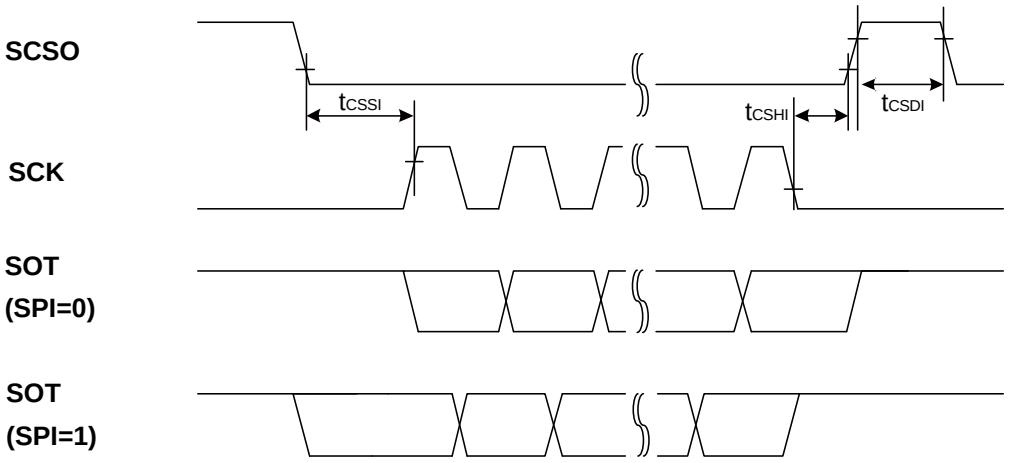
SPI (SPI=1, SCINV=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

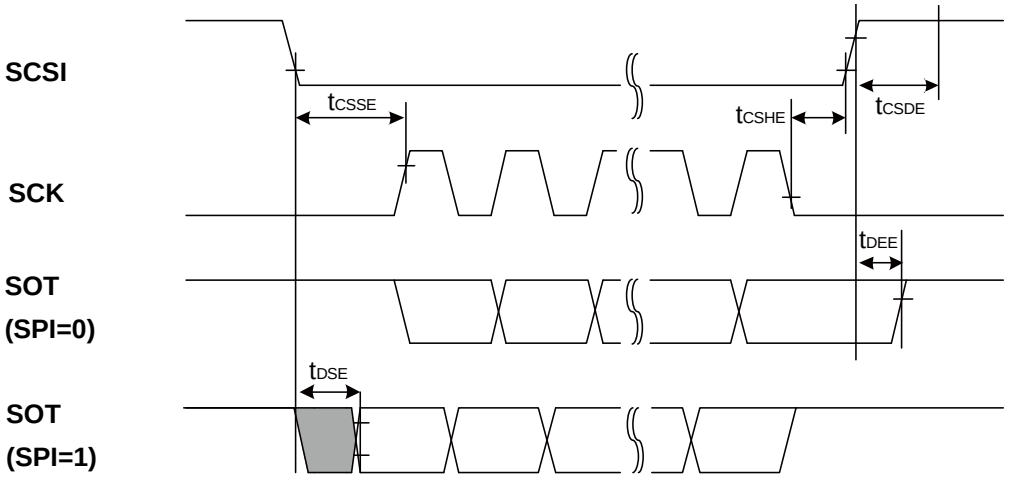
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		60	-	50	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} +10	-	t_{CYCP} +10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

11.5 12-bit A/D Converter

Electrical Characteristics of A/D Converter (Preliminary Values)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time *1	-	-	2.0	-	-	µs	AV_{CC} ≥ 2.7 V
			4.0	-	-		1.8 ≤ AV_{CC} < 2.7 V
			10	-	-		1.65 ≤ AV_{CC} < 1.8 V
Sampling time *2	t_S	-	0.6	-	10	µs	AV_{CC} ≥ 2.7 V
			1.2	-			1.8 ≤ AV_{CC} < 2.7 V
			3.0	-			1.65 ≤ AV_{CC} < 1.8 V
Compare clock cycle *3	t_{CCK}	-	100	-	1000	ns	AV_{CC} ≥ 2.7 V
			200	-			1.8 ≤ AV_{CC} < 2.7 V
			500	-			1.65 ≤ AV_{CC} < 1.8 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistance	R_{AIN}	-	-	-	2.2	kΩ	AV_{CC} ≥ 2.7 V
					5.5		1.8 ≤ AV_{CC} < 2.7 V
					10.5		1.65 ≤ AV_{CC} < 1.8 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	AVCC ≥ 2.7V
			AV_{CC}				AVCC < 2.7V

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The minimum conversion time is computed according to the following conditions:
AV_{CC} ≥ 2.7 V sampling time=0.6 µs, compare time=1.4 µs
1.8 ≤ AV_{CC} < 2.7 V sampling time=1.2 µs, compare time=2.8 µs
1.65 ≤ AV_{CC} < 1.8 V sampling time=3.0 µs, compare time=7.0 µs
Ensure that the conversion time satisfies the specifications of the sampling time (t_S) and compare clock cycle (t_{CCK}).
For details of the settings of the sampling time and compare clock cycle, refer to "Chapter: A/D Converter" in "FM0+ Family Peripheral Manual Analog Macro Part".
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see "8. Block Diagram".
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: The required sampling time varies according to the external impedance.
Set a sampling time that satisfies (Equation 1).

*3: The compare time (t_C) is the result of (Equation 2).

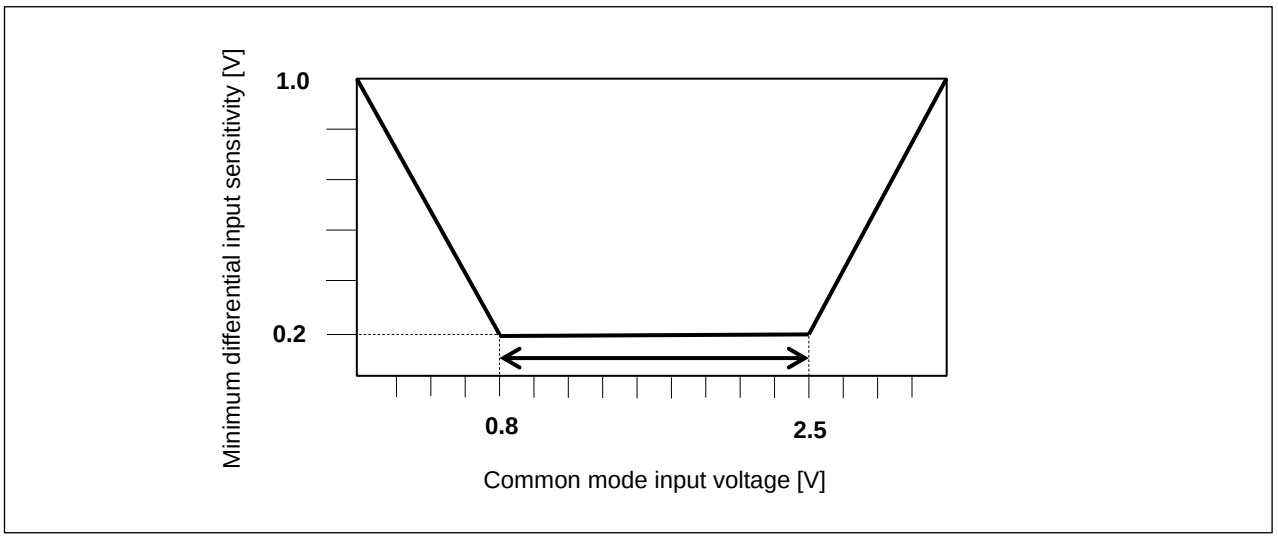
11.6 USB Characteristics

(V_{CC}=3.0 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

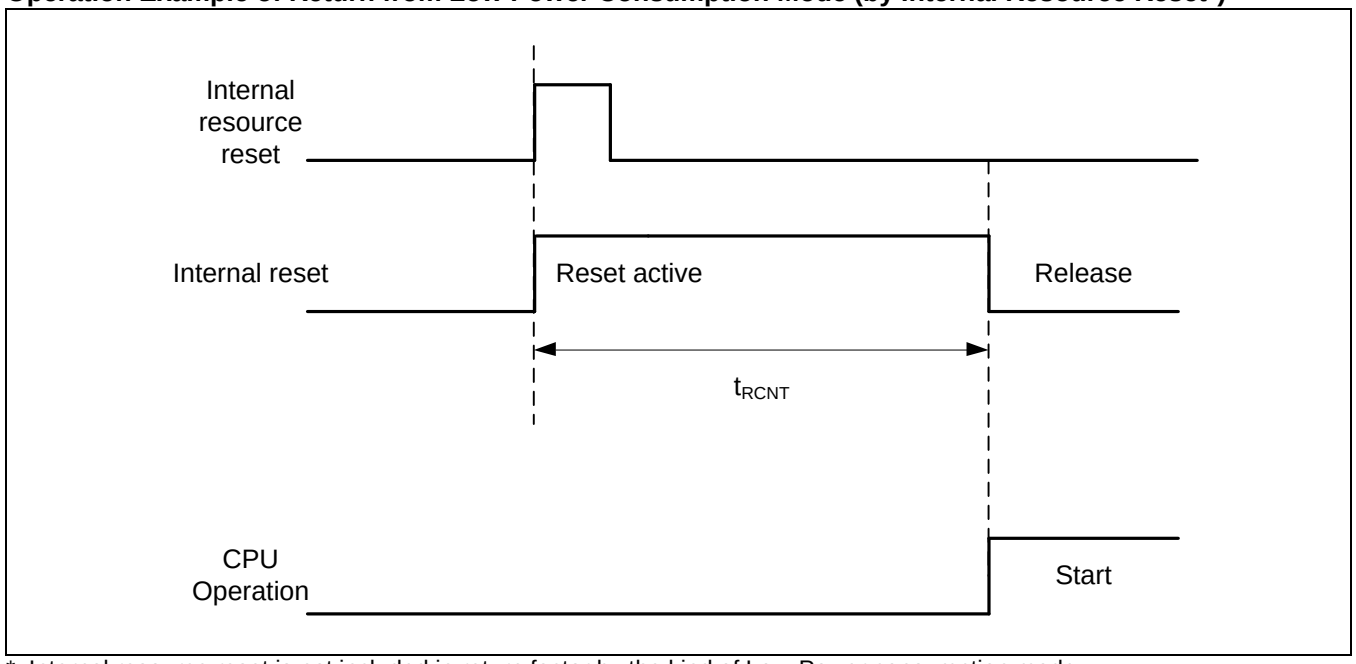
Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	V_{CC} + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} – 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Differential common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristic	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-speed	4	20	ns	*5
	Falling time	t_{FF}		Full-speed	4	20	ns	*5
	Rising/Falling time matching	t_{FRFM}		Full-speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-speed	75	300	ns	*7
	Falling time	t_{LF}		Low-speed	75	300	ns	*7
	Rising/Falling time matching	t_{LRFM}		Low-speed	80	125	%	*7

*1 : The switching threshold voltage of single-end-receiver of USB I/O buffer is set as within V_{IL}(Max)=0.8 V, VIH(Min)=2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2 : Use differential-receiver to receive USB differential data signal.
Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.



Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4889752	TEKA	08/31/2015	New Spec.