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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b84ehagv20000

1. Product Lineup

Memory Size

Product Name		S6E1B84E/F/G	S6E1B86E/F/G
On-chip Flash memory	Upper Bank	256 Kbytes	512 Kbytes
	Lower Bank	48 Kbytes	48 Kbytes
On-chip SRAM		32 Kbytes	64 Kbytes

Function

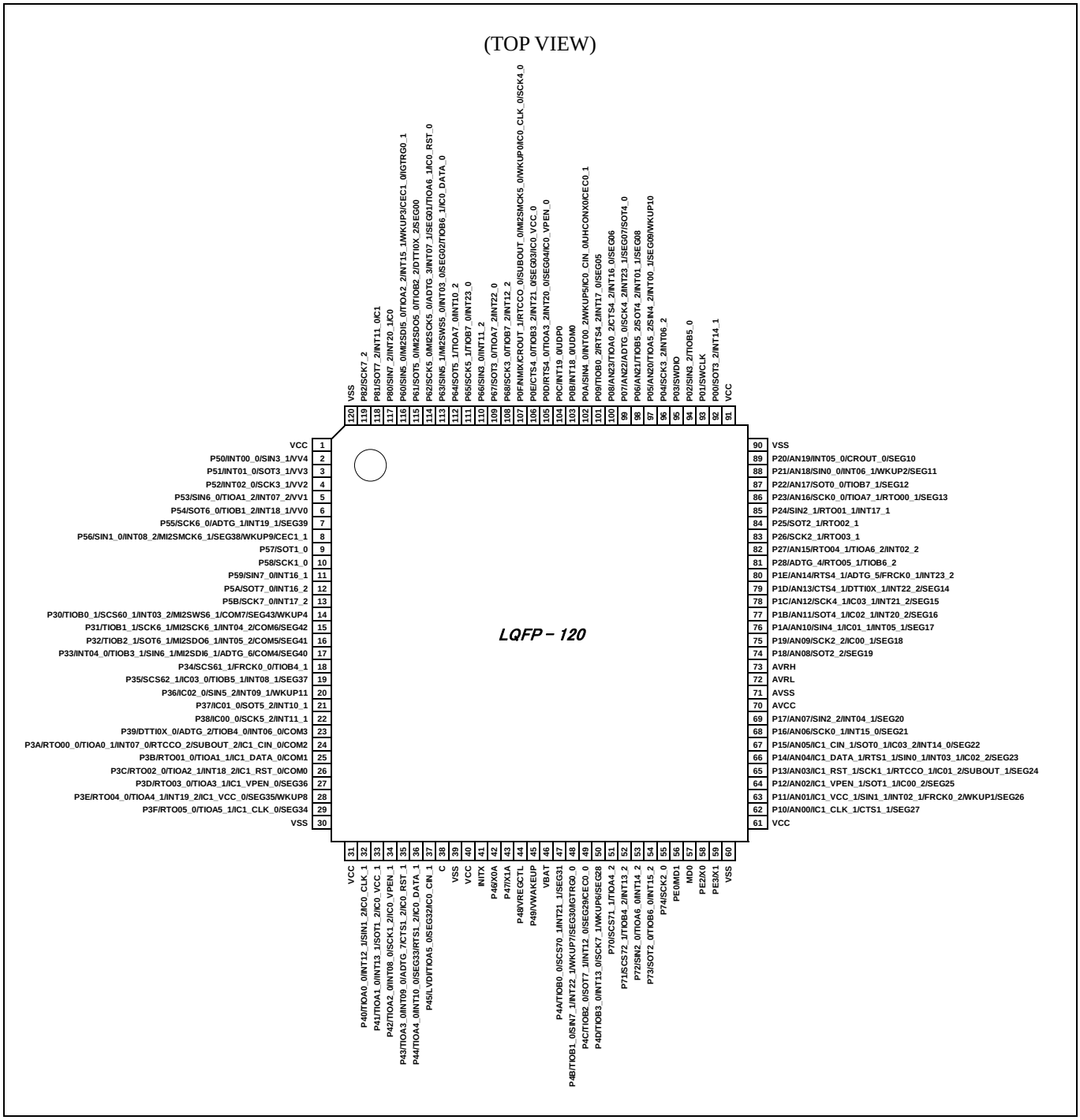
Product Name			S6E1B84E0A S6E1B86E0A S6E1B84EHA S6E1B86EHA	S6E1B84F0A S6E1B86F0A S6E1B84FHA S6E1B86FHA	S6E1B84G0A S6E1B86G0A S6E1B84GHA S6E1B86GHA
Pin count			80	100	120
CPU			Cortex-M0+		
	Frequency		40.8 MHz		
Power supply voltage range			1.65 V to 3.6 V		
USB 2.0 (Device/Host)			1 unit		
DSTC			64ch		
Multi-function Serial Interface (UART/CSIO (SPI)/I^{2}C/I^{2}S)			8ch (Max) with 128 bytes FIFO I^{2}S: ch.5, ch.6		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch (Max)		
LCD controller			20SEG x 8COM(Max) / 24SEG x 4COM(Max)	32SEG x 8COM(Max) / 36SEG x 4COM(Max)	40SEG x 8COM(Max) / 44SEG x 4COM(Max)
Multi-function Timer	A/D activation compare	6ch	1 unit		
	Input capture	4ch			
	Free-run timer	3ch			
	Output compare	6ch			
	Waveform generator	3ch			
	PPG	3ch			
Dual Timer			1 unit		
HDMI-CEC/ Remote Control Receiver			2ch (max)		
Smart Card Interface			2ch (max)		
Real-time Clock			1 unit (with battery power)		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1ch (SW) + 1ch (HW)		
External Interrupt			24 pins (Max), NMI × 1		
I/O port			65 pins (Max)	82 pins (Max)	102 pins (Max)
12-bit A/D converter			16ch (1 unit)	23ch (1 unit)	24ch (1 unit)
CSV (Clock Supervisor)			Yes		
LVD (Low-voltage Detection)			2ch		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SW-DP		
Unique ID			Yes		
AES Calculator			-	Yes*1	-	Yes*1	-	Yes*1

*1: AES Calculator is built in following products.
S6E1B86GHA, S6E1B84GHA, S6E1B86FHA, S6E1B84FHA, S6E1B86EHA, S6E1B84EHA

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
  See "11 Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

FPT-120P-M21



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

4. List of Pin Functions

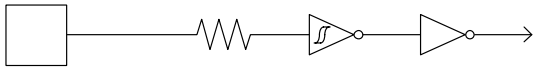
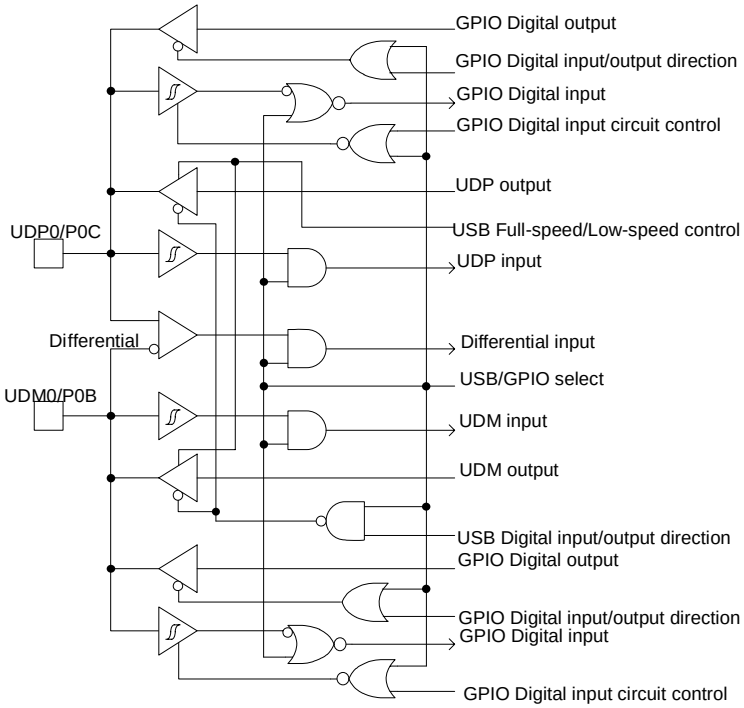
List of Pin Numbers

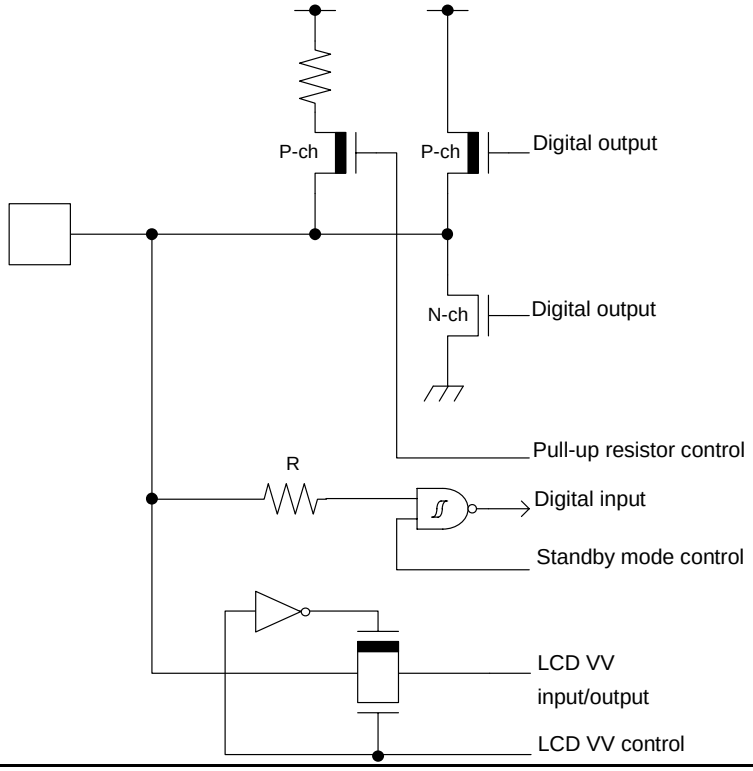
The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
1	1	1	VCC	-	
2	2	2	P50	Q	X
			SIN3_1		
			INT00_0		
			VV4		
3	3	3	P51	Q	X
			SOT3_1		
			INT01_0		
			VV3		
4	4	4	P52	Q	X
			SCK3_1		
			INT02_0		
			VV2		
5	5	5	P53	Q	X
			SIN6_0		
			TIOA1_2		
			INT07_2		
			VV1		
6	6	6	P54	Q	X
			SOT6_0		
			TIOB1_2		
			INT18_1		
			VV0		
7	7	7	P55	L	S
			SCK6_0		
			ADTG_1		
			INT19_1		
			SEG39		
8	8	8	P56	L	U
			MI2SMCK6_1		
			CEC1_1		
			INT08_2		
			WKUP9		
			SEG38		
	-	-	SIN1_0		
9	-	-	P57	F	I
			SOT1_0		
10	-	-	P58	F	I
			SCK1_0		
11	-	-	P59	F	J
			SIN7_0		
			INT16_1		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
49	44	34	P4C TIOB2_0 SOT7_1 CEC0_0 INT12_0 SEG29	L	R
50	45	35	P4D TIOB3_0 SCK7_1 INT13_0 WKUP6 SEG28	L	T
51	-	-	P70 TIOA4_2 SCS71_1	F	I
52	-	-	P71 TIOB4_2 SCS72_1 INT13_2	F	J
53	-	-	P72 SIN2_0 TIOA6_0 INT14_2	F	J
54	-	-	P73 SOT2_0 TIOB6_0 INT15_2	F	J
55	-	-	P74 SCK2_0	F	I
56	46	36	PE0 MD1	C	D
57	47	37	MD0	J	M
58	48	38	PE2 X0	A	A
59	49	39	PE3 X1	A	B
60	50	40	VSS	-	-
61	51	41	VCC	-	-
62	52	42	P10 IC1_CLK_1 CTS1_1 AN00 SEG27	P	K
63	53	43	P11 IC1_VCC_1 SIN1_1 FRCK0_2 INT02_1 WKUP1 AN01 SEG26	P	W

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
64	54	44	P12 IC1_VPEN_1 SOT1_1 IC00_2 AN02 SEG25	P	K
65	55	45	P13 IC1_RST_1 SCK1_1 RTCCO_1 IC01_2 SUBOUT_1 AN03 SEG24	P	K
66	56	46	P14 IC1_DATA_1 RTS1_1 SIN0_1 IC02_2 INT03_1 AN04 SEG23	P	V
67	57	47	P15 IC1_CIN_1 SOT0_1 IC03_2 INT14_0 AN05 SEG22	P	V
68	58	48	P16 SCK0_1 INT15_0 AN06 SEG21	P	V
69	59	49	P17 SIN2_2 INT04_1 AN07 SEG20	P	V
70	60	50	AVCC	-	-
71	61	51	AVSS	-	-
72	62	52	AVRL	-	-
73	63	53	AVRH	-	-
74	64	54	P18 SOT2_2 AN08 SEG19	P	K
75	65	55	P19 SCK2_2 IC00_1 AN09 SEG18	P	K

Type	Circuit	Remarks
J		・CMOS level hysteresis input
K		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. ・Full-speed, Low-speed control When the GPIO is selected. ・CMOS level output ・CMOS level hysteresis input ・With standby mode control

Type	Circuit	Remarks
Q		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD VV input/output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

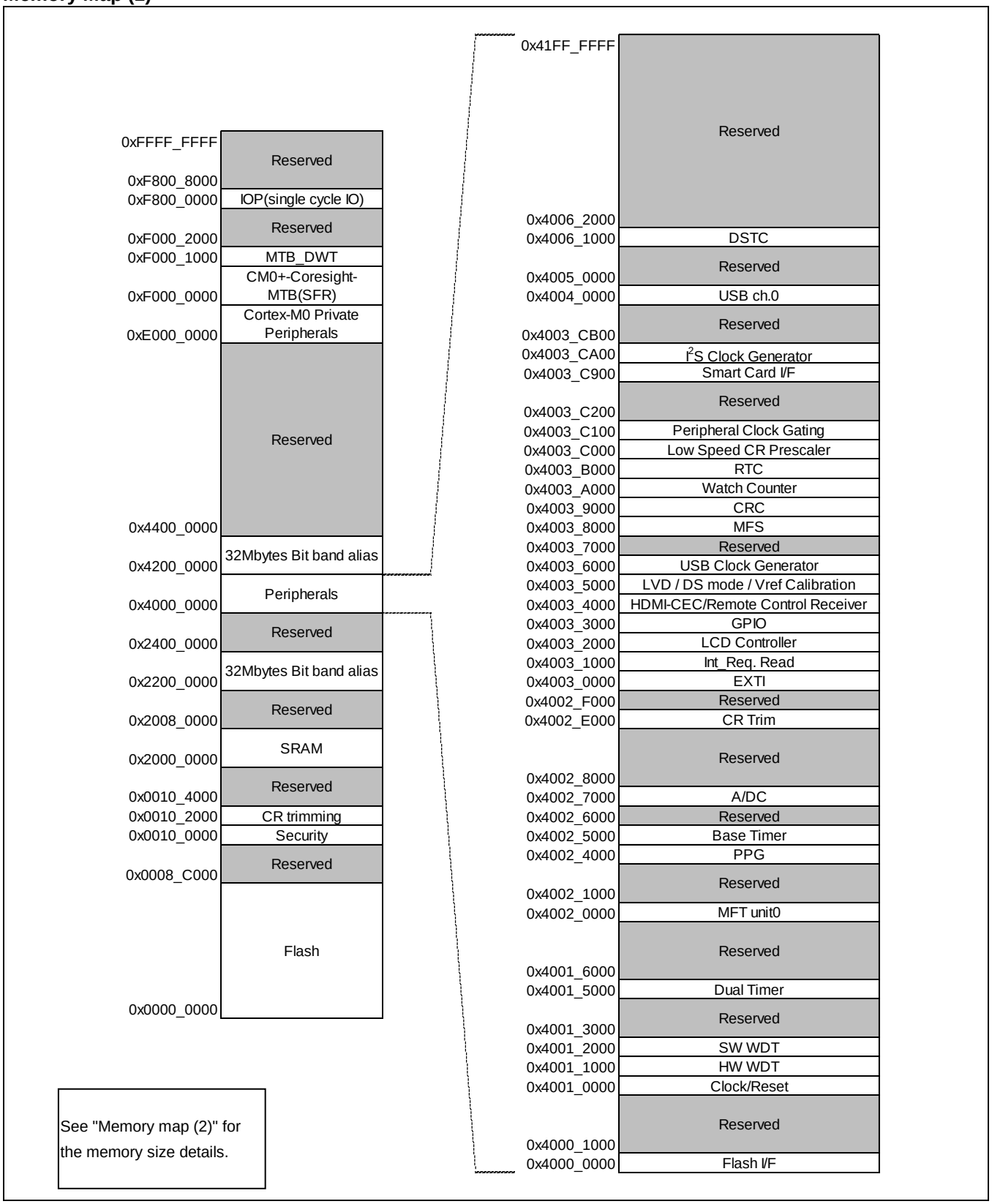
(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

9. Memory Map

Memory Map (1)



10. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the "L" level.

- INITX=1

  This is the period when the INITX pin is the "H" level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at "0"

  This is the status that the input function cannot be used. Internal input is fixed at "L".

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state in which a pin was immediately prior to entering the current mode.

  If a built-in peripheral function is operating, the output follows the peripheral function.

  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

11.3 DC Characteristics

11.3.1 Current Rating

Symbol (Pin Name)	Conditions		HCLK Frequency[*4]	Value Typ[*1]	Value Max[*2]	Unit	Remarks
I_{CC} (VCC)	Run mode, code executed from Flash	4 MHz external clock input, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.7	TBD	mA	*3
			8 MHz	1.15	TBD		
			20 MHz	2.25	TBD		
			40 MHz	4.5	TBD		
		4 MHz external clock input, PLL ON[*8] Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4 MHz	0.75	TBD	mA	*3
			8 MHz	1.25	TBD		
			20 MHz	2.5	TBD		
			40 MHz	5.0	TBD		
		4 MHz crystal oscillation, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.8	TBD	mA	*3
			8 MHz	1.4	TBD		
			20 MHz	2.75	TBD		
			40 MHz	5.5	TBD		
	Run mode, code executed from RAM	4 MHz external clock input, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.2	TBD		
			20 MHz	2.4	TBD		
			40 MHz	4.8	TBD		
	Run mode, code executed from Flash	4 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHz	2.6	TBD	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR[*5] NOP code executed All peripheral clock stopped by CKENx	4 MHz	1.2	TBD	mA	*3
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHz	96	TBD	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHz	120	TBD	µA	*3
I_{CCS} (VCC)	Sleep operation	4 MHz external clock input, PLL ON[*8] All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.1	TBD		
			20 MHz	1.9	TBD		
			40 MHz	3.2	TBD		
		Built-in high speed CR[*5] All peripheral clock stopped by CKENx	4 MHz	0.5	TBD	mA	*3
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHz	94	TBD	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHz	105	TBD	µA	*3

*1 : T_A=+25°C,V_{CC}=3.3 V
*2 : T_A=+105°C,V_{CC}=3.6 V
*3 : All ports are fixed
*4 : PCLK0 is set to divided rate 8
*5 : The frequency is set to 4 MHz by trimming
*6 : Flash sync down is set to FRWTR.RWT=11 and FSYNDN.SD=1111
*7 : VCC=1.65 V
*8 : When HCLK=4 MHz, PLL OFF

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I_{CCHD} (VCC)	Deep standby Stop mode	RAM off	T_A=25°C V_{CC}=3.3 V	0.75	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	0.7	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
			RAM on	T_A=25°C V_{CC}=3.3 V	1.1	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.0	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
	I_{CCRD} (VCC)	Deep standby RTC mode	RAM off	T_A=25°C V_{CC}=3.3 V	1.7	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.6	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
			RAM on	T_A=25°C V_{CC}=3.3 V	1.9	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.7	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1

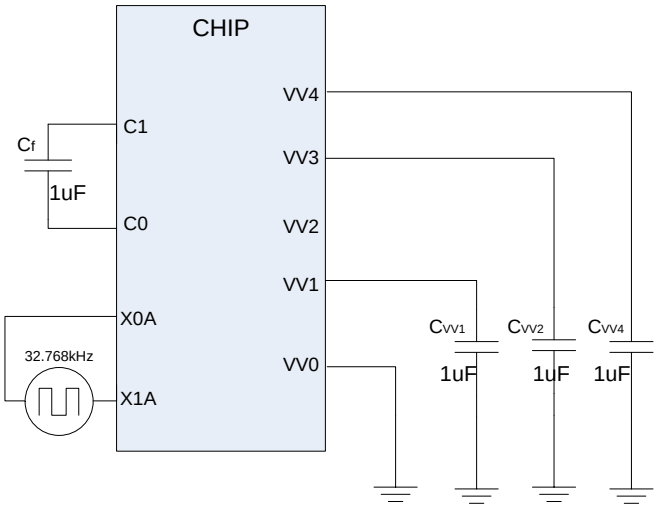
*1: All ports are fixed. LVD off.

11.3.3 LCD Characteristic

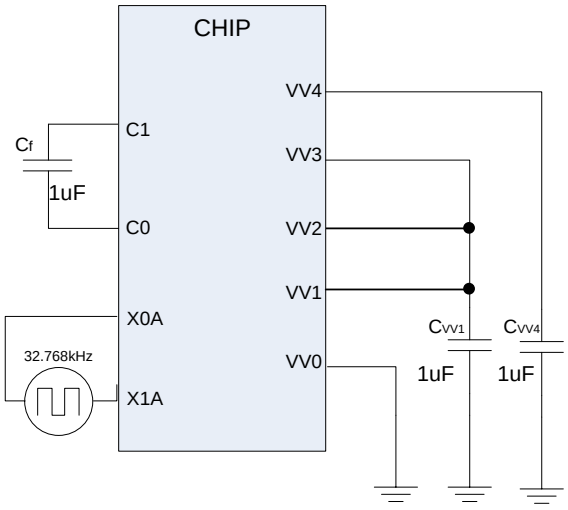
11.3.3.1 LCD Characteristic Without Booster

(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
VV0 to VV3 output voltage (1/4 bias)	V_{VV0}	VV0	When using internal dividing register	0	-	V_{VV4} x 5%	V	
	V_{VV1}	VV1		V_{VV4} x 1/4 -10%	-	V_{VV4} x 1/4 +10%		
	V_{VV2}	VV2		V_{VV4} x 1/2 -10%	-	V_{VV4} x 1/2 + 10%		
	V_{VV3}	VV3		V_{VV4} x 3/4 -10%	-	V_{VV4} x 3/4 + 10%		
VV0 to VV3 output voltage (1/3 bias)	V_{VV0}	VV0	When using internal dividing register	0	-	V_{VV4} x 5%	V	
	V_{VV1}	VV1		V_{VV4} x 1/3 -10%	-	V_{VV4} x 1/3 + 10%		
	V_{VV2}	VV2		V_{VV4} x 2/3 -10%	-	V_{VV4} x 2/3 + 10%		
	V_{VV3}	VV3		V_{VV4} x 2/3 -10%	-	V_{VV4} x 2/3 + 10%		
VV0 to VV3 output voltage (1/2 bias)	V_{VV0}	VV0	When using internal dividing register	0	-	V_{VV4} x 5%	V	
	V_{VV1}	VV1		V_{VV4} x 1/2 -10%	-	V_{VV4} x 1/2 + 10%		
	V_{VV2}	VV2		V_{VV4} x 1/2 -10%	-	V_{VV4} x 1/2 + 10%		
	V_{VV3}	VV3		V_{VV4} x 1/2 -10%	-	V_{VV4} x 1/2 + 10%		
VV4 Active current (1/4 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing resistor	-	10	TBD	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing resistor	-	100	TBD	µA	
VV4 Active current (1/3 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing resistor	-	12	TBD	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing resistor	-	120	TBD	µA	
VV4 Active current (1/2 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing resistor	-	18	TBD	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing resistor	-	180	TBD	µA	
VV4 static current	I_{OFF_VV4}	VV4	When LCD stops	-	0.5	TBD	µA	
VV0 output voltage in using external resistor	V_{VV0E}	VV0	I_{OL}=1 mA	-	-	0.66	V	



LCD Booster 1/3 mode （BIAS[1:0]=2'b01)



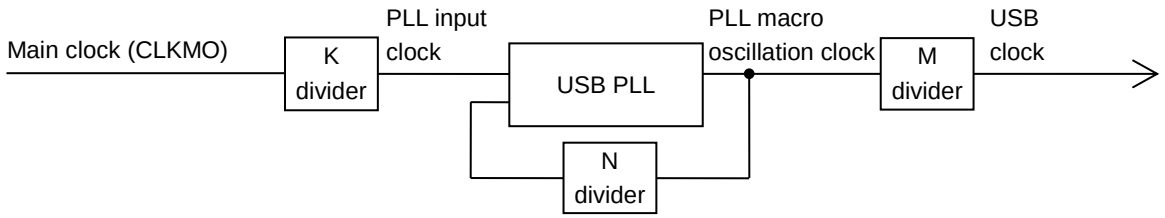
LCD Booster 1/2 mode （BIAS[1:0]=2'b00)

DC Electrical Specifications of Internal reference output voltage setting

(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks
			TRC[1:0] *1	TRF[3:0] *1	Min	Typ	Max		
Internal reference output voltage setting	VV1A	VV1	00	1010	0.89	1.00	1.11	V	BIAS[1:0]=10 *4 Other BIAS[1:0]setting is inhibited
			00	1011	0.94	1.05	1.16		
			00	1100	0.99	1.10	1.21		
			00	1101	1.03	1.15	1.27		
			00	1110	1.07	1.20	1.38		
			01	0111	1.11	1.25	1.38	V	BIAS[1:0]=01 *3 Other BIAS[1:0]setting is inhibited
			01	1000	1.16	1.30	1.44		
			01	1001	1.20	1.35	1.49		
			01	1010	1.25	1.40	1.55		
			01	1011	1.30	1.45	1.60		
			01	1100	1.34	1.50	1.65		
			01	1101	1.39	1.55	1.71		
			01	1110	1.44	1.60	1.76		
			10	0101	1.46	1.65	1.83		
			10	1100	1.79	2.00	2.21	V	BIAS[1:0]=00 *2 Other BIAS[1:0]setting is inhibited
			10	1101	1.84	2.05	2.26		
			10	1110	1.89	2.10	2.32		
			11	0010	1.85	2.15	2.39		
			11	0011	1.90	2.20	2.44		

USB PLL connection



11.4.6 Reset Input Characteristics

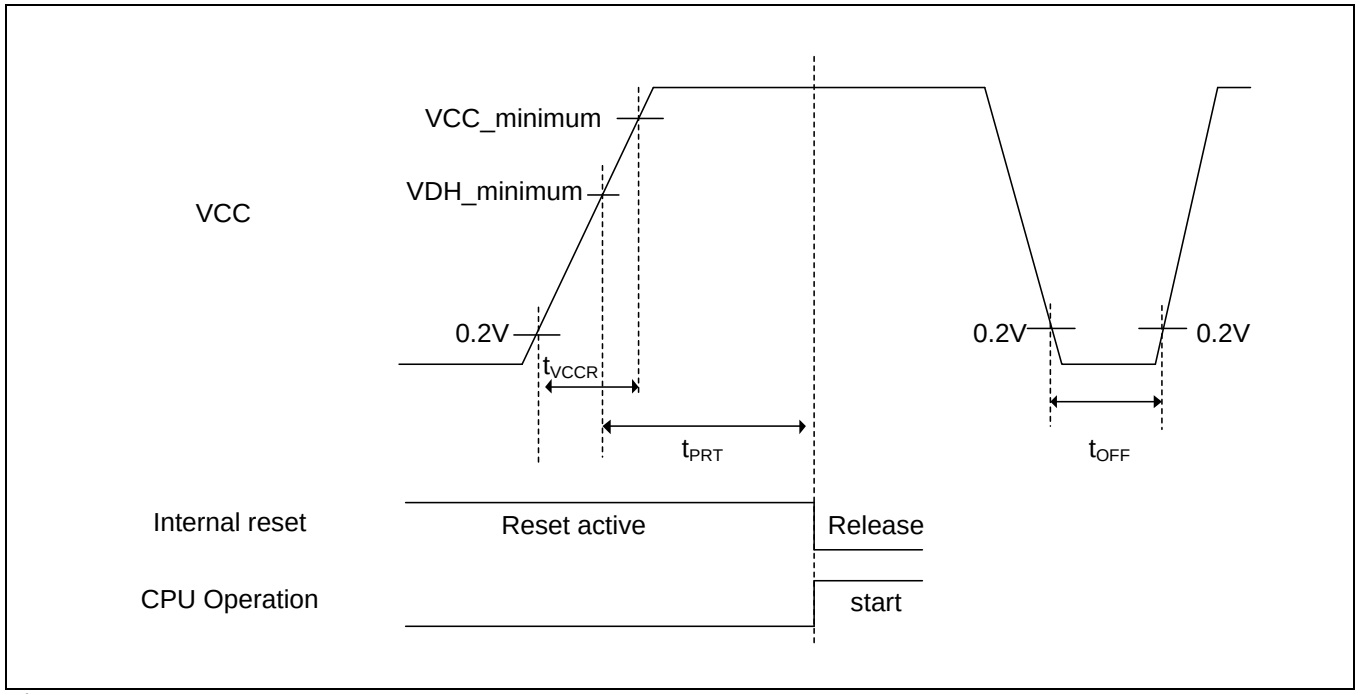
(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

11.4.7 Power-on Reset Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		0.43	3.4	ms	

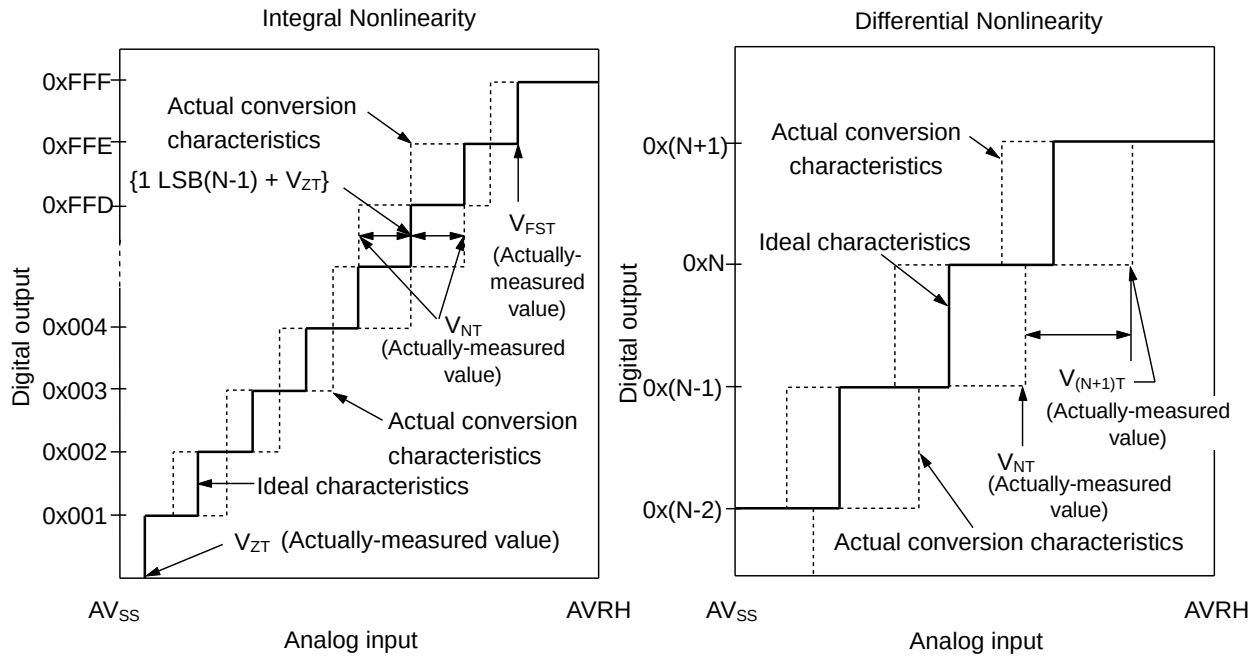


Glossary

- VCC_minimum : Minimum V_{CC} of recommended operating conditions.
- VDH_minimum : Minimum detection voltage of Low-Voltage detection reset.
  See "11.7 Low-Voltage Detection Characteristics".

Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



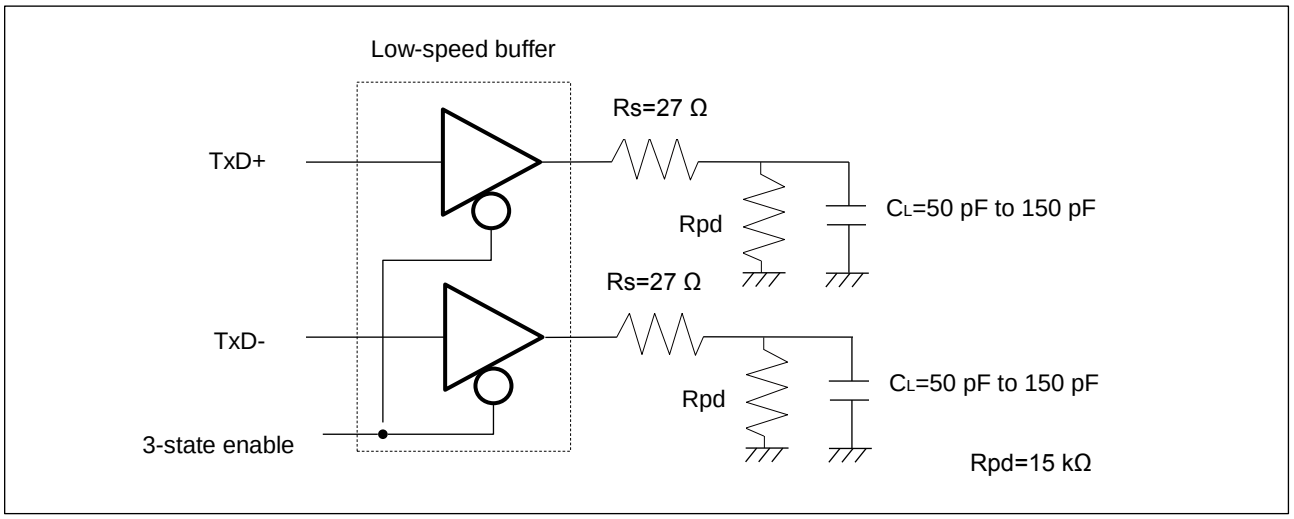
$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

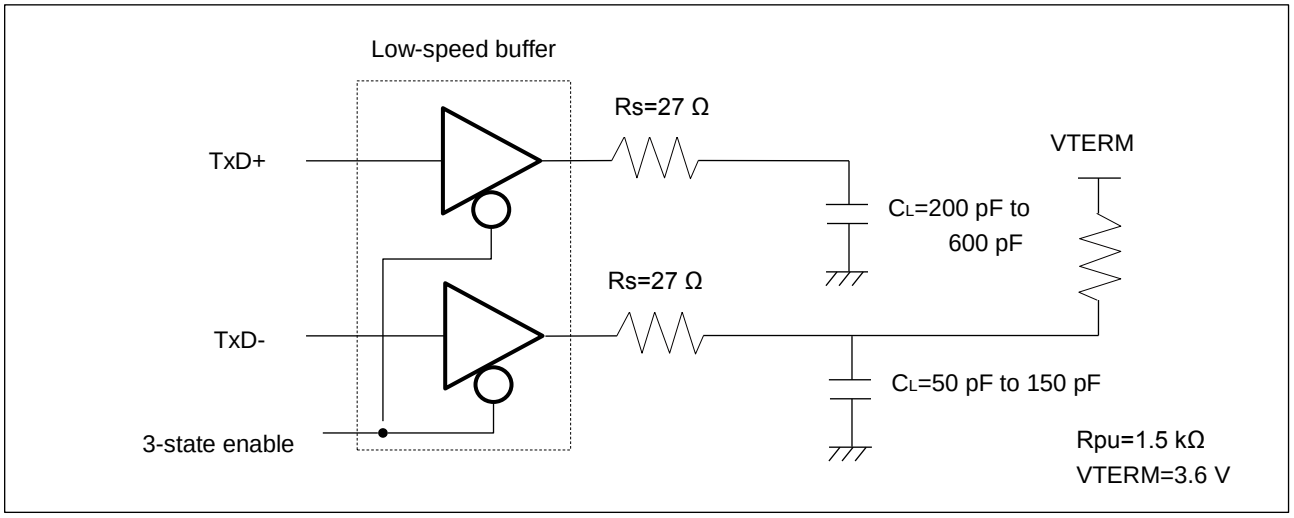
$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

- Low-Speed Load (Upstream Port Load) – Reference 1



- Low-Speed Load (Downstream Port Load) – Reference 2



11.8 Flash Memory Write/Erase Characteristics

(V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ*	Max*		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

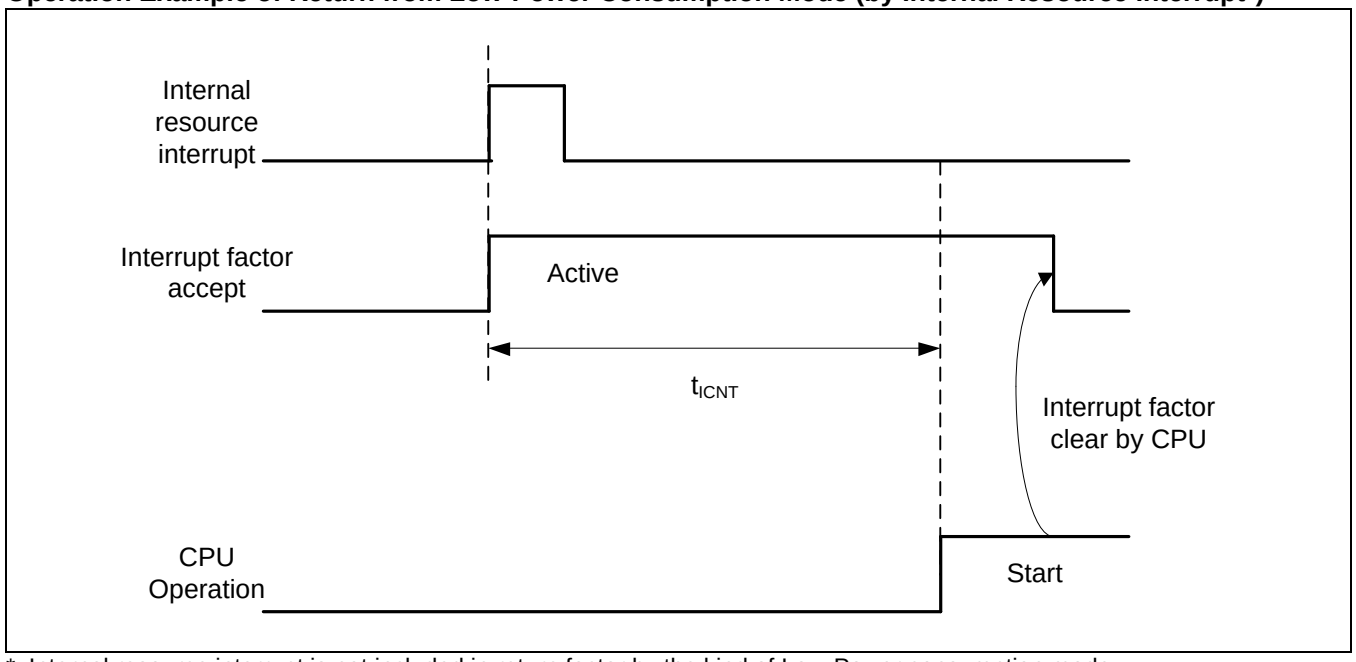
*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time (Target Value)

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*

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**	4889752	TEKA	08/31/2015	New Spec.