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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 23x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b84f0agv20000

- I^2C
  - Standard-mode (Max: 100 kbps) supported / Fast-mode (Max 400 kbps) supported.
- I^2S
  - Using CSIO (ch.5, ch.6) and I^2S clock generator
  - Supports two transfer protocol
    - I^2S
    - MSB-justified
  - Master mode only

Descriptor System Data Transfer Controller (DSTC) (64 Channels)

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor
- system and, following the specified contents of the Descriptor that has already been constructed on the
- memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

A/D Converter (Max: 24 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 µs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 102 fast general-purpose I/O ports @120-pin package
- Certain ports are 5 V tolerant.
  See 4. List of Pin Functions and 5. I/O Circuit Type for the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Multi-Function Timer

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC with Vbat)

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

2. Packages

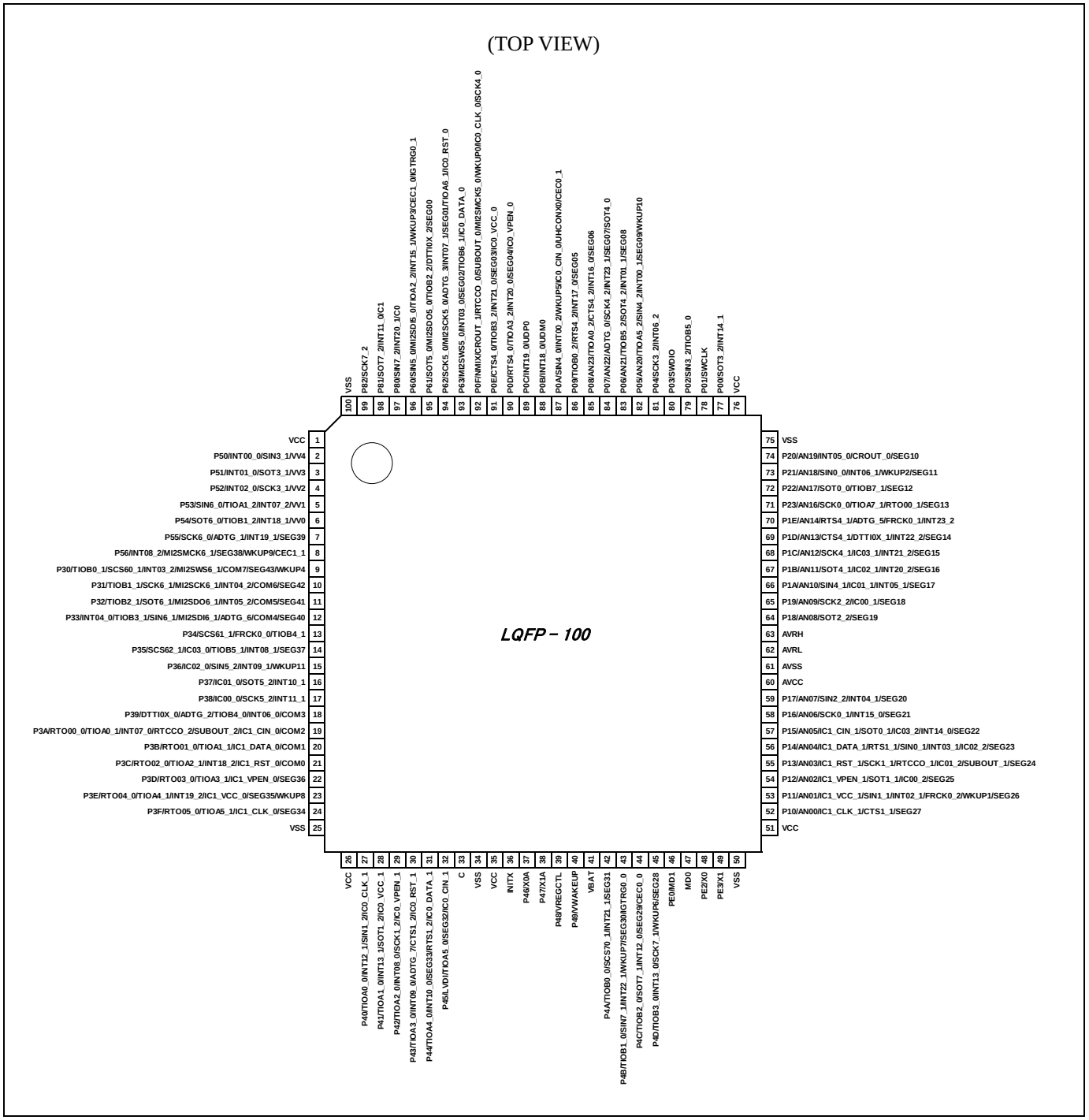
Product Name / Package	S6E1B84E/S6E1B86E	S6E1B84F/S6E1B86F	S6E1B84G/S6E1B86G
LQFP: FPT-80P-M21 (0.50 mm pitch)	❍	-	-
LQFP: FPT-100P-M20 (0.50 mm pitch)	-	❍	-
LQFP: FPT-120P-M21 (0.50 mm pitch)	-	-	❍

❍: Available

Note:

- *See "13. Package Dimensions" for detailed information on each package.*

FPT-100P-M20



Note:

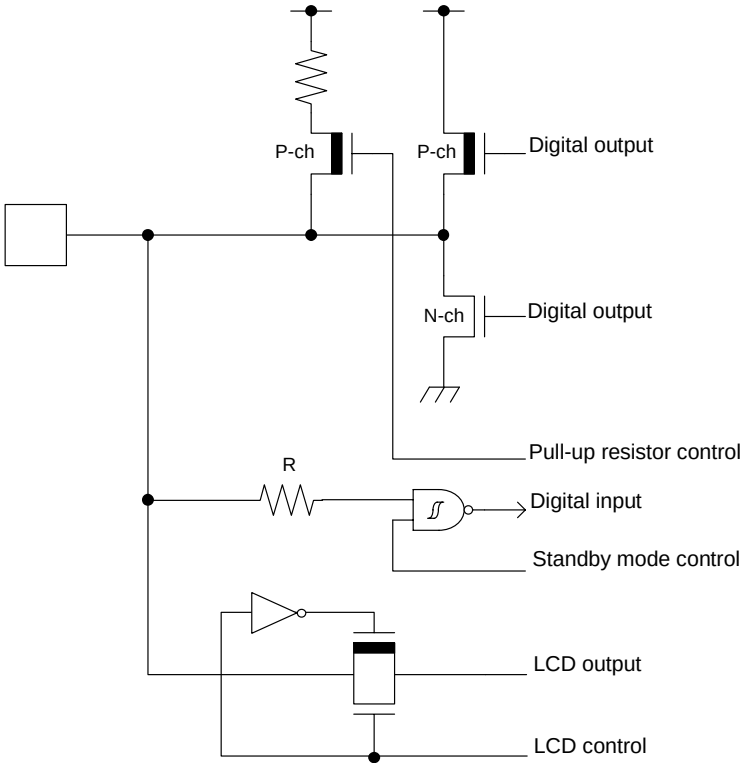
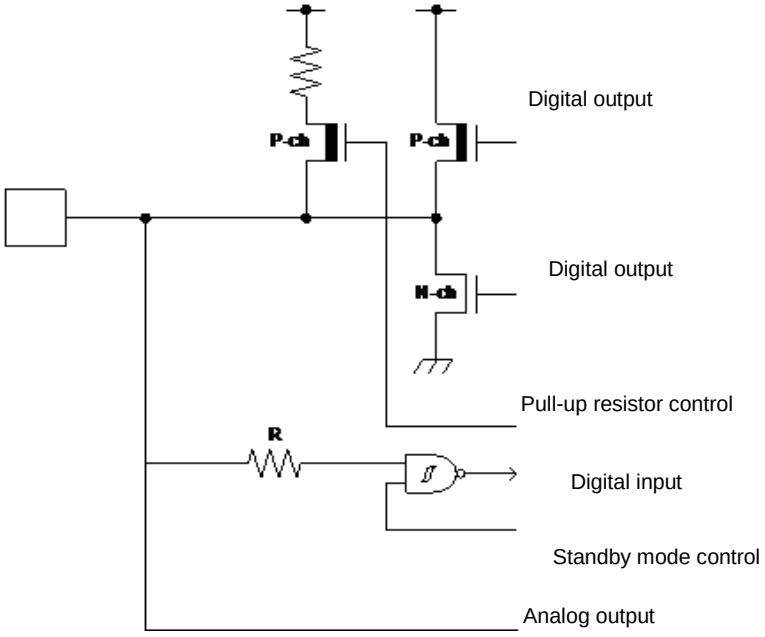
- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
12	-	-	P5A SOT7_0 INT16_2	F	J
13	-	-	P5B SCK7_0 INT17_2	F	J
14	9	9	P30 TIOB0_1 SCS60_1 MI2SWS6_1 INT03_2 WKUP4 COM7 SEG43	M	T
15	10	10	P31 TIOB1_1 SCK6_1 MI2SCK6_1 INT04_2 COM6 SEG42	M	S
16	11	11	P32 TIOB2_1 SOT6_1 MI2SDO6_1 INT05_2 COM5 SEG41	M	S
17	12	12	P33 TIOB3_1 SIN6_1 MI2SDI6_1 INT04_0 ADTG_6 COM4 SEG40	M	S
18	13	-	P34 SCS61_1 FRCK0_0 TIOB4_1	I	I
19	14	-	P35 SCS62_1 IC03_0 TIOB5_1 INT08_1 SEG37	L	S
20	15	-	P36 IC02_0 SIN5_2 INT09_1 WKUP11	I	N
21	16	-	P37 IC01_0 SOT5_2 INT10_1	I	J

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
22	17	-	P38 IC00_0 SCK5_2 INT11_1	F	J
23	18	13	P39 DTTI0X_0 TIOB4_0 ADTG_2 INT06_0 COM3	N	S
24	19	14	P3A RTO00_0 TIOA0_1 RTCCO_2 SUBOUT_2 IC1_CIN_0 INT07_0 COM2	N	S
25	20	15	P3B RTO01_0 TIOA1_1 IC1_DATA_0 COM1	N	P
26	21	16	P3C RTO02_0 TIOA2_1 INT18_2 IC1_RST_0 COM0	N	S
27	22	17	P3D RTO03_0 TIOA3_1 IC1_VPEN_0 SEG36	L	P
28	23	18	P3E RTO04_0 TIOA4_1 IC1_VCC_0 INT19_2 WKUP8 SEG35	L	T
29	24	19	P3F RTO05_0 TIOA5_1 IC1_CLK_0 SEG34	L	P
30	25	20	VSS	-	-
31	26	-	VCC	-	-
32	27	-	P40 TIOA0_0 IC0_CLK_1 INT12_1 SIN1_2	F	J

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-
	TIOA1_1		25	20	15
	TIOA1_2		5	5	5
	TIOB1_0	Base timer ch.1 TIOB pin	48	43	33
	TIOB1_1		15	10	10
	TIOB1_2		6	6	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-
	TIOA2_1		26	21	16
	TIOA2_2		116	96	76
	TIOB2_0	Base timer ch.2 TIOB pin	49	44	34
	TIOB2_1		16	11	11
	TIOB2_2		115	95	75
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-
	TIOA3_1		27	22	17
	TIOA3_2		105	90	70
	TIOB3_0	Base timer ch.3 TIOB pin	50	45	35
	TIOB3_1		17	12	12
	TIOB3_2		106	91	71
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21
	TIOA4_1		28	23	18
	TIOA4_2		51	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	23	18	13
	TIOB4_1		18	13	-
	TIOB4_2		52	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	37	32	22
	TIOA5_1		29	24	19
	TIOA5_2		97	82	-
	TIOB5_0	Base timer ch.5 TIOB pin	94	79	63
	TIOB5_1		19	14	-
	TIOB5_2		98	83	-
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-
	TIOA6_1		114	94	74
	TIOA6_2		82	-	-
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-
	TIOB6_1		113	93	73
	TIOB6_2		81	-	-
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-
	TIOA7_1		86	71	58
	TIOA7_2		109	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-
	TIOB7_1		87	72	59
	TIOB7_2		108	-	-
Debugger	SWCLK	Serial wire debug interface clock input pin	93	78	62
	SWDIO	Serial wire debug interface data input / output pin	95	80	64

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 5	SIN5_0 (MI2SDI5_0)	Multi-function serial interface ch.5 input pin. SIN5_0 pin operates as I2SIN5_0 when used as an I^2S pin (operation mode 2).	116	96	76
	SIN5_1		113	-	-
	SIN5_2		20	15	-
	SOT5_0 (SDA5_0) (MI2SDO5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA5 when used as an I^2C pin (operation mode 4). SOT5_0 pin operates as MI2SDO5_0 when used as an I^2S pin (operation mode 2).	115	95	75
	SOT5_1 (SDA5_1)		112	-	-
	SOT5_2 (SDA5_2)		21	16	-
	SCK5_0 (SCL5_0) (MI2SCK5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when used as a CSIO (operation mode 2) and as SCL5 when used as an I^2C pin (operation mode 4). SCK5_0 pin operates as MI2SCK5_0 when used as an I^2S pin (operation mode 2).	114	94	74
	SCK5_1 (SCL5_1)		111	-	-
	SCK5_2 (SCL5_2)		22	17	-
	MI2SWS5_0	I^2S word select (WS) output	113	93	73
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin. SIN6_1 pin operates as I2SIN6_1 when used as an I^2S pin (operation mode 2).	5	5	5
	SIN6_1 (MI2SDI6_1)		17	12	12
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I^2C pin (operation mode 4). SOT6_1 pin operates as MI2SDO6_1 when used as an I^2S pin (operation mode 2).	6	6	6
	SOT6_1 (SDA6_1) (MI2SDO6_1)		16	11	11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I^2C pin (operation mode 4). SCK6_6 pin operates as MI2SCK6_1 when used as an I^2S pin (operation mode 2).	7	7	7
	SCK6_1 (SCL6_1) (MI2SCK6_1)		15	10	10
	SCS60_1	Multi-function serial interface ch.6 serial chip select 0 input/output pin.	14	9	9
	SCS61_1	Multi-function serial interface ch.6 serial chip select 1 input/output pin.	18	13	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 input/output pin.	19	14	-
	MI2SWS6_1	I^2S word select (WS) output	14	9	9

Type	Circuit	Remarks
N		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD common output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}=-4 mA, I_{OL}= 4 mA ・Available to control of PZR registers.
O		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog output ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Peripheral Address Map

Start Address	End Address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function Timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		LCD Controller
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/ Remote Control Receiver
0x4003_5000	0x4003_5FFF		Low-Voltage Detection / DS mode / Vref Calibration
0x4003_6000	0x4003_6FFF		USB Clock Generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_FFFF		Reserved
0x4003_C900	0x4003_C9FF		Smart Card Interface
0x4003_CA00	0x4003_CAFF		I^2S Clock Generator
0x4003_CB00	0x4003_FFFF		Reserved
0x4004_0000	0x4005_FFFF	AHB	USB ch.0
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		DSTC
0x4006_2000	0x41FF_FFFF		Reserved

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
T	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
W	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
X	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output Maintain previous state / Internal input fixed at 0		

*1: Oscillation stops in Sub timer mode, Low-speed CR timer mode, Stop mode, RTC mode.

*2: Oscillation stops in Stop mode.

11.4 AC Characteristics

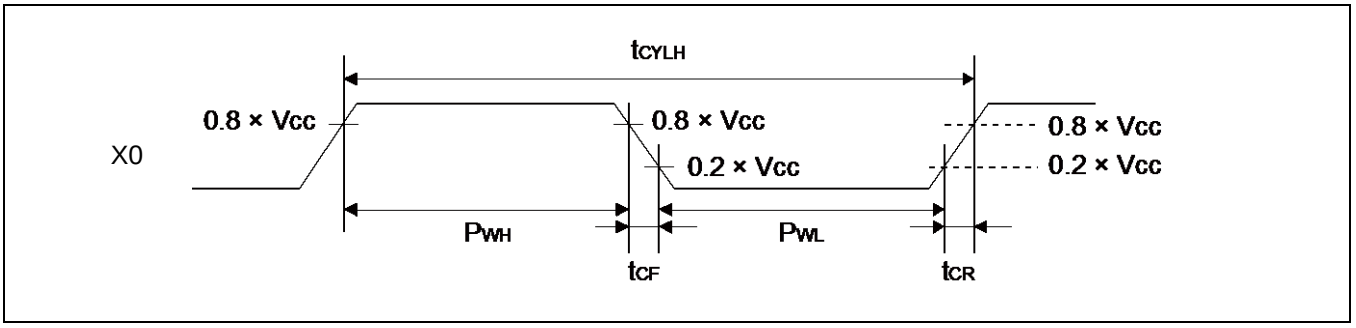
11.4.1 Main Clock Input Characteristics

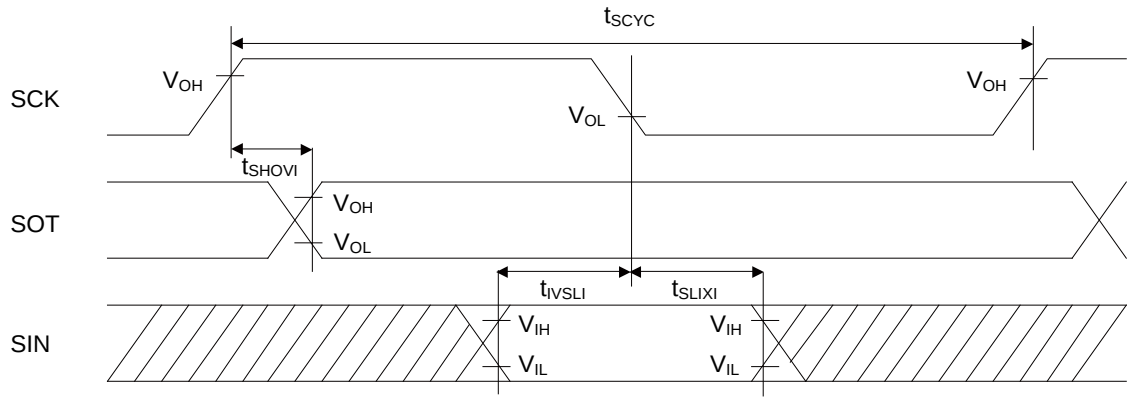
(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥ 2.7 V	4	48	MHz	When the crystal oscillator is connected
			V_{CC} < 2.7 V	4	20		
			-	4	48	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	f_{CM}	-	-	-	40.8	MHz	Master clock
	f_{CC}	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40.8	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40.8	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.5	-	ns	APB1 bus clock*2

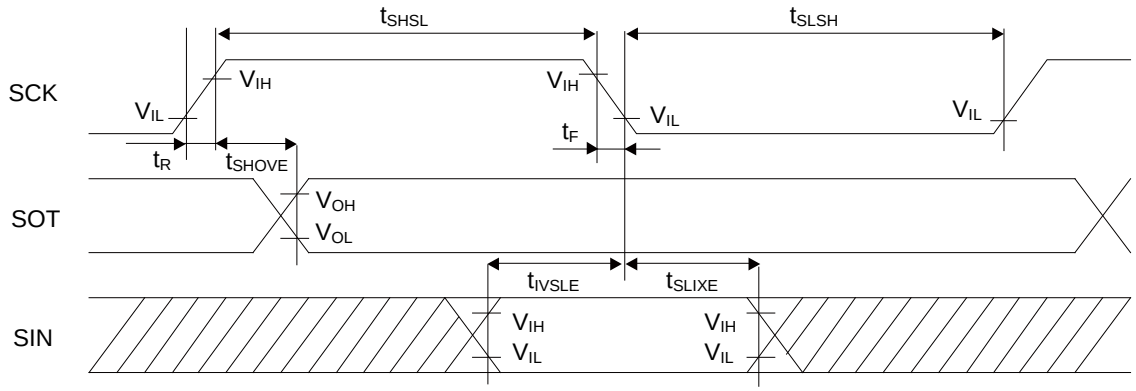
*1: For details of each internal operating clock, refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".





Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

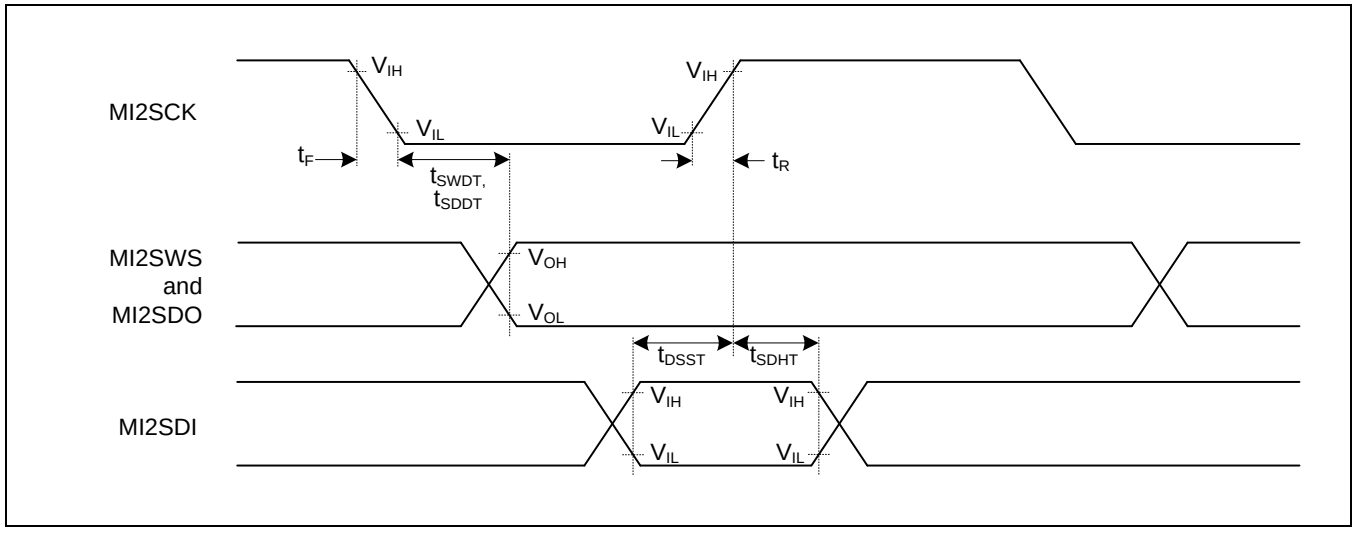
- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

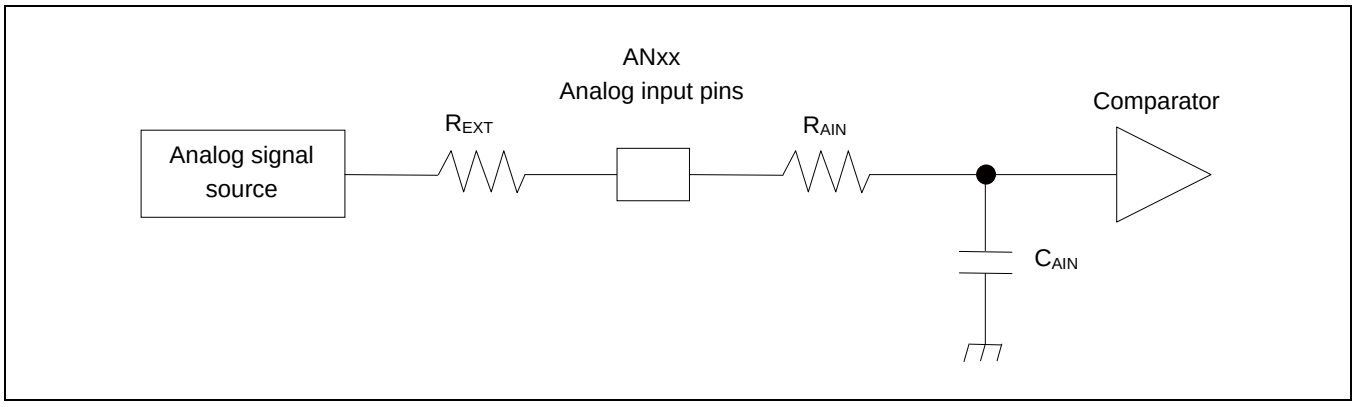
11.4.12 I²S Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency*1	f_{MI2SCK}	MI2SCKx	C_L=30 pF	-	6.144	-	6.144	MHz
I²S clock cycle time*1	t_{ICYC}	MI2SCKx		4 t_{CYCP}	-	4 t_{CYCP}	-	ns
I²S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t_{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t_{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t_{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t_{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	t_F	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	t_R	MI2SCKx		-	5	-	5	ns

*1: I²S clock should meet the multiple of PCLK (t_{ICYC}) and the frequency less than f_{MI2SCK} meantime. The detail information please refer to Chapter I²S of Communication Macro Part of Peripheral Manual.





(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D Converter = 2.2 kΩ with $2.7 \leq AV_{CC} \leq 3.6$ ch.1 to ch.14, ch.16 to ch.19
Input resistance of A/D Converter = 1.9 kΩ with $2.7 \leq AV_{CC} \leq 3.6$ ch.15
Input resistance of A/D Converter = 2.3 kΩ with $2.7 \leq AV_{CC} \leq 3.6$ ch.20 to ch.23
Input resistance of A/D Converter = 5.7 kΩ with $1.8 \leq AV_{CC} \leq 2.7$ ch.1 to ch.14, ch.16 to ch.19
Input resistance of A/D Converter = 5.6 kΩ with $1.8 \leq AV_{CC} \leq 2.7$ ch.15
Input resistance of A/D Converter = 5.8 kΩ with $1.8 \leq AV_{CC} \leq 2.7$ ch.20 to ch.23
Input resistance of A/D Converter = 12.6 kΩ with $1.65 \leq AV_{CC} \leq 1.8$ ch.1 to ch.19
Input resistance of A/D Converter = 12.7 kΩ with $1.65 \leq AV_{CC} \leq 1.8$ ch.20 to ch.23

C_{AIN}: Input capacitance of A/D Converter = 9.7 pF with $2.7 \leq AV_{CC} \leq 3.6$

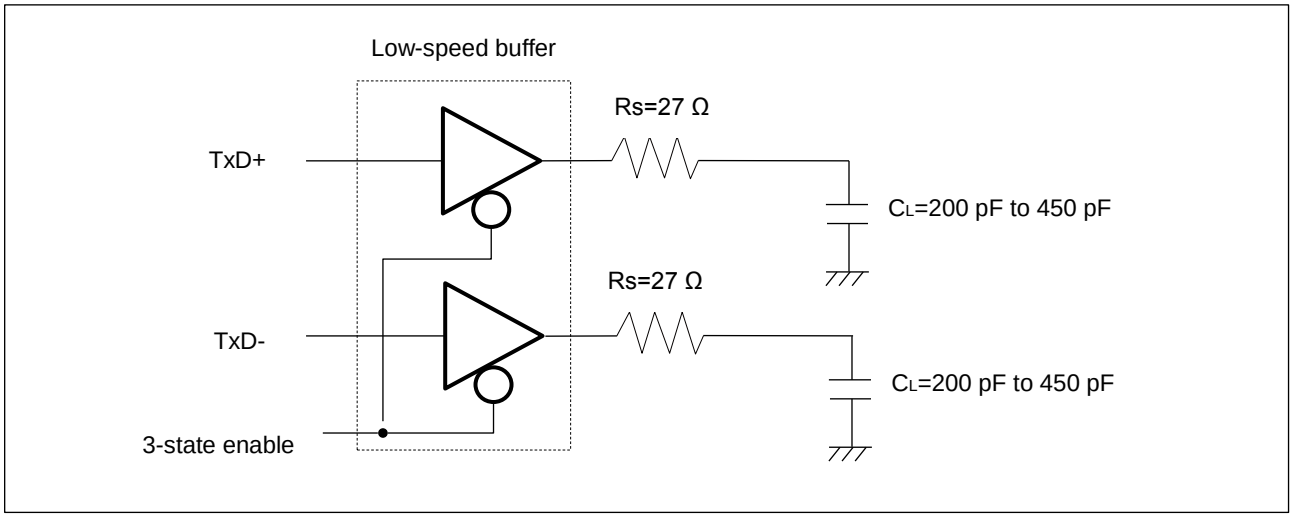
R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

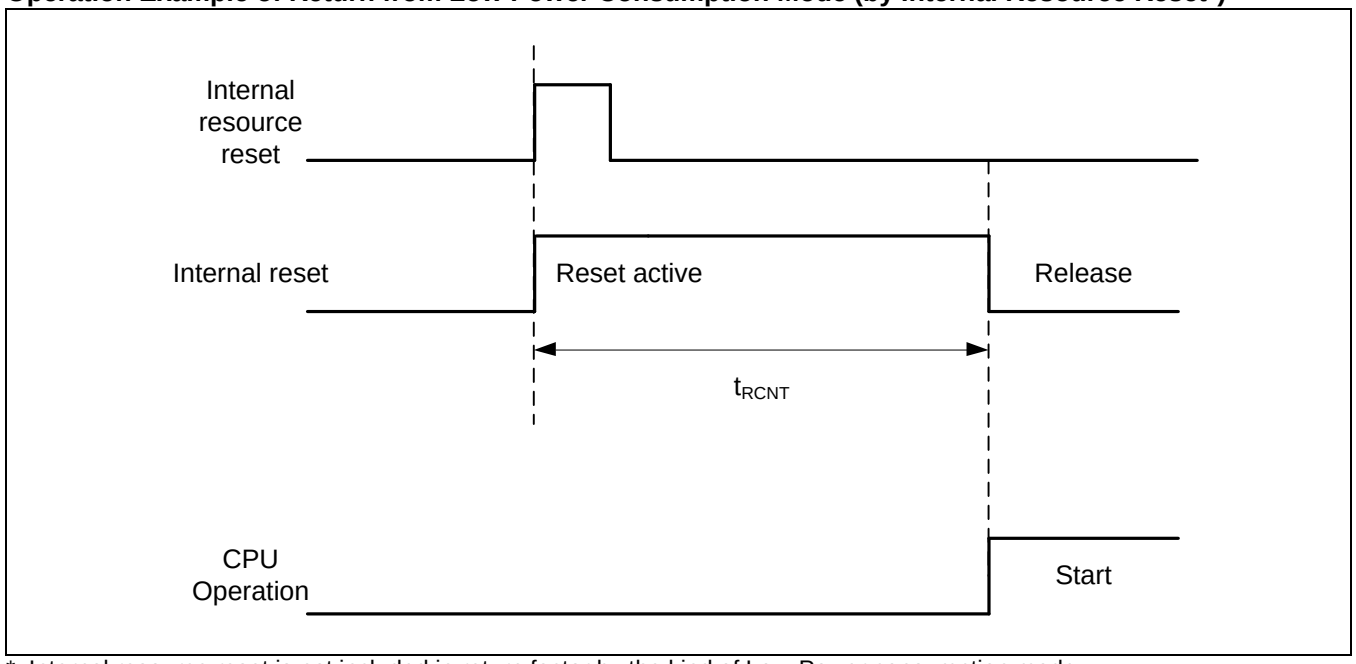
t_C: Compare time

t_{CCK} : Compare clock cycle

・Low-Speed Load (Compliance Load)



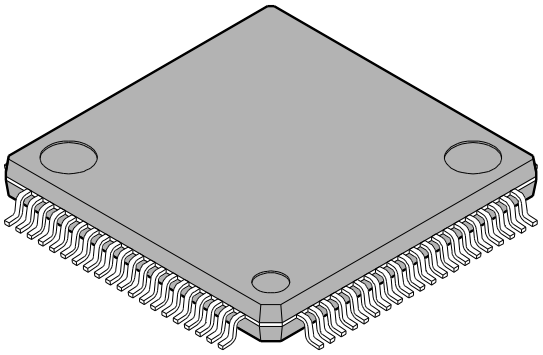
Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

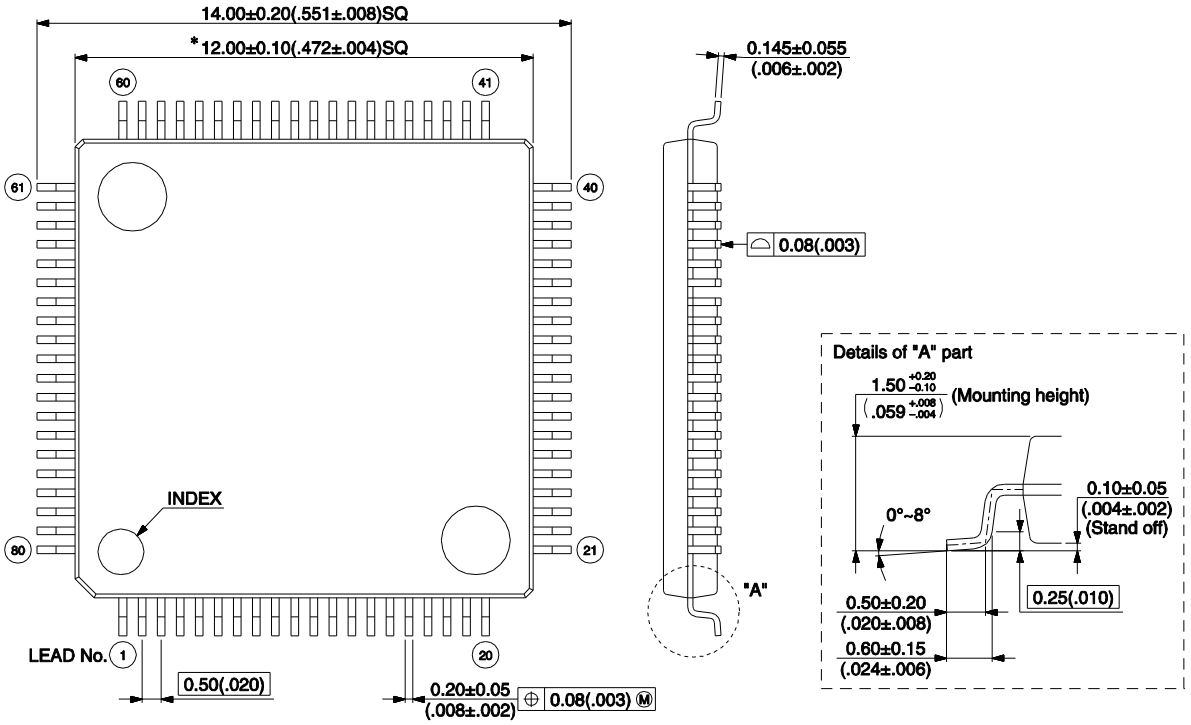
Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
(FPT-80P-M21)	Code (Reference)	P-LFQFP80-12×12-0.50

80-pin plastic LQFP
(FPT-80P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values