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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex® -M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I ² C, LINbus, SmartCard, UART/USART, USB
Peripherals	I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	304KB (304K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 23x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b84fhagv20000

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
49	44	34	P4C	L	R
			TIOB2_0		
			SOT7_1		
			CEC0_0		
			INT12_0		
			SEG29		
50	45	35	P4D	L	T
			TIOB3_0		
			SCK7_1		
			INT13_0		
			WKUP6		
			SEG28		
51	-	-	P70	F	I
			TIOA4_2		
			SCS71_1		
52	-	-	P71	F	J
			TIOB4_2		
			SCS72_1		
			INT13_2		
53	-	-	P72	F	J
			SIN2_0		
			TIOA6_0		
			INT14_2		
54	-	-	P73	F	J
			SOT2_0		
			TIOB6_0		
			INT15_2		
55	-	-	P74	F	I
			SCK2_0		
56	46	36	PE0	C	D
			MD1		
57	47	37	MD0	J	M
58	48	38	PE2	A	A
			X0		
59	49	39	PE3	A	B
			X1		
60	50	40	VSS	-	-
61	51	41	VCC	-	-
62	52	42	P10	P	K
			IC1_CLK_1		
			CTS1_1		
			AN00		
			SEG27		
63	53	43	P11	P	W
			IC1_VCC_1		
			SIN1_1		
			FRCK0_2		
			INT02_1		
			WKUP1		
			AN01		
			SEG26		

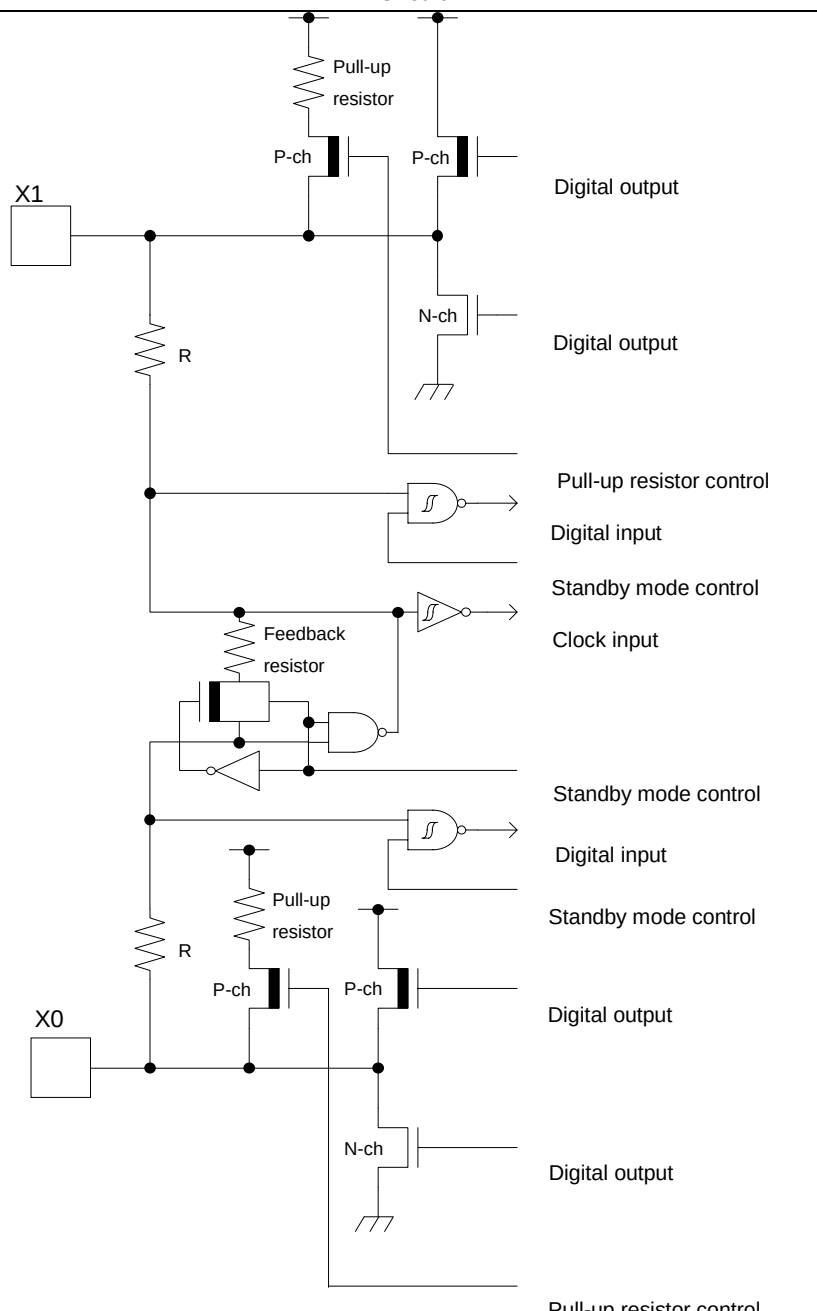
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
64	54	44	P12	P	K
			IC1_VPEN_1		
			SOT1_1		
			IC00_2		
			AN02		
			SEG25		
65	55	45	P13	P	K
			IC1_RST_1		
			SCK1_1		
			RTCCO_1		
			IC01_2		
			SUBOUT_1		
			AN03		
66	56	46	SEG24	P	V
			P14		
			IC1_DATA_1		
			RTS1_1		
			SIN0_1		
			IC02_2		
			INT03_1		
67	57	47	AN04	P	V
			SEG23		
			P15		
			IC1_CIN_1		
			SOT0_1		
			IC03_2		
			INT14_0		
68	58	48	AN05	P	V
			SEG22		
			P16		
			SCK0_1		
			INT15_0		
69	59	49	AN06	P	V
			SEG21		
			P17		
			SIN2_2		
			INT04_1		
70	60	50	AN07	P	K
71	61	51	SEG20		
72	62	52	AVCC		
73	63	53	AVSS		
			AVRL		
			AVRH	P	K
74	64	54	P18		
			SOT2_2		
			AN08		
			SEG19		
75	65	55	P19	P	K
			SCK2_2		
			IC00_1		
			AN09		
			SEG18		

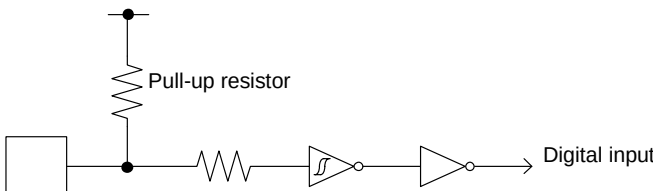
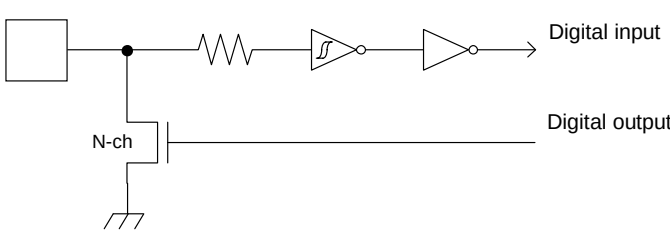
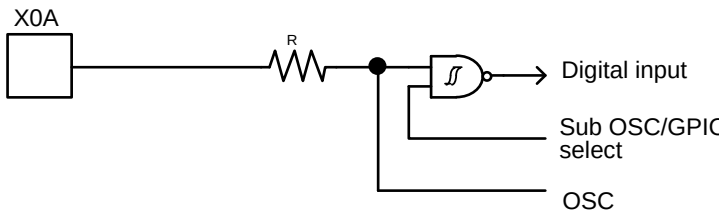
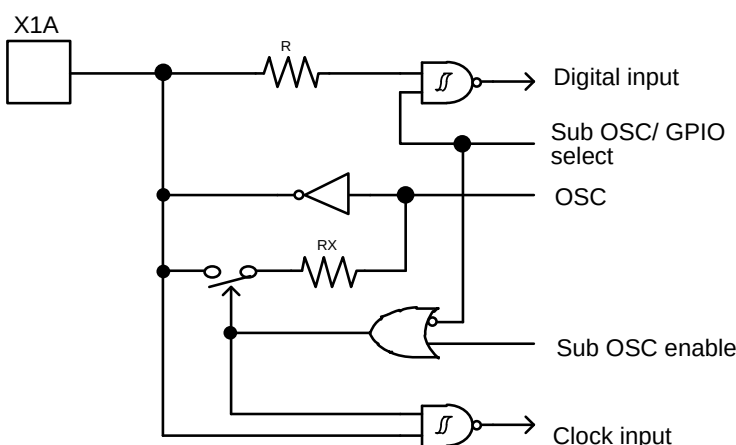
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
100	85	-	P08	P	V
			TIOA0_2		
			CTS4_2		
			INT16_0		
			AN23		
			SEG06		
101	86	-	P09	L	S
			TIOB0_2		
			RTS4_2		
			INT17_0		
			SEG05		
102	87	67	P0A	I	O
			SIN4_0		
			INT00_2		
			WKUP5		
			IC0_CIN_0		
			UHCONX0		
			CEC0_1		
103	88	68	P0B	K	Q
			INT18_0		
			UDM0		
104	89	69	P0C	K	Q
			INT19_0		
			UDP0		
105	90	70	P0D	L	S
			RTS4_0		
			TIOA3_2		
			INT20_0		
			SEG04		
106	91	71	IC0_VPEN_0	L	S
			P0E		
			CTS4_0		
			TIOB3_2		
			INT21_0		
			SEG03		
107	92	72	IC0_VCC_0	I	G
			P0F		
			CROUT_1		
			RTCCO_0		
			SUBOUT_0		
			MI2SMCK5_0		
			NMIX		
			WKUP0		
			IC0_CLK_0		
108	-	-	SCK4_0	F	J
			P68		
			SCK3_0		
			TIOB7_2		
109	-	-	INT12_2	F	J
			P67		
			SOT3_0		
			TIOA7_2		
110	-	-	INT22_0	F	J
			P66		
			SIN3_0		
			INT11_2		

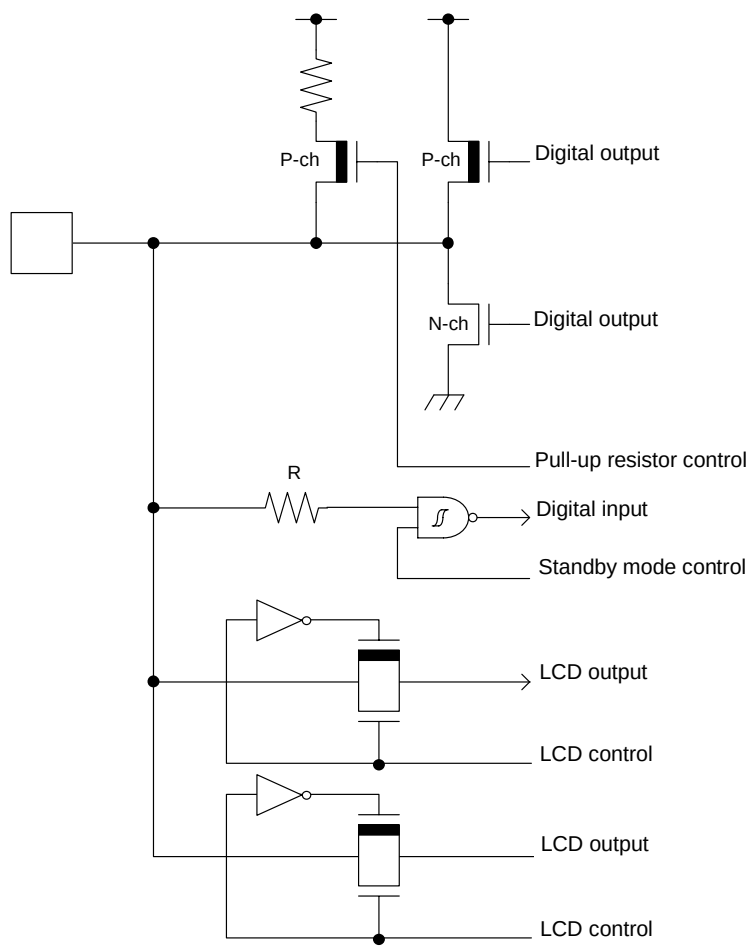
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 5	SIN5_0 (MI2SDI5_0)	Multi-function serial interface ch.5 input pin. SIN5_0 pin operates as I ² SIN5_0 when used as an I ² S pin (operation mode 2).	116	96	76
	SIN5_1		113	-	-
	SIN5_2		20	15	-
	SOT5_0 (SDA5_0) (MI2SDO5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA5 when used as an I ² C pin (operation mode 4). SOT5_0 pin operates as MI2SDO5_0 when used as an I ² S pin (operation mode 2).	115	95	75
	SOT5_1 (SDA5_1)		112	-	-
	SOT5_2 (SDA5_2)		21	16	-
	SCK5_0 (SCL5_0) (MI2SCK5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when used as a CSIO (operation mode 2) and as SCL5 when used as an I ² C pin (operation mode 4). SCK5_0 pin operates as MI2SCK5_0 when used as an I ² S pin (operation mode 2).	114	94	74
	SCK5_1 (SCL5_1)		111	-	-
	SCK5_2 (SCL5_2)		22	17	-
	MI2SWS5_0	I ² S word select (WS) output	113	93	73
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin. SIN6_1 pin operates as I ² SIN6_1 when used as an I ² S pin (operation mode 2).	5	5	5
	SIN6_1 (MI2SDI6_1)		17	12	12
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I ² C pin (operation mode 4). SOT6_1 pin operates as MI2SDO6_1 when used as an I ² S pin (operation mode 2).	6	6	6
	SOT6_1 (SDA6_1) (MI2SDO6_1)		16	11	11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I ² C pin (operation mode 4). SCK6_6 pin operates as MI2SCK6_1 when used as an I ² S pin (operation mode 2).	7	7	7
	SCK6_1 (SCL6_1) (MI2SCK6_1)		15	10	10
	SCS60_1	Multi-function serial interface ch.6 serial chip select 0 input/output pin.	14	9	9
	SCS61_1	Multi-function serial interface ch.6 serial chip select 1 input/output pin.	18	13	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 input/output pin.	19	14	-
	MI2SWS6_1	I ² S word select (WS) output	14	9	9

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	11	-	-
	SIN7_1		48	43	33
	SIN7_2		117	97	77
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin.	12	-	-
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I ² C pin (operation mode 4).	49	44	34
	SOT7_2 (SDA7_2)		118	98	78
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin.	13	-	-
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I ² C pin (operation mode 4).	50	45	35
	SCK7_2 (SCL7_2)		119	99	79
	SCS70_1	Multi-function serial interface ch.7 serial chip select 0 input/output pin.	47	42	32
	SCS71_1	Multi-function serial interface ch.7 serial chip select 1 input/output pin.	51	-	-
	SCS72_1	Multi-function serial interface ch.7 serial chip select 2 input/output pin.	52	-	-
Smart Card Interface 0	IC0_VCC_0	Smart card ch.0 power enable output pin	106	91	71
	IC0_VCC_1		33	28	-
	IC0_VPEN_0	Smart card ch.0 programming output pin	105	90	70
	IC0_VPEN_1		34	29	-
	IC0_RST_0	Smart card ch.0 reset output pin	114	94	74
	IC0_RST_1		35	30	-
	IC0_CIN_0	Smart card ch.0 insert detection input pin	102	87	67
	IC0_CIN_1		37	32	22
	IC0_CLK_0	Smart card ch.0 serial interface clock output pin	107	92	72
	IC0_CLK_1		32	27	-
	IC0_DATA_0	Smart card ch.0 serial interface data input/output pin	113	93	73
	IC0_DATA_1		36	31	21
Smart Card Interface 1	IC1_VCC_0	Smart card ch.1 power enable output pin	28	23	18
	IC1_VCC_1		63	53	43
	IC1_VPEN_0	Smart card ch.1 programming output pin	27	22	17
	IC1_VPEN_1		64	54	44
	IC1_RST_0	Smart card ch.1 reset output pin	26	21	16
	IC1_RST_1		65	55	45
	IC1_CIN_0	Smart card ch.1 insert detection input pin	24	19	14
	IC1_CIN_1		67	57	47
	IC1_CLK_0	Smart card ch.1 serial interface clock output pin	29	24	19
	IC1_CLK_1		62	52	42
	IC1_DATA_0	Smart card ch.1 serial interface data input/output pin	25	20	15
	IC1_DATA_1		66	56	46
USB	UDM0	USB device/host D – pin	103	88	68
	UDP0	USB device/host D + pin	104	89	69
	UHCONX0	USB external pull-up control pin	102	87	67

5. I/O Circuit Type

Type	Circuit	Remarks
A	 Pull-up resistor P-ch P-ch N-ch Digital output Digital output Pull-up resistor control Digital input Standby mode control Clock input Feedback resistor Standby mode control Digital input Standby mode control Pull-up resistor P-ch P-ch N-ch Digital output Digital output Pull-up resistor control	It is possible to select the main oscillation / GPIO function When the main oscillation is selected. Oscillation feedback resistor : Approximately 1 MΩ With standby mode control When the GPIO is selected. CMOS level output. CMOS level hysteresis input With pull-up resistor control With standby mode control Pull-up resistor : Approximately 33 kΩ $I_{OH} = -4\text{mA}$, $I_{OL} = 4\text{ mA}$

Type	Circuit	Remarks
B	 Pull-up resistor Digital input	CMOS level hysteresis input Pull-up resistor : Approximately 33 kΩ
C	 Digital input Digital output N-ch	Open drain output CMOS level hysteresis input
D	 X0A R Digital input Sub OSC/GPIO select OSC	• CMOS level output • Please refer to the "VBAT domain" setting of IO in of the "Peripheral Manual main part (MN710-00001)".
E	 X1A R Digital input Sub OSC/GPIO select OSC RX Sub OSC enable Clock input	It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 12 MΩ When the GPIO is selected. • CMOS level hysteresis input • Please refer to the "VBAT domain" setting of IO in the "Peripheral Manual main part (MN710-00001)".

Type	Circuit	Remarks
M	 P-ch Digital output N-ch Digital output Pull-up resistor control R Digital input Standby mode control LCD output LCD control LCD output LCD control	• CMOS level output • CMOS level hysteresis input • With input control • 5 V tolerant • LCD common output • LCD segment output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • Available to control of PZR registers. • When this pin is used as an I²C pin, the digital output P-ch transistor is always off

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

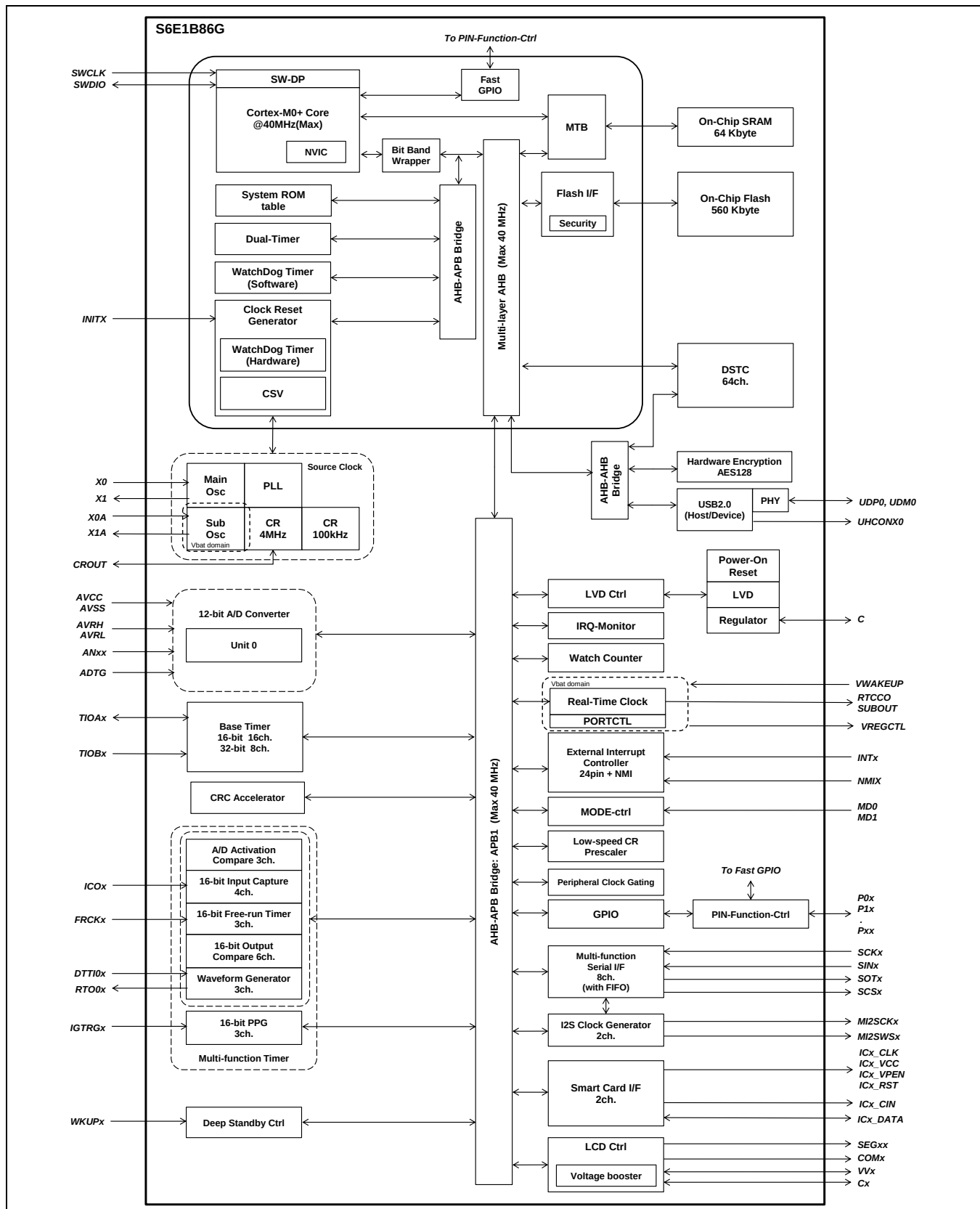
Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

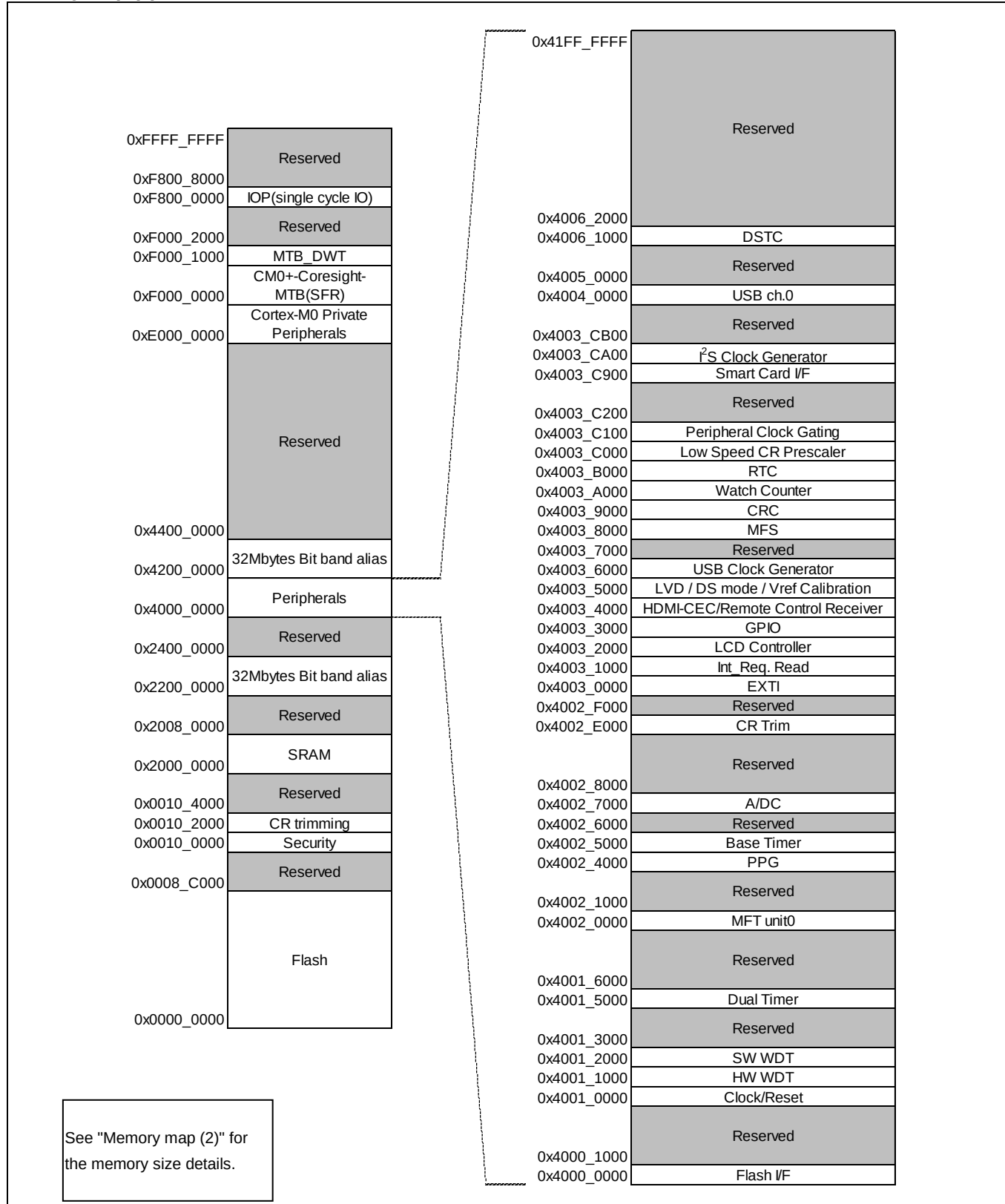
- (1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

8. Block Diagram



9. Memory Map

Memory Map (1)

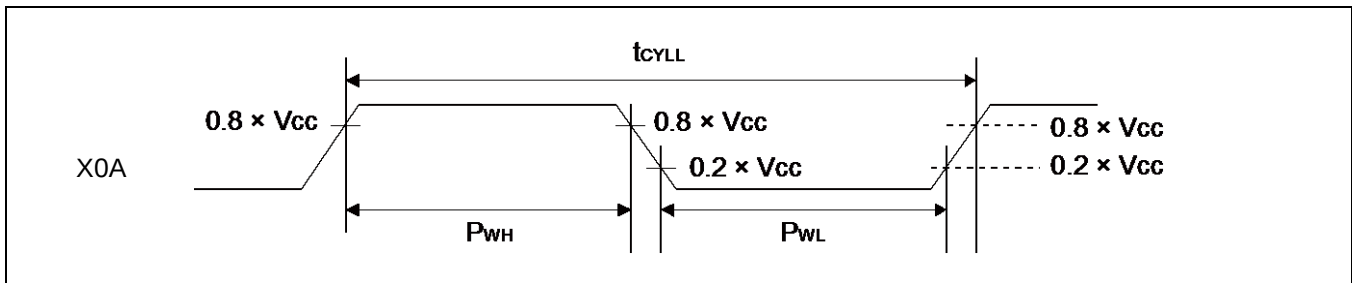


Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State				
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable				
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1				
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-				
O	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state				
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0				
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0					
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Internal input fixed at 0										
	GPIO selected													
P	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous State	Maintain previous State	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected				
	GPIO selected													
Q	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected				
	USB IO					Hi-Z/Input enabled	Hi-Z/Input enabled	Hi-Z/Input enabled	Hi-Z/Input enabled	Hi-Z/Input enabled				
	GPIO selected	Hi-Z	Hi-Z/Input enabled	Hi-Z/Input enabled		Maintain previous state	Hi-Z	GPIO	Hi-Z	GPIO				

11.4.2 Sub Clock Input Characteristics
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C})$

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected*
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	μs	When the external clock is used
Input clock pulse width	-		$P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}$	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



11.4.4 Operating Conditions of Main PLL

(In the Case of Using the Main Clock as the Input Clock of the PLL)

($V_{CC}=AV_{CC}=1.65\text{ V}$ to 3.6 V , $V_{SS}=AV_{SS}=0\text{ V}$, $T_A=-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* ¹ (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency* ²	f_{CLKPLL}	-	-	40.8	MHz	
USB clock frequency* ³	f_{CLKSPLL}	-	-	48	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*3: For more information about USB clock, see "Chapter: USB Clock Generation" in "FM0+ Family Peripheral Manual Communication Macro Part".

11.4.5 Operating Conditions of Main PLL

(In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)

($V_{CC}=AV_{CC}=1.65\text{ V}$ to 3.6 V , $V_{SS}=AV_{SS}=0\text{ V}$, $T_A=-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$)

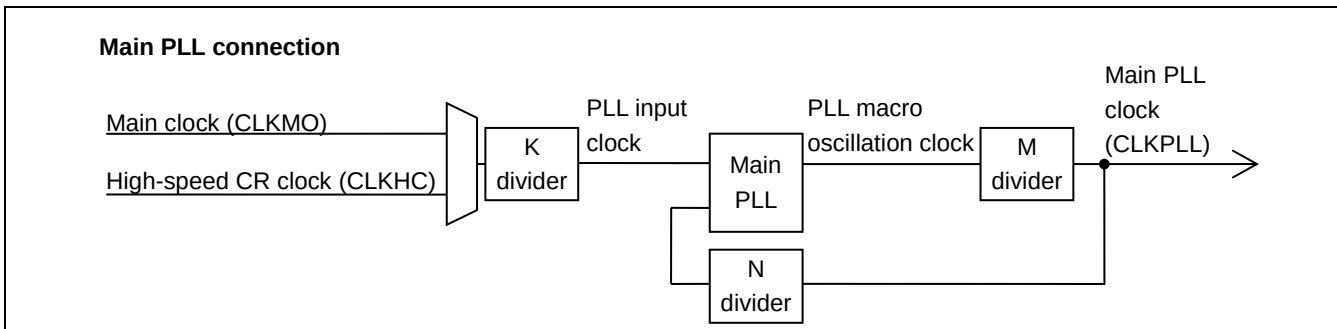
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* ¹ (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency* ²	f_{CLKPLL}	-	-	40.8	MHz	

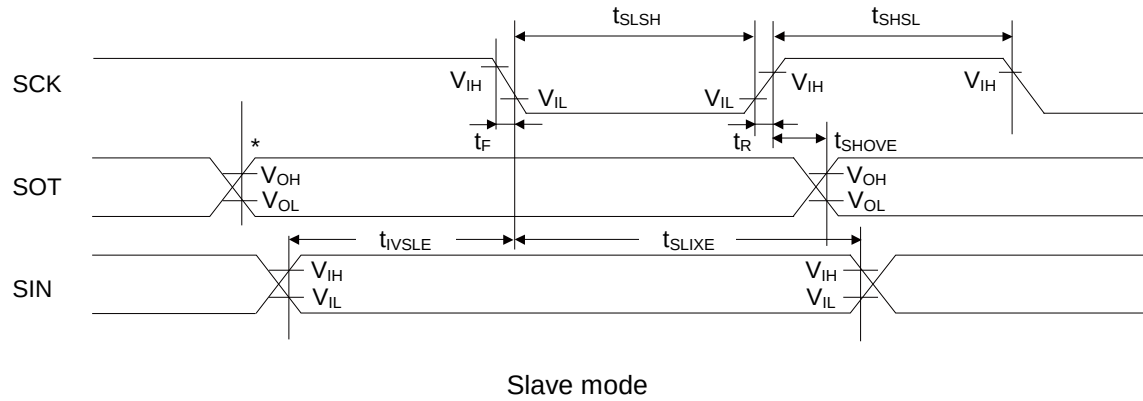
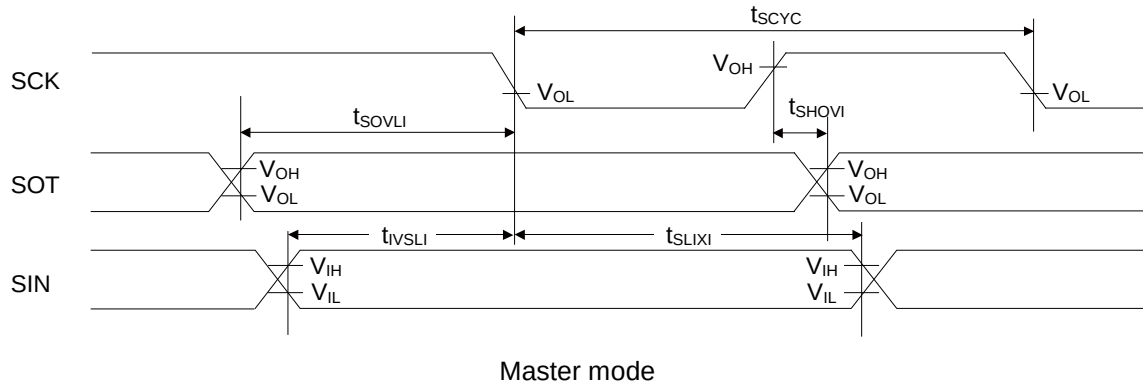
*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

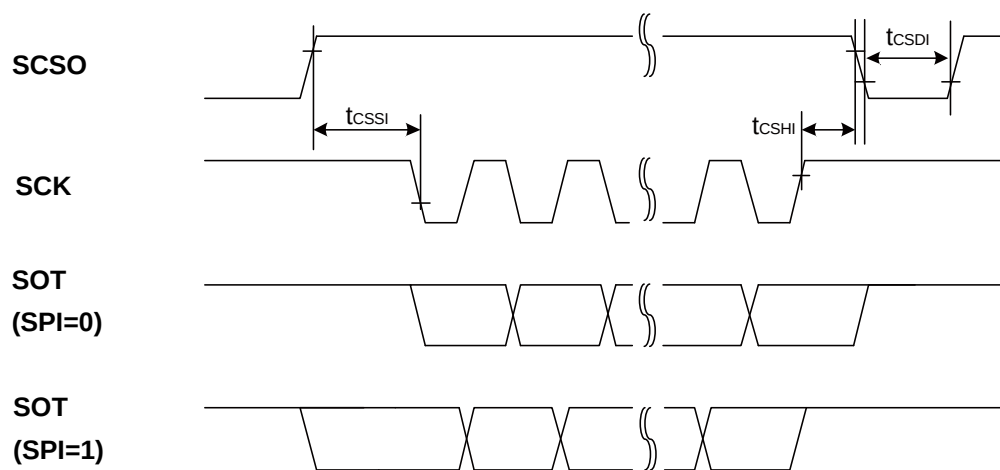
Note:

- For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

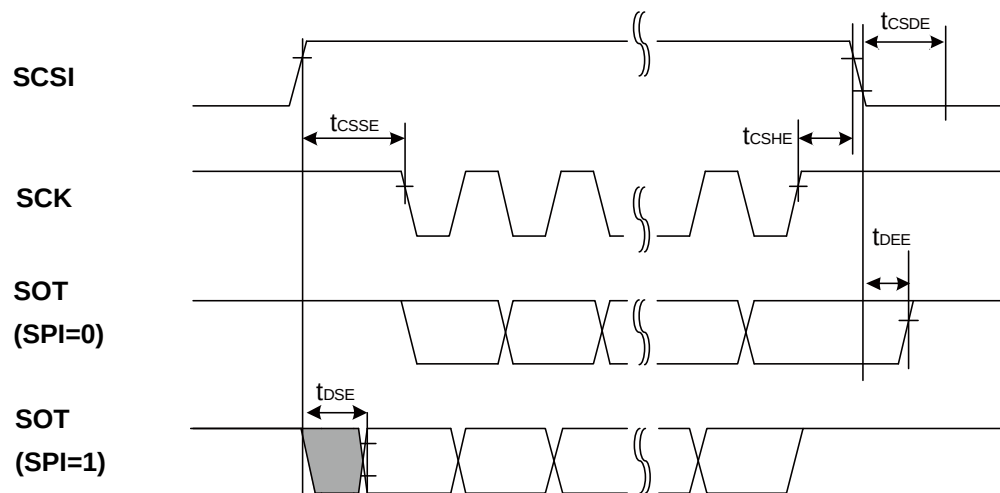




*: Changes when writing to TDR register



Master mode



Slave mode

11.4.13 Smart Card Interface Characteristics

 (V_{CC}=1.65 V to 3.3 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t _R	ICx_VCC, ICx_RST,	C _L =30 pF	4	20	ns	
Output falling time	t _F	ICx_CLK, ICx_DATA		4	20	ns	
Output clock frequency	f _{CLK}	ICx_CLK		-	20	MHz	
Duty cycle	Δ			45%	55%		

■ External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx_CIN pin when it's used as smart card reader function.

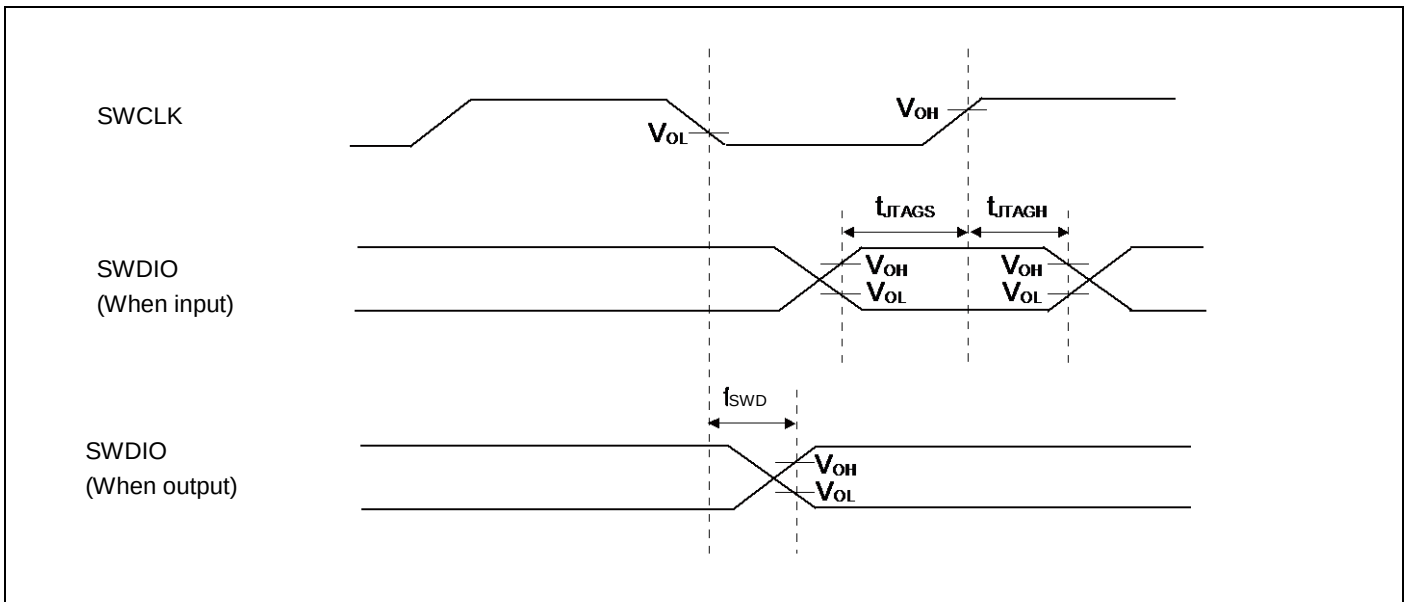
11.4.14 SW-DP Timing

 ($V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$, $V_{SS}=AV_{SS}=0\text{ V}$, $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- External load capacitance $C_L=30\text{ pF}$

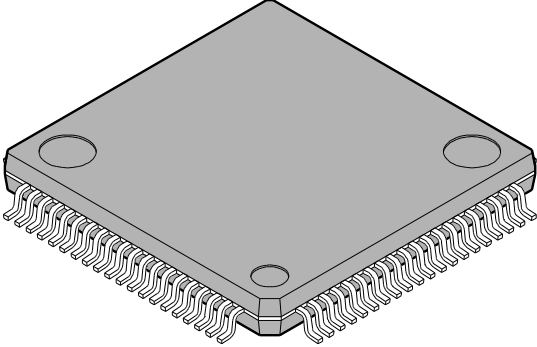


11.7.2 Low-Voltage Detection Interrupt

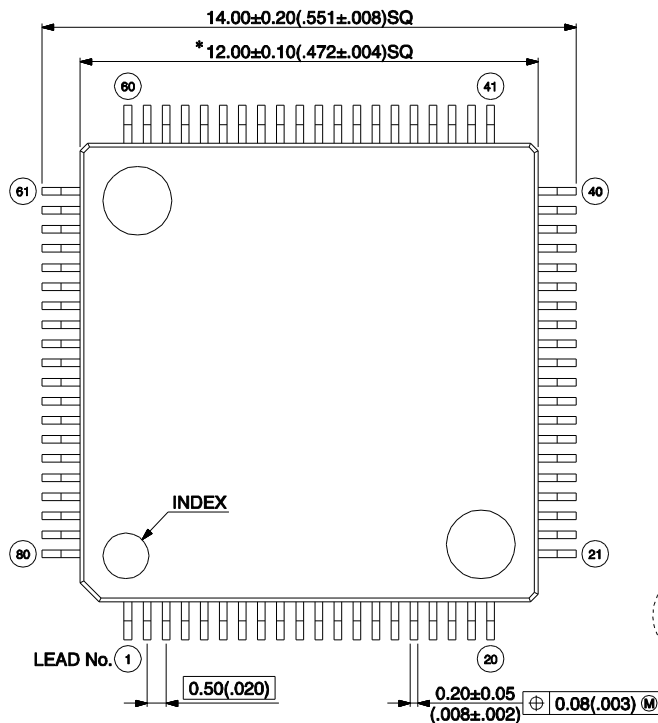
(T_A=−40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH	SVHRLI=00100	1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH	SVHRLI=00101	1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH	SVHRLI=00110	1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH	SVHRLI=00111	1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH	SVHRLI=01000	1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH	SVHRLI=01001	1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH	SVHRLI=01010	1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH	SVHRLI=01011	1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH	SVHRLI=01100	2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH	SVHRLI=01101	2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH	SVHRLI=01110	2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH	SVHRLI=01111	2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH	SVHRLI=10000	2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH	SVHRLI=10001	2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH	SVHRLI=10010	2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH	SVHRLI=10011	3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	t _{LVDW}	-	-	-	8160 × t _{CYCP} *	μs	
LVD detection delay time	t _{LVDL}	-	-	-	200	μs	

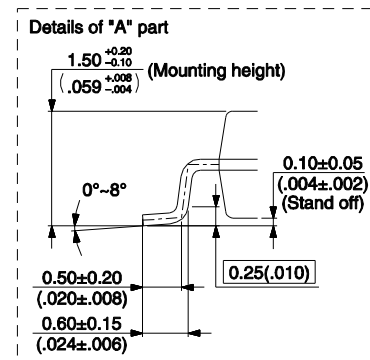
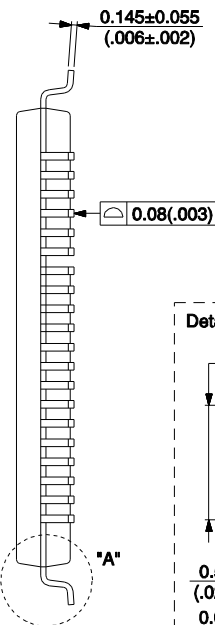
*: t_{CYCP} represents the APB1 bus clock cycle time.

80-pin plastic LQFP  (FPT-80P-M21)	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
	Code (Reference)	P-LFQFP80-12×12-0.50

80-pin plastic LQFP
(FPT-80P-M21)



Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
 Note: The values in parentheses are reference values