Infineon Technologies - S6E1B86E0AGF20000 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86e0agf20000

- I^2C
  - Standard-mode (Max: 100 kbps) supported / Fast-mode (Max 400 kbps) supported.
- I^2S
  - Using CSIO (ch.5, ch.6) and I^2S clock generator
  - Supports two transfer protocol
    - I^2S
    - MSB-justified
  - Master mode only

Descriptor System Data Transfer Controller (DSTC) (64 Channels)

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor
- system and, following the specified contents of the Descriptor that has already been constructed on the
- memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

A/D Converter (Max: 24 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 µs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 102 fast general-purpose I/O ports @120-pin package
- Certain ports are 5 V tolerant.
  See 4. List of Pin Functions and 5. I/O Circuit Type for the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Multi-Function Timer

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

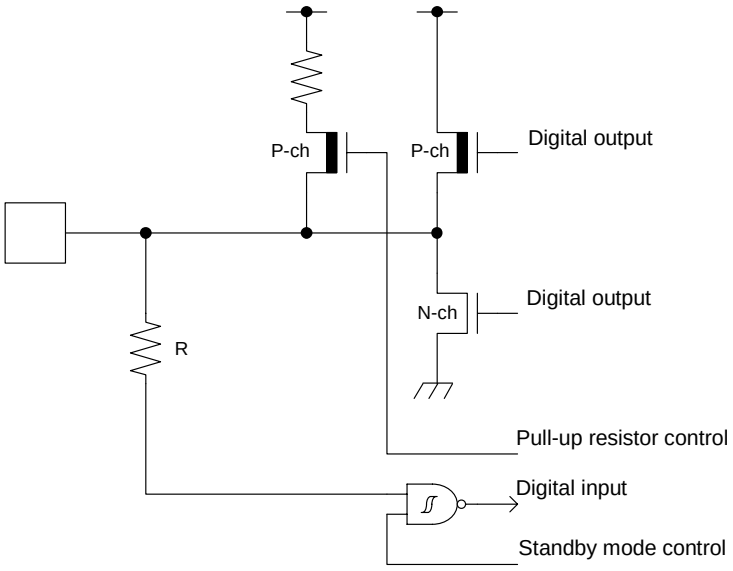
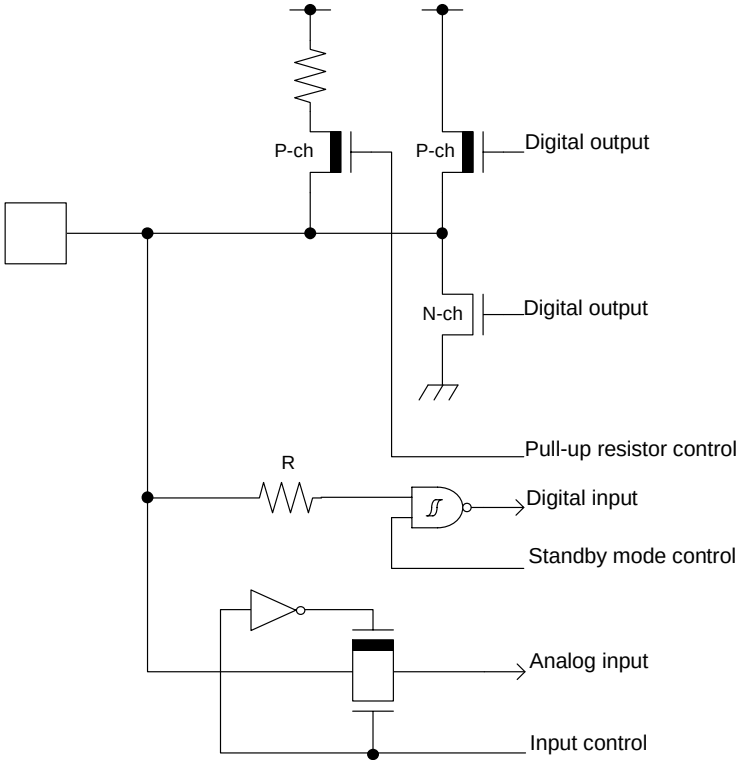
Real-Time Clock (RTC with Vbat)

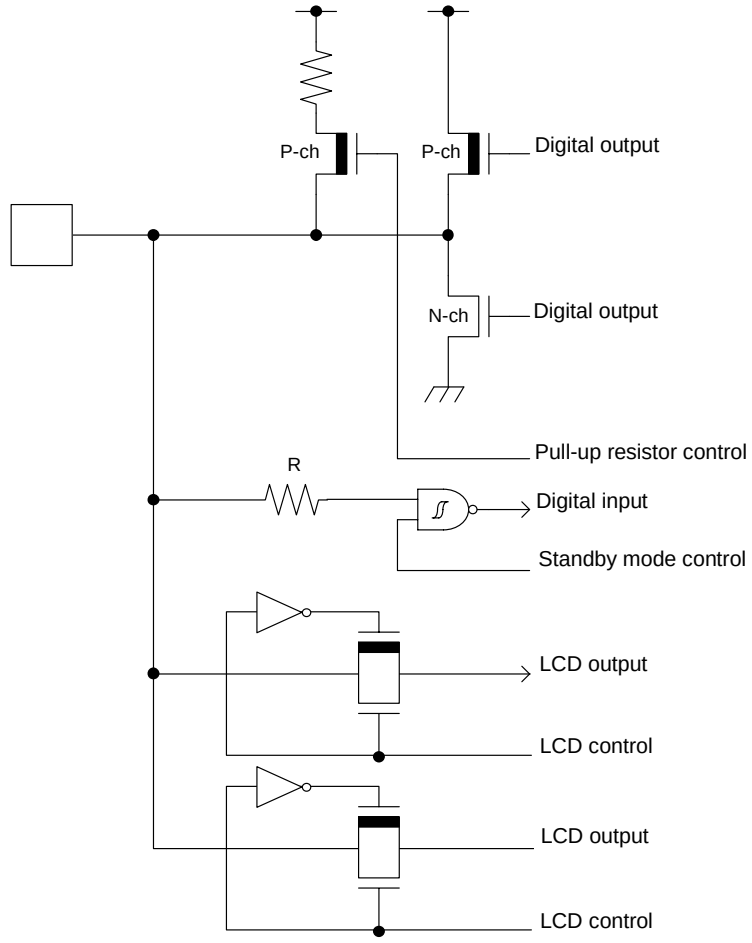
The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

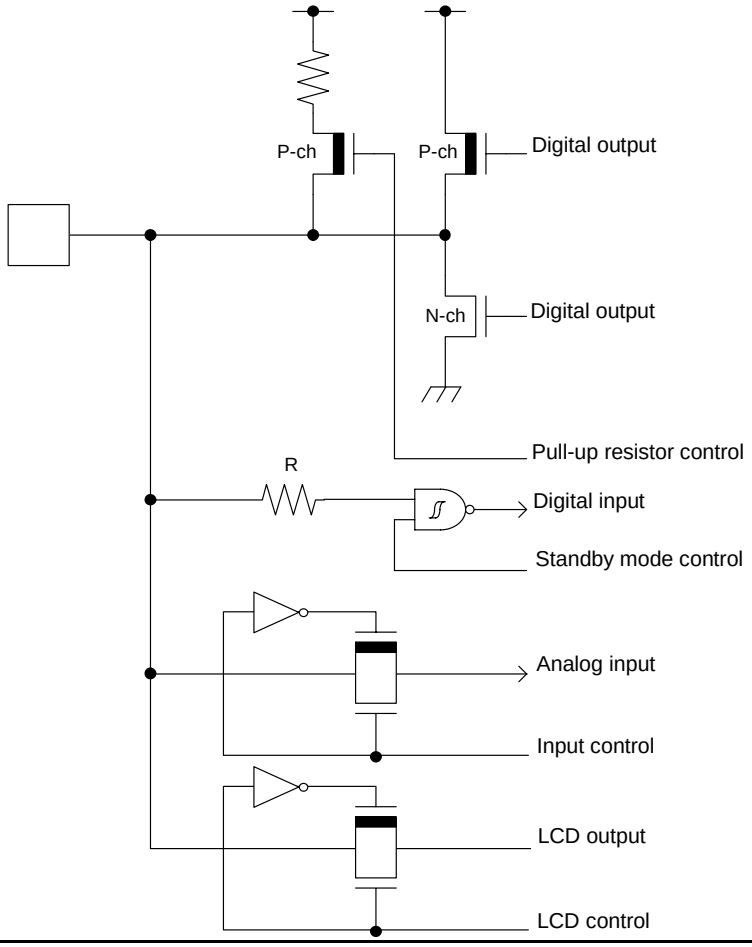
- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
49	44	34	P4C TIOB2_0 SOT7_1 CEC0_0 INT12_0 SEG29	L	R
50	45	35	P4D TIOB3_0 SCK7_1 INT13_0 WKUP6 SEG28	L	T
51	-	-	P70 TIOA4_2 SCS71_1	F	I
52	-	-	P71 TIOB4_2 SCS72_1 INT13_2	F	J
53	-	-	P72 SIN2_0 TIOA6_0 INT14_2	F	J
54	-	-	P73 SOT2_0 TIOB6_0 INT15_2	F	J
55	-	-	P74 SCK2_0	F	I
56	46	36	PE0 MD1	C	D
57	47	37	MD0	J	M
58	48	38	PE2 X0	A	A
59	49	39	PE3 X1	A	B
60	50	40	VSS	-	-
61	51	41	VCC	-	-
62	52	42	P10 IC1_CLK_1 CTS1_1 AN00 SEG27	P	K
63	53	43	P11 IC1_VCC_1 SIN1_1 FRCK0_2 INT02_1 WKUP1 AN01 SEG26	P	W

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 5	SIN5_0 (MI2SDI5_0)	Multi-function serial interface ch.5 input pin. SIN5_0 pin operates as I2SIN5_0 when used as an I^2S pin (operation mode 2).	116	96	76
	SIN5_1		113	-	-
	SIN5_2		20	15	-
	SOT5_0 (SDA5_0) (MI2SDO5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA5 when used as an I^2C pin (operation mode 4). SOT5_0 pin operates as MI2SDO5_0 when used as an I^2S pin (operation mode 2).	115	95	75
	SOT5_1 (SDA5_1)		112	-	-
	SOT5_2 (SDA5_2)		21	16	-
	SCK5_0 (SCL5_0) (MI2SCK5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when used as a CSIO (operation mode 2) and as SCL5 when used as an I^2C pin (operation mode 4). SCK5_0 pin operates as MI2SCK5_0 when used as an I^2S pin (operation mode 2).	114	94	74
	SCK5_1 (SCL5_1)		111	-	-
	SCK5_2 (SCL5_2)		22	17	-
	MI2SWS5_0	I^2S word select (WS) output	113	93	73
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin. SIN6_1 pin operates as I2SIN6_1 when used as an I^2S pin (operation mode 2).	5	5	5
	SIN6_1 (MI2SDI6_1)		17	12	12
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I^2C pin (operation mode 4). SOT6_1 pin operates as MI2SDO6_1 when used as an I^2S pin (operation mode 2).	6	6	6
	SOT6_1 (SDA6_1) (MI2SDO6_1)		16	11	11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I^2C pin (operation mode 4). SCK6_6 pin operates as MI2SCK6_1 when used as an I^2S pin (operation mode 2).	7	7	7
	SCK6_1 (SCL6_1) (MI2SCK6_1)		15	10	10
	SCS60_1	Multi-function serial interface ch.6 serial chip select 0 input/output pin.	14	9	9
	SCS61_1	Multi-function serial interface ch.6 serial chip select 1 input/output pin.	18	13	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 input/output pin.	19	14	-
	MI2SWS6_1	I^2S word select (WS) output	14	9	9

Type	Circuit	Remarks
F		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
G		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
M		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD common output ・LCD segment output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
P		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・5 V tolerant ・LCD segment output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

> CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
>
> (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
>
> (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf

List of Pin Status

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
H	Serial wire debug selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
J	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than the above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output Maintain previous state / Internal input fixed at 0
	GPIO selected									

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
L level maximum output current*4	I_{OL}	-	10	mA	
			39	mA	P0B / P0C
L level average output current*5	I_{OLAV}	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	
			- 39	mA	P0B / P0C
H level average output current*5	I_{OHAV}	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	250	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0 V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not to exceed V_{CC} + 0.5 V at power-on.

*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

*7: When P0C/UDP0 and P0B/UDM0 pins are used as GPIO (P0C, P0B).

*8: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

<WARNING>

- *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

Peripheral Current Dissipation

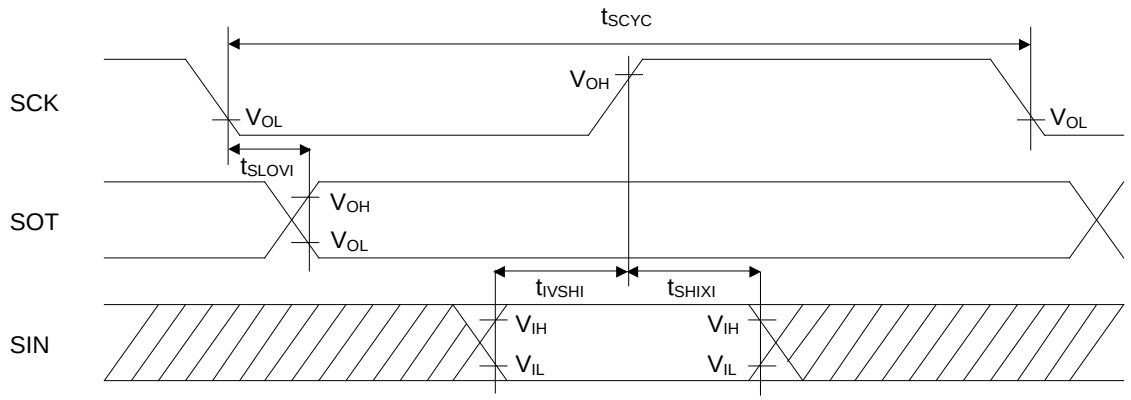
(V_{CC}= 3.3 V, T_A=25°C)

Clock System	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.02	0.04	0.11	0.22	mA	
	DSTC	At 2ch operation	0.07	0.15	0.37	0.74		
PCLK1	Base timer	At 4ch operation	0.02	0.04	0.08	0.16	mA	
	Multi-functional timer/PPG	At 1 unit/4ch operation	0.06	0.11	0.28	0.55		
	ADC	At 1 unit operation	0.02	0.04	010	0.20		
	Multi-function serial	At 1ch operation	0.03	0.06	0.16	0.31		

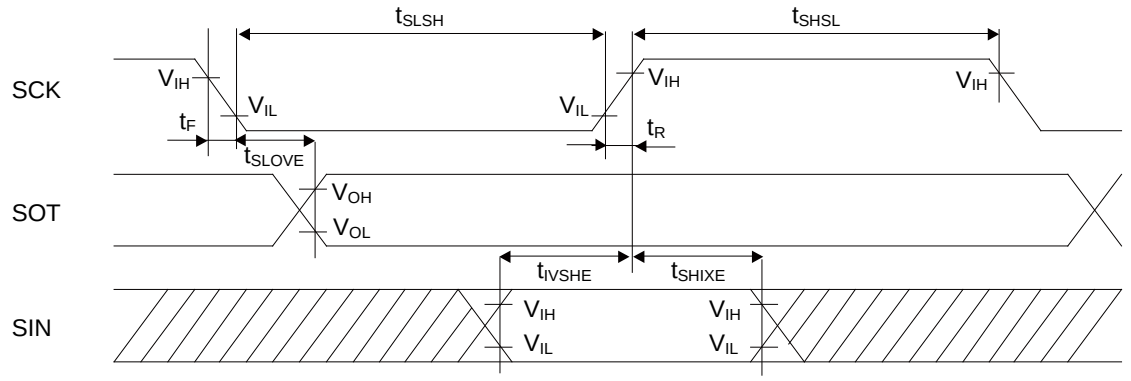
11.3.2 Pin Characteristics

(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	V_{CC} ≥ 2.7 V	V_{CC} × 0.8	-	V_{CC} +0.3	V	
			V_{CC} < 2.7 V	V_{CC} × 0.7				
		5 V tolerant input pin	V_{CC} ≥ 2.7 V	V_{CC} × 0.8	-	V_{SS} +5.5	V	
			V_{CC} < 2.7 V	V_{CC} × 0.7				
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	V_{CC} ≥ 2.7 V	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
			V_{CC} < 2.7 V			V_{CC} × 0.3		
		5 V tolerant input pin	V_{CC} ≥ 2.7 V	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
			V_{CC} < 2.7 V			V_{CC} × 0.3		
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 2.7 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 2.7 V, I_{OH} = - 2 mA	V_{CC} - 0.45				
		The pin doubled as USB I/O	-	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	
L level output voltage	V_{OL}	4 mA type	V_{CC} ≥ 2.7 V, I_{OL} 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 2.7 V, I_{OL}=2 mA					
		The pin doubled as USB I/O	-	V_{SS}	-	0.4	V	
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 2.7 V	21	33	66	kΩ	
			V_{CC} < 2.7 V	-	-	134		
Input capacitance	C_{IN}	Other than VCC, USBVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

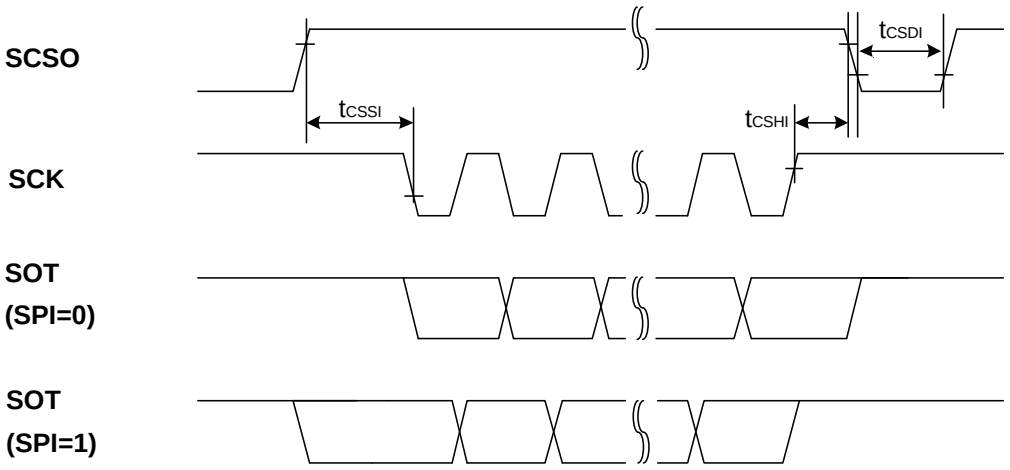
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

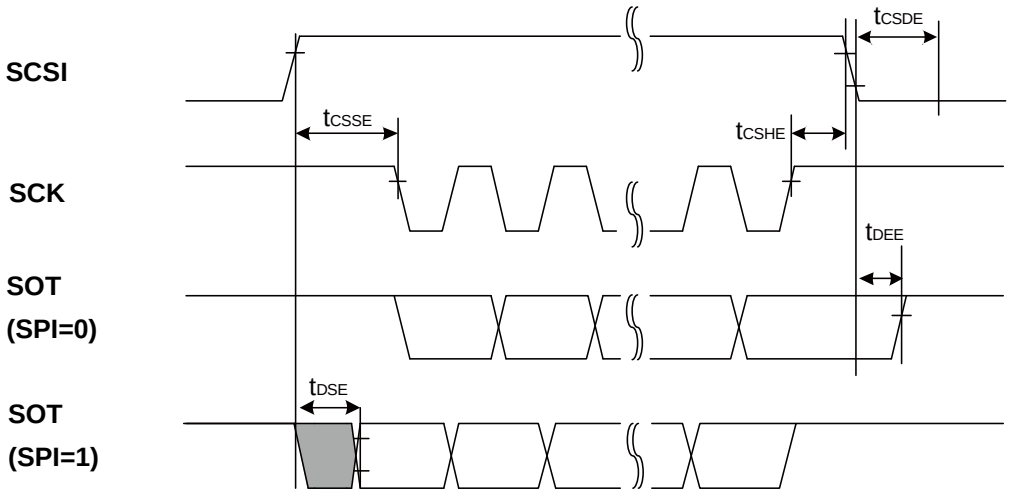
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode



Slave mode

11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed*1	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160× t_{CYCP}*2	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*1: The value of low voltage detection reset is always fixed.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

11.8 Flash Memory Write/Erase Characteristics

(V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ*	Max*		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

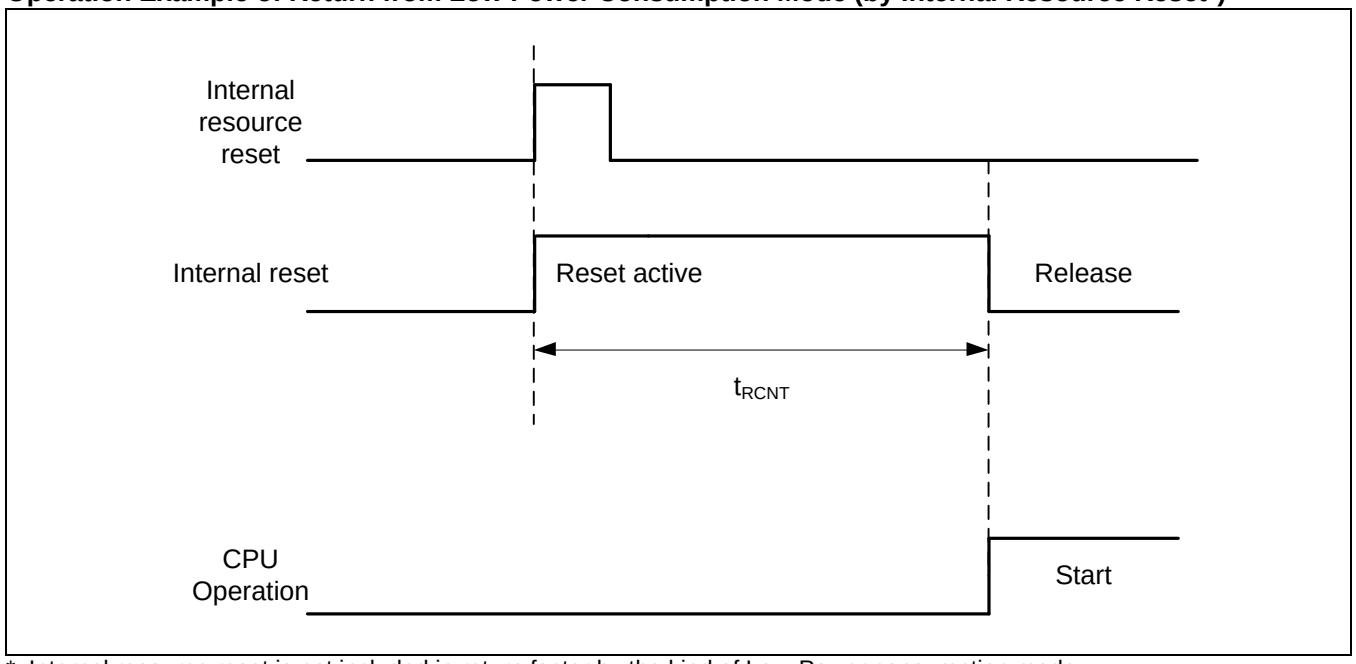
*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time (Target Value)

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*