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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

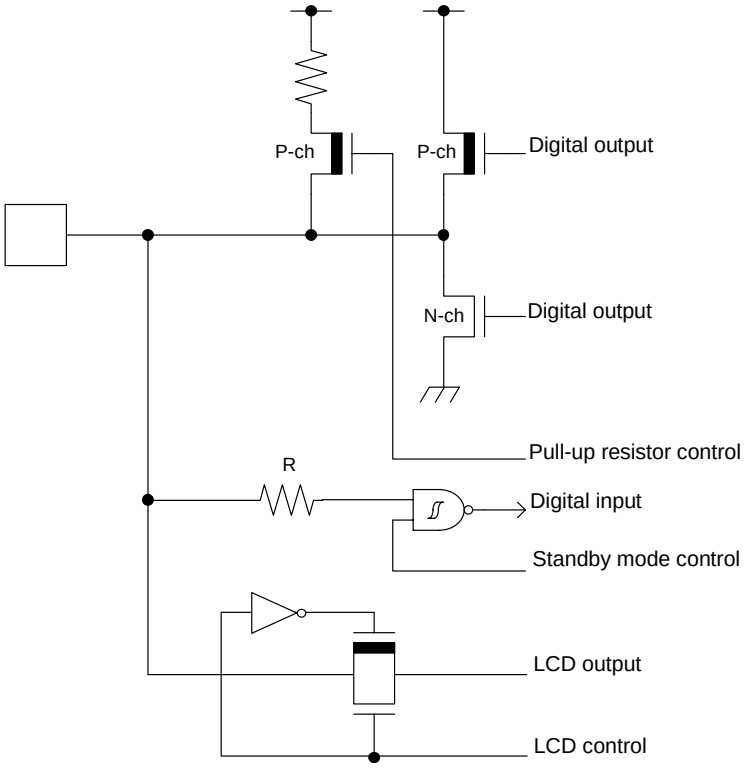
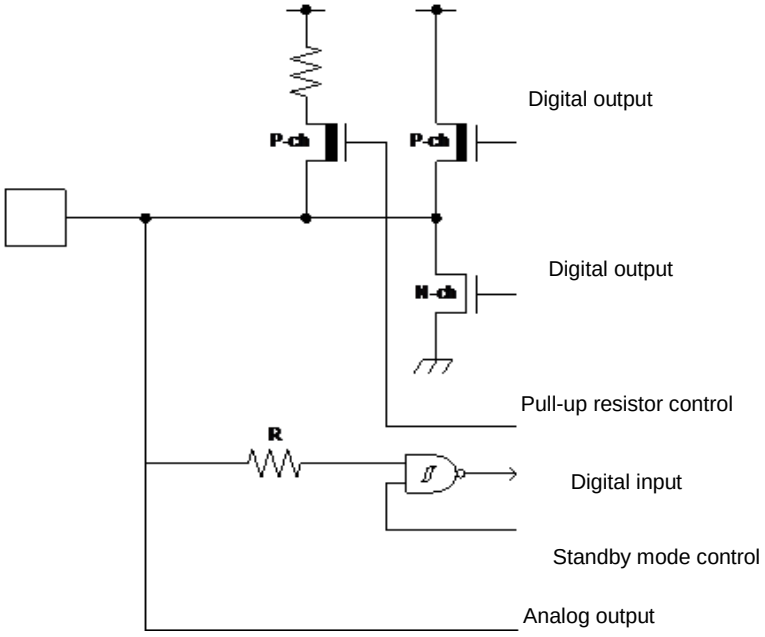
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86e0agv20000

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
33	28	-	P41 TIOA1_0 SOT1_2 IC0_VCC_1 INT13_1	F	J
34	29	-	P42 TIOA2_0 SCK1_2 IC0_VPEN_1 INT08_0	F	J
35	30	-	P43 TIOA3_0 CTS1_2 ADTG_7 IC0_RST_1 INT09_0	F	J
36	31	21	P44 TIOA4_0 IC0_DATA_1 INT10_0 RTS1_2 SEG33	L	S
37	32	22	P45 TIOA5_0 IC0_CIN_1 LVDI SEG32	L	P
38	33	23	C	-	-
39	34	24	VSS	-	-
40	35	25	VCC	-	-
41	36	26	INITX	B	C
42	37	27	P46 X0A	D	E
43	38	28	P47 X1A	E	F
44	39	29	P48 VREGCTL	I	I
45	40	30	P49 VWAKEUP	I	I
46	41	31	VBAT	-	-
47	42	32	P4A TIOB0_0 SCS70_1 INT21_1 SEG31	L	S
48	43	33	P4B TIOB1_0 SIN7_1 INT22_1 WKUP7 SEG30 IGTRG0_0	L	T

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
87	72	59	P22 SOT0_0 TIOB7_1 AN17 SEG12	P	K
88	73	60	P21 SIN0_0 INT06_1 WKUP2 AN18 SEG11	P	W
89	74	-	P20 INT05_0 CROUT_0 AN19 SEG10	P	V
90	75	-	VSS	-	-
91	76	-	VCC	-	-
92	77	61	P00 SOT3_2 INT14_1	I	J
93	78	62	P01 SWCLK	I	H
94	79	63	P02 SIN3_2 TIOB5_0	I	I
95	80	64	P03 SWDIO	I	H
96	81	65	P04 SCK3_2 INT06_2	I	J
97	82	-	P05 TIOA5_2 SIN4_2 INT00_1 WKUP10 AN20 SEG09	P	W
98	83	-	P06 TIOB5_2 SOT4_2 INT01_1 AN21 SEG08	P	V
99	84	66	P07 SCK4_2 ADTG_0 INT23_1 AN22 SEG07 SOT4_0	P	V

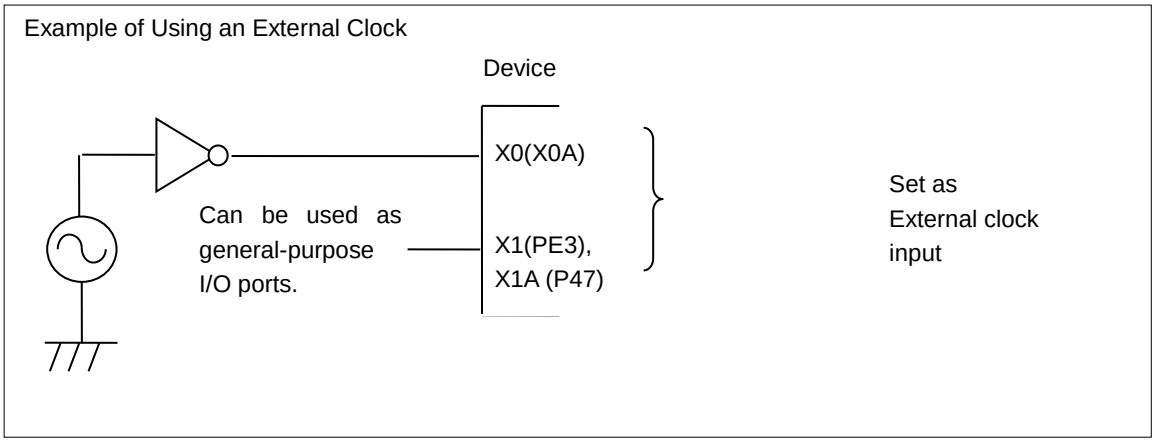
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT15_0	External interrupt request 15 input pin	68	58	48
	INT15_1		116	96	76
	INT15_2		54	-	-
	INT16_0	External interrupt request 16 input pin	100	85	-
	INT16_1		11	-	-
	INT16_2		12	-	-
	INT17_0	External interrupt request 17 input pin	101	86	-
	INT17_1		85	-	-
	INT17_2		13	-	-
	INT18_0	External interrupt request 18 input pin	103	88	68
	INT18_1		6	6	6
	INT18_2		26	21	16
	INT19_0	External interrupt request 19 input pin	104	89	69
	INT19_1		7	7	7
	INT19_2		28	23	18
	INT20_0	External interrupt request 20 input pin	105	90	70
	INT20_1		117	97	77
	INT20_2		77	67	57
	INT21_0	External interrupt request 21 input pin	106	91	71
	INT21_1		47	42	32
	INT21_2		78	68	-
	INT22_0	External interrupt request 22 input pin	109	-	-
	INT22_1		48	43	33
	INT22_2		79	69	-
	INT23_0	External interrupt request 23 input pin	111	-	-
	INT23_1		99	84	66
	INT23_2		80	70	-
	NMIX	Non-Maskable Interrupt input pin	107	92	72
GPIO	P00	General-purpose I/O port 0	92	77	61
	P01		93	78	62
	P02		94	79	63
	P03		95	80	64
	P04		96	81	65
	P05		97	82	-
	P06		98	83	-
	P07		99	84	66
	P08		100	85	-
	P09		101	86	-
	P0A		102	87	67
	P0B		103	88	68
	P0C		104	89	69
	P0D		105	90	70
	P0E		106	91	71
	P0F		107	92	72

Type	Circuit	Remarks
N		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD common output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}=-4 mA, I_{OL}= 4 mA ・Available to control of PZR registers.
O		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog output ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH}= -4 mA, I_{OL}= 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

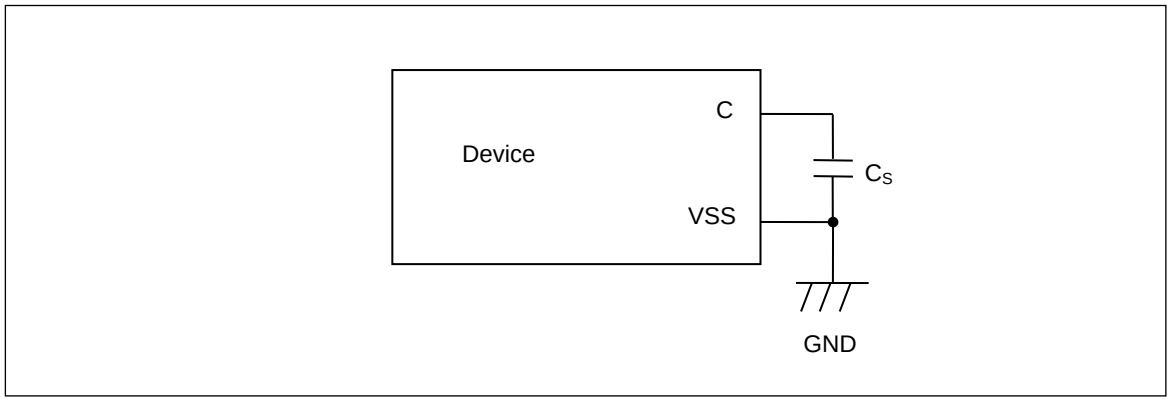


Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

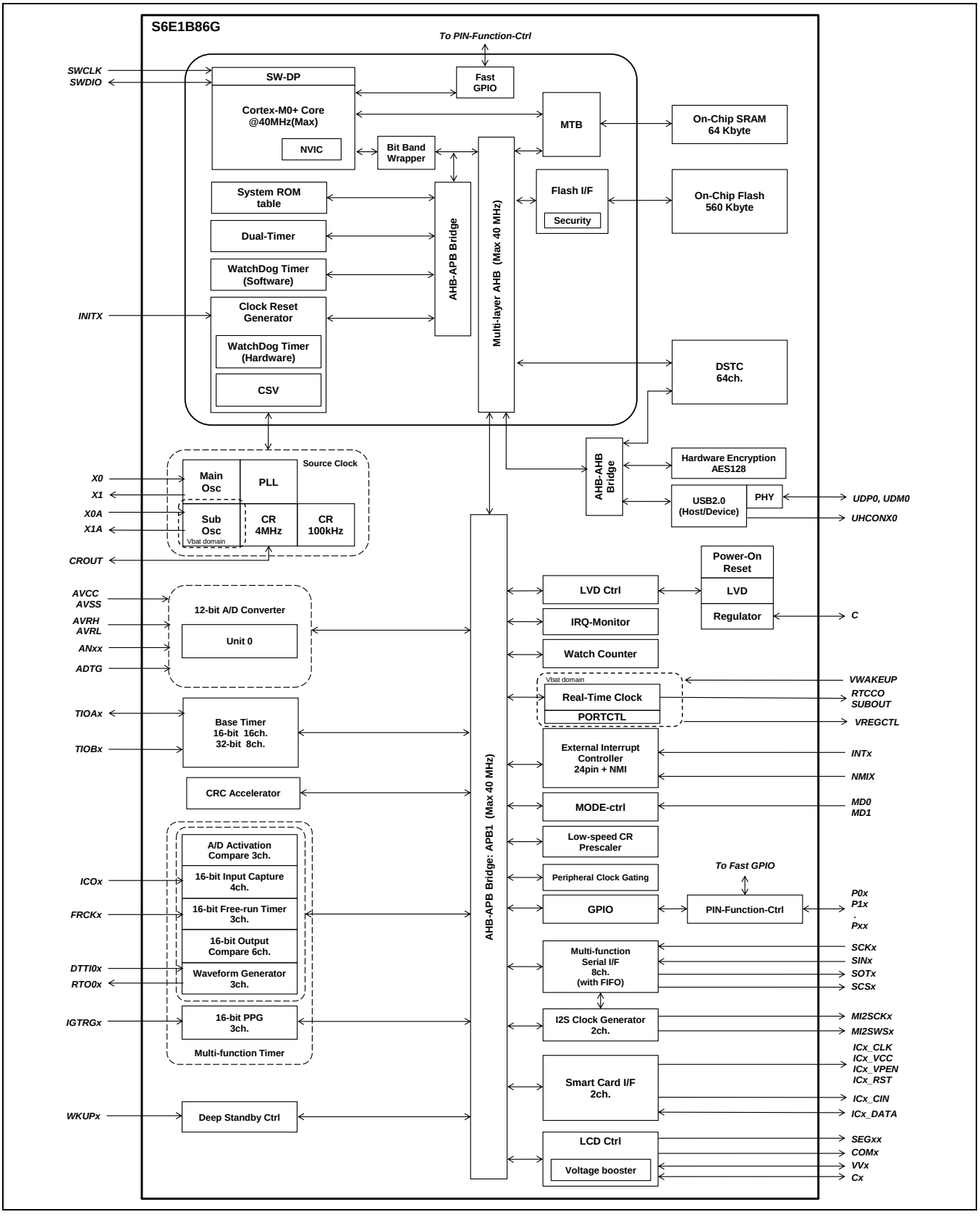
This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



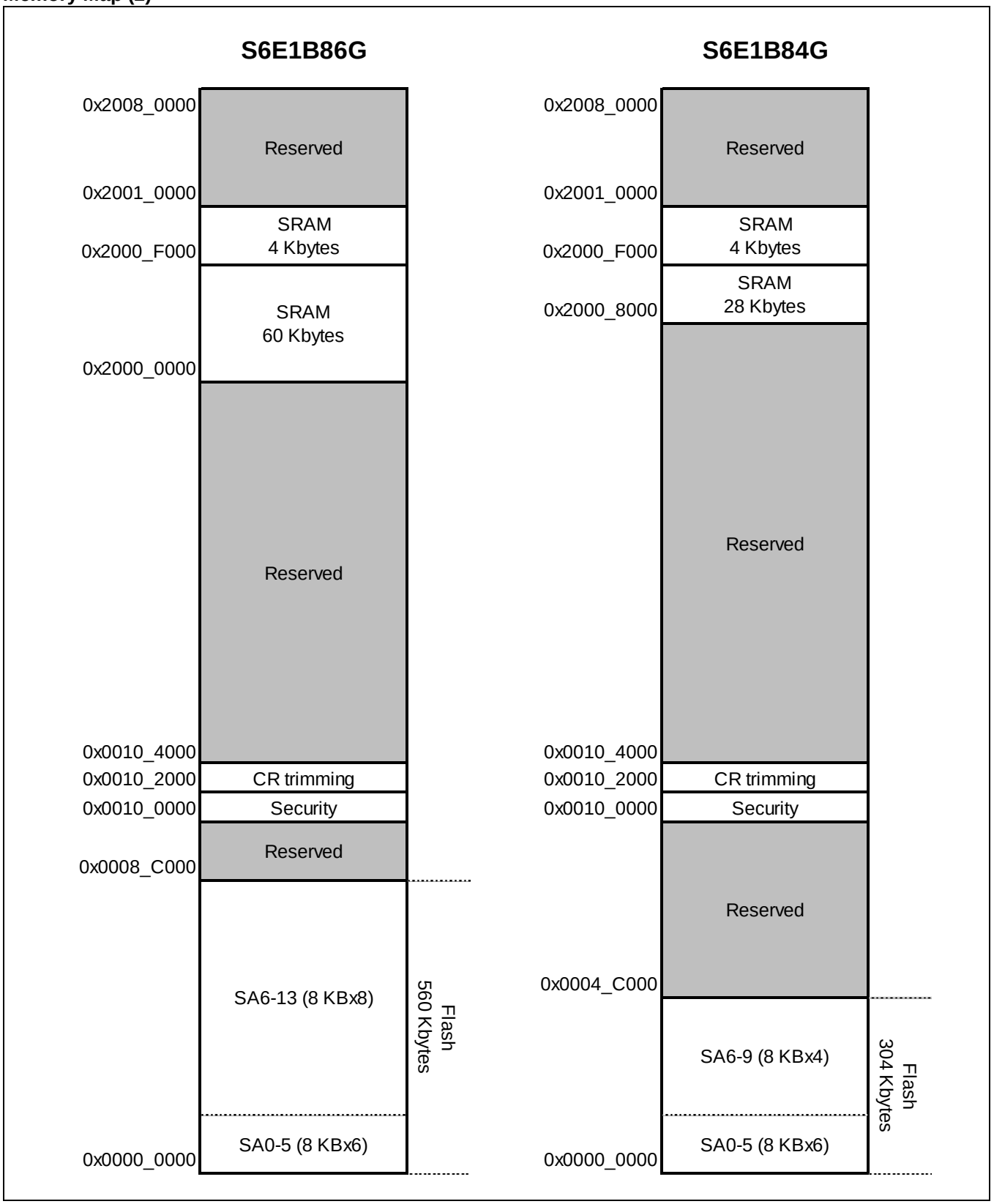
Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

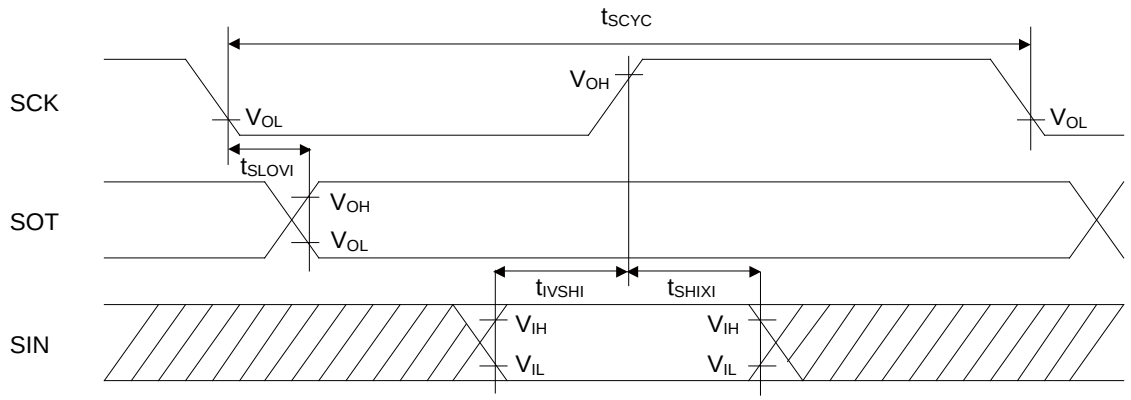
8. Block Diagram



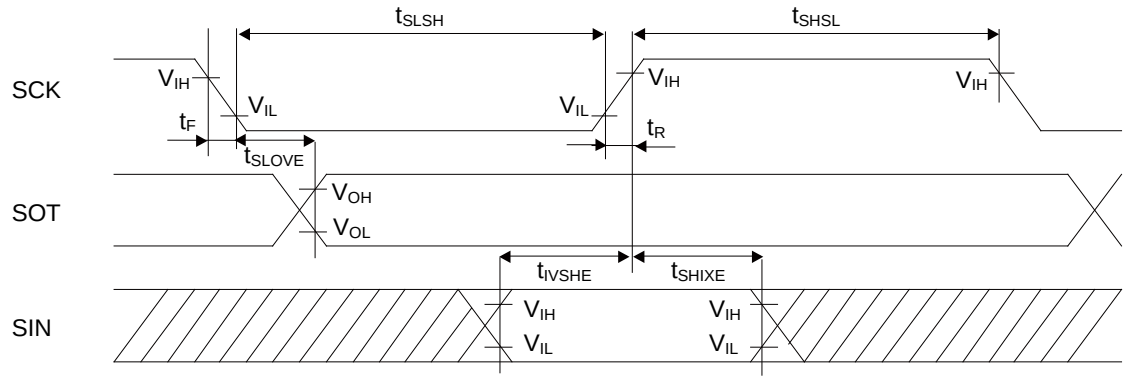
Memory Map (2)



*: See "S6E1B8 Series Flash Programming Manual" to check details of the Flash memory.



Master mode



Slave mode

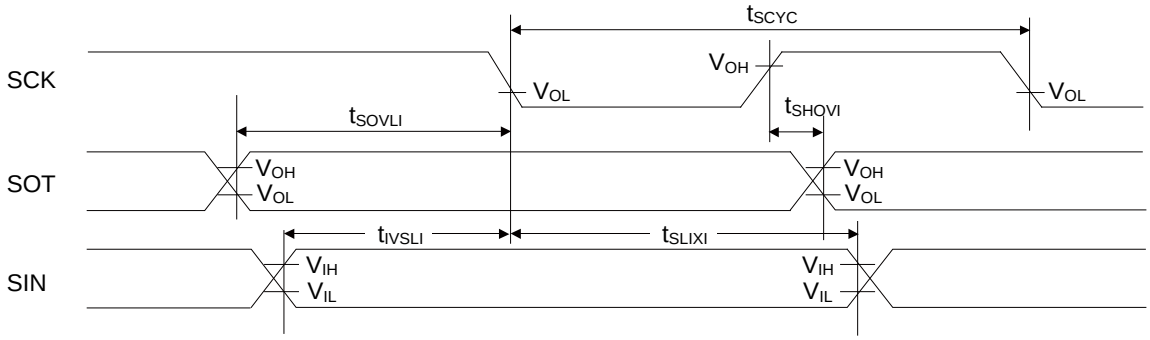
SPI (SPI=1, SCINV=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

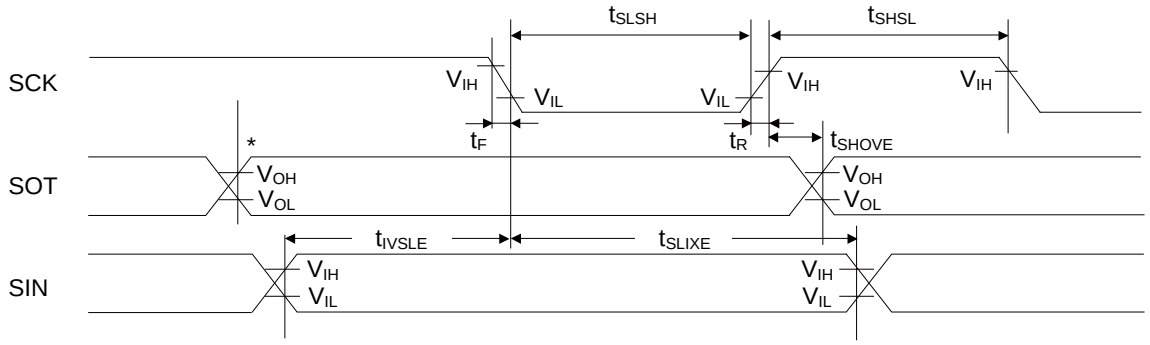
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		60	-	50	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} +10	-	t_{CYCP} +10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



Master mode



Slave mode

*: Changes when writing to TDR register

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

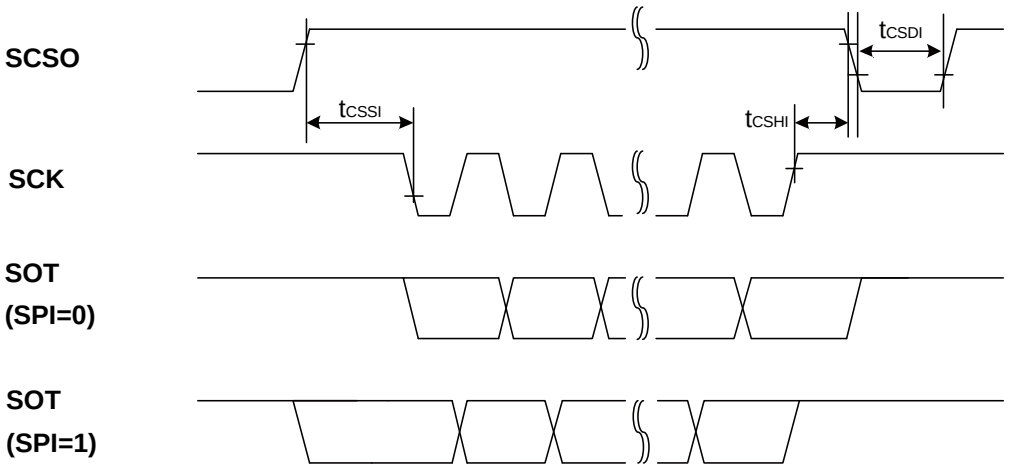
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

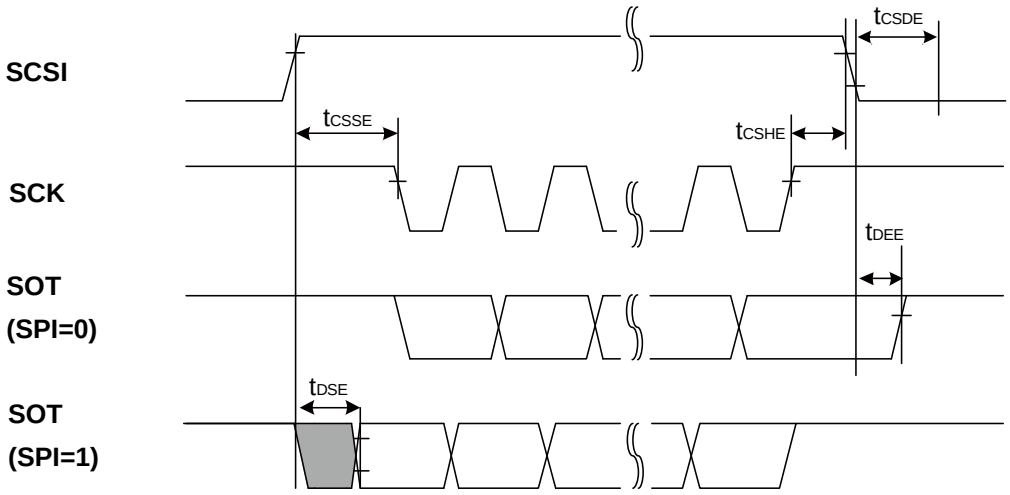
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

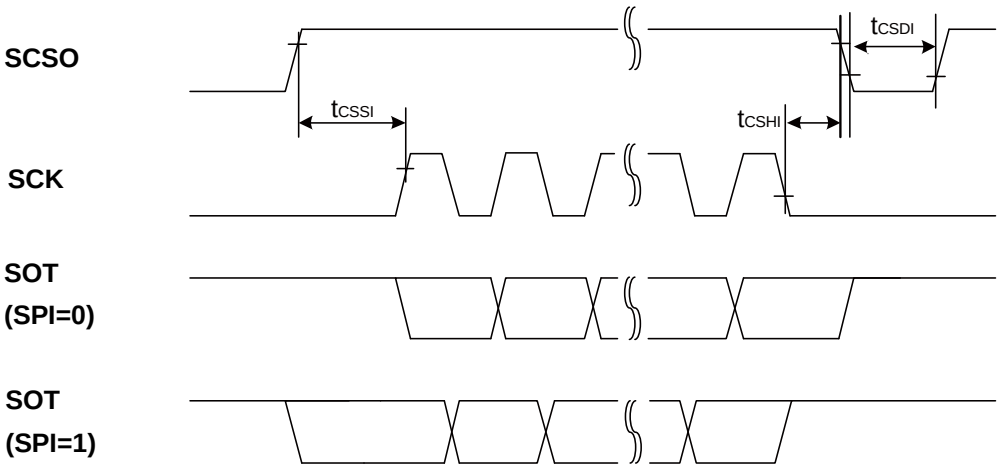
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

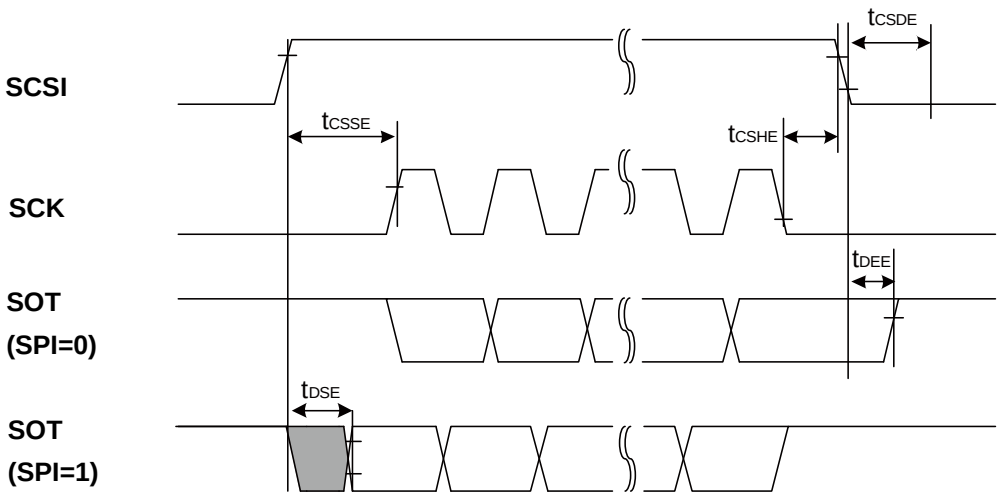
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode

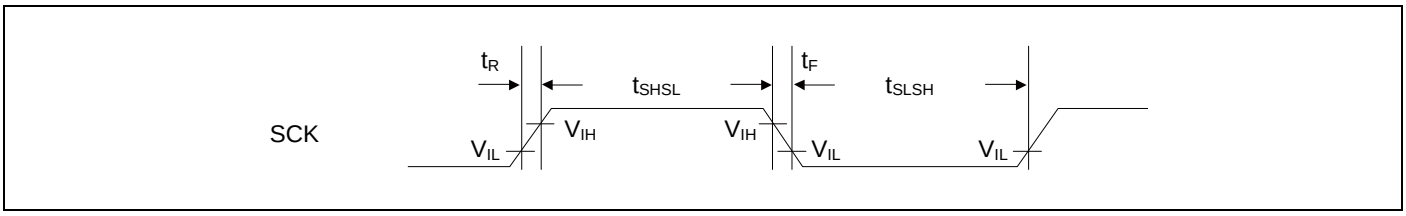


Slave mode

UART external clock input (EXT=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L=30 pF	t_{CYCP} +10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} +10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



11.4.13 Smart Card Interface Characteristics

(V_{CC}=1.65 V to 3.3 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t_R	ICx_VCC, ICx_RST, ICx_CLK, ICx_DATA	C_L=30 pF	4	20	ns	
Output falling time	t_F			4	20	ns	
Output clock frequency	f_{CLK}	ICx_CLK		-	20	MHz	
Duty cycle	Δ			45%	55%		

■External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx_CIN pin when it's used as smart card reader function.

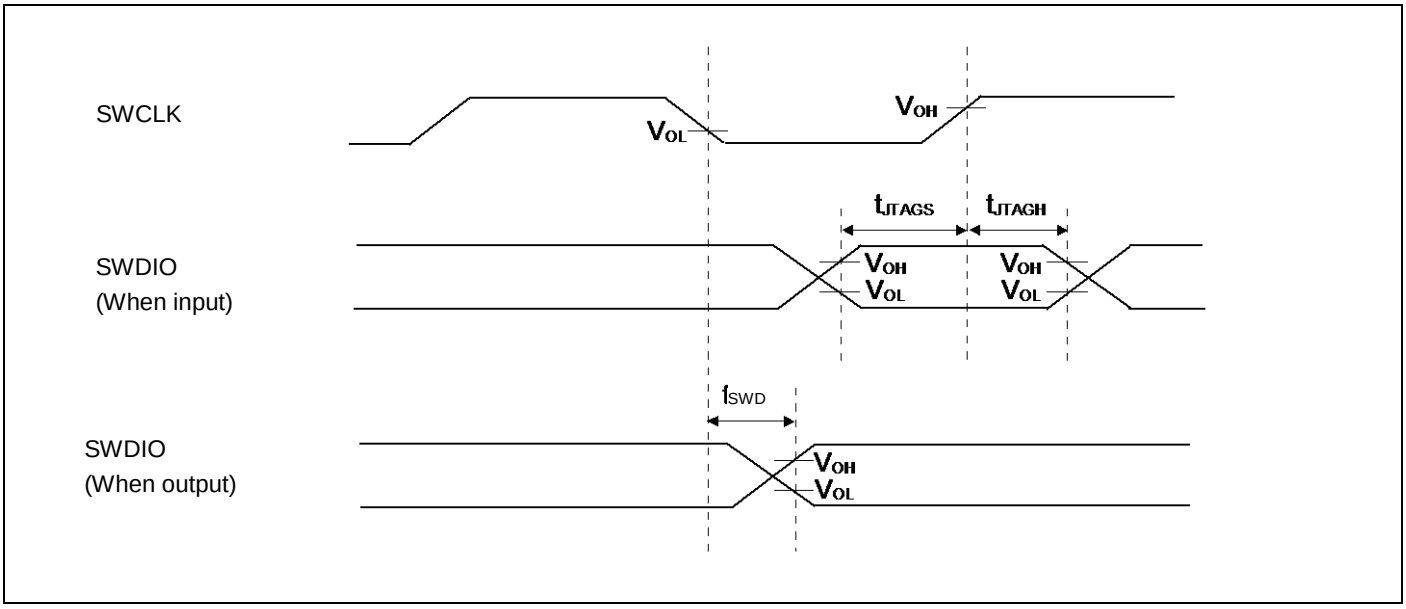
11.4.14 SW-DP Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- *External load capacitance C_L=30 pF*



11.5 12-bit A/D Converter

Electrical Characteristics of A/D Converter (Preliminary Values)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time *1	-	-	2.0	-	-	µs	AV_{CC} ≥ 2.7 V
			4.0	-	-		1.8 ≤ AV_{CC} < 2.7 V
			10	-	-		1.65 ≤ AV_{CC} < 1.8 V
Sampling time *2	t_S	-	0.6	-	10	µs	AV_{CC} ≥ 2.7 V
			1.2	-			1.8 ≤ AV_{CC} < 2.7 V
			3.0	-			1.65 ≤ AV_{CC} < 1.8 V
Compare clock cycle *3	t_{CCK}	-	100	-	1000	ns	AV_{CC} ≥ 2.7 V
			200	-			1.8 ≤ AV_{CC} < 2.7 V
			500	-			1.65 ≤ AV_{CC} < 1.8 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistance	R_{AIN}	-	-	-	2.2	kΩ	AV_{CC} ≥ 2.7 V
					5.5		1.8 ≤ AV_{CC} < 2.7 V
					10.5		1.65 ≤ AV_{CC} < 1.8 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	AVCC ≥ 2.7V
			AV_{CC}				AVCC < 2.7V

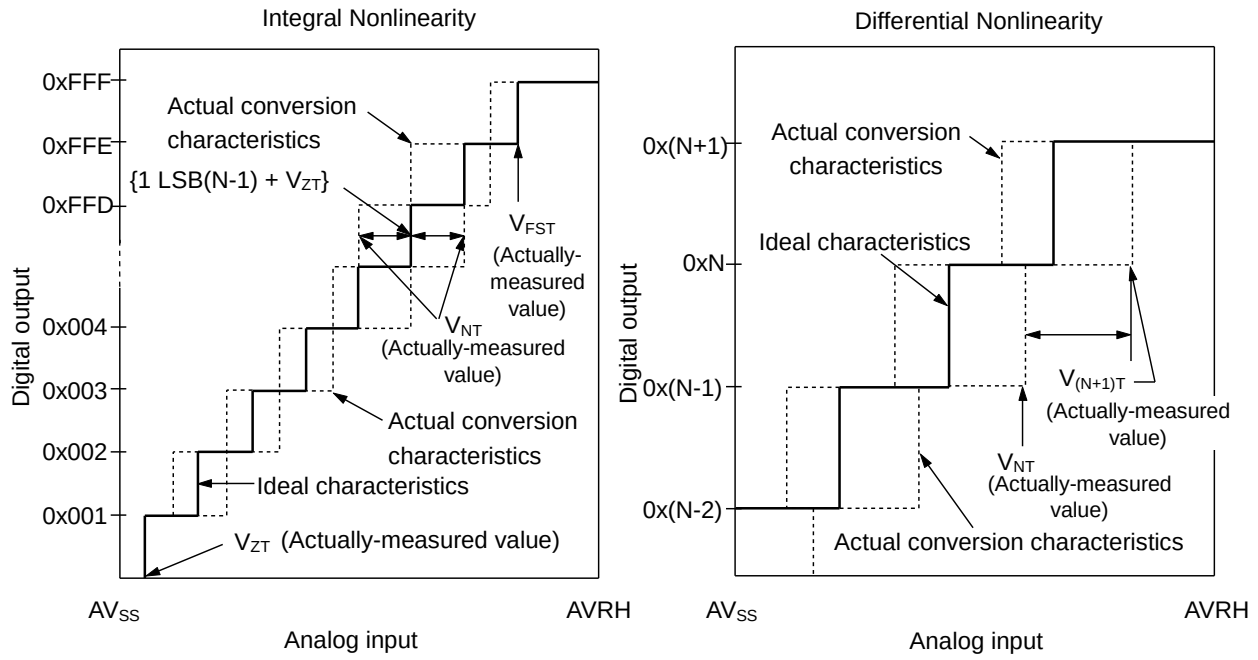
*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).
The minimum conversion time is computed according to the following conditions:
AV_{CC} ≥ 2.7 V sampling time=0.6 µs, compare time=1.4 µs
1.8 ≤ AV_{CC} < 2.7 V sampling time=1.2 µs, compare time=2.8 µs
1.65 ≤ AV_{CC} < 1.8 V sampling time=3.0 µs, compare time=7.0 µs
Ensure that the conversion time satisfies the specifications of the sampling time (t_S) and compare clock cycle (t_{CCK}).
For details of the settings of the sampling time and compare clock cycle, refer to "Chapter: A/D Converter" in "FM0+ Family Peripheral Manual Analog Macro Part".
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see "8. Block Diagram".
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: The required sampling time varies according to the external impedance.
Set a sampling time that satisfies (Equation 1).

*3: The compare time (t_C) is the result of (Equation 2).

Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

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