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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex® -M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86ehagf20000

1. Product Lineup

Memory Size

Product Name		S6E1B84E/F/G	S6E1B86E/F/G
On-chip Flash memory	Upper Bank	256 Kbytes	512 Kbytes
	Lower Bank	48 Kbytes	48 Kbytes
On-chip SRAM		32 Kbytes	64 Kbytes

Function

Product Name			S6E1B84E0A S6E1B86E0A S6E1B84EHA S6E1B86EHA	S6E1B84F0A S6E1B86F0A S6E1B84FHA S6E1B86FHA	S6E1B84G0A S6E1B86G0A S6E1B84GHA S6E1B86GHA		
Pin count			80		100	120	
CPU			Cortex-M0+				
Frequency			40.8 MHz				
Power supply voltage range			1.65 V to 3.6 V				
USB 2.0 (Device/Host)			1 unit				
DSTC			64ch				
Multi-function Serial Interface (UART/CSIO (SPI)/I ² C/I ² S)			8ch (Max) with 128 bytes FIFO I ² S: ch.5, ch.6				
Base Timer (PWC/Reload timer/PWM/PPG)			8ch (Max)				
LCD controller			20SEG x 8COM(Max) / 24SEG x 4COM(Max)	32SEG x 8COM(Max) / 36SEG x 4COM(Max)	40SEG x 8COM(Max) / 44SEG x 4COM(Max)		
Multi-function Timer	A/D activation compare	6ch	1 unit				
	Input capture	4ch					
	Free-run timer	3ch					
	Output compare	6ch					
	Waveform generator	3ch					
	PPG	3ch					
Dual Timer			1 unit				
HDMI-CEC/ Remote Control Receiver			2ch (max)				
Smart Card Interface			2ch (max)				
Real-time Clock			1 unit (with battery power)				
Watch Counter			1 unit				
CRC Accelerator			Yes				
Watchdog timer			1ch (SW) + 1ch (HW)				
External Interrupt			24 pins (Max), NMI × 1				
I/O port			65 pins (Max)	82 pins (Max)	102 pins (Max)		
12-bit A/D converter			16ch (1 unit)	23ch (1 unit)	24ch (1 unit)		
CSV (Clock Supervisor)			Yes				
LVD (Low-voltage Detection)			2ch				
Built-in CR	High-speed		4 MHz				
	Low-speed		100 kHz				
Debug Function			SW-DP				
Unique ID			Yes				
AES Calculator			-	Yes ^{*1}	-	Yes ^{*1}	

*1: AES Calculator is built in following products.

S6E1B86GHA, S6E1B84GHA, S6E1B86FHA, S6E1B84FHA, S6E1B86EHA, S6E1B84EHA

Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
See "11 Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

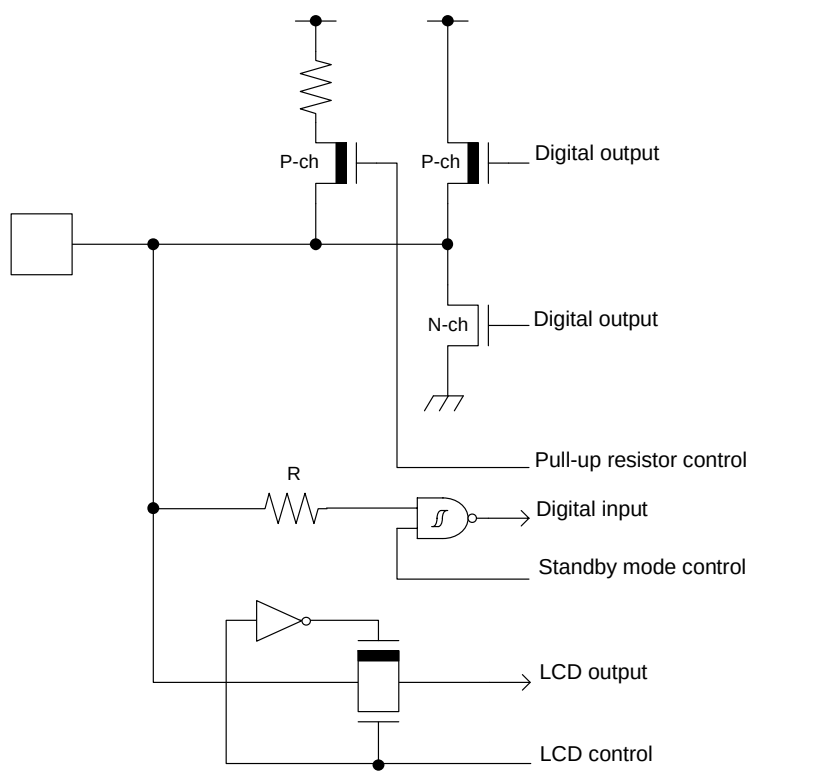
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
76	66	56	P1A	P	V
			SIN4_1		
			IC01_1		
			INT05_1		
			AN10		
			SEG17		
77	67	57	P1B	P	V
			SOT4_1		
			IC02_1		
			INT20_2		
			AN11		
			SEG16		
78	68	-	P1C	P	V
			SCK4_1		
			IC03_1		
			INT21_2		
			AN12		
			SEG15		
79	69	-	P1D	P	V
			CTS4_1		
			DTTIOX_1		
			INT22_2		
			AN13		
			SEG14		
80	70	-	P1E	H	L
			RTS4_1		
			FRCK0_1		
			ADTG_5		
			INT23_2		
			AN14		
81	-	-	P28	F	I
			RTO05_1		
			TIOB6_2		
			ADTG_4		
82	-	-	P27	G	L
			RTO04_1		
			TIOA6_2		
			INT02_2		
			AN15		
83	-	-	P26	F	I
			SCK2_1		
			RTO03_1		
84	-	-	P25	F	I
			SOT2_1		
			RTO02_1		
85	-	-	P24	F	J
			SIN2_1		
			RTO01_1		
			INT17_1		
86	71	58	P23	P	K
			SCK0_0		
			TIOA7_1		
			RTO00_1		
			AN16		
			SEG13		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
100	85	-	P08	P	V
			TIOA0_2		
			CTS4_2		
			INT16_0		
			AN23		
			SEG06		
101	86	-	P09	L	S
			TIOB0_2		
			RTS4_2		
			INT17_0		
			SEG05		
102	87	67	P0A	I	O
			SIN4_0		
			INT00_2		
			WKUP5		
			IC0_CIN_0		
			UHCONX0		
			CEC0_1		
103	88	68	P0B	K	Q
			INT18_0		
			UDM0		
104	89	69	P0C	K	Q
			INT19_0		
			UDP0		
105	90	70	P0D	L	S
			RTS4_0		
			TIOA3_2		
			INT20_0		
			SEG04		
106	91	71	IC0_VPEN_0	L	S
			P0E		
			CTS4_0		
			TIOB3_2		
			INT21_0		
			SEG03		
107	92	72	IC0_VCC_0	I	G
			P0F		
			CROUT_1		
			RTCCO_0		
			SUBOUT_0		
			MI2SMCK5_0		
			NMIX		
			WKUP0		
			IC0_CLK_0		
108	-	-	SCK4_0	F	J
			P68		
			SCK3_0		
			TIOB7_2		
109	-	-	INT12_2	F	J
			P67		
			SOT3_0		
			TIOA7_2		
110	-	-	INT22_0	F	J
			P66		
			SIN3_0		
			INT11_2		

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	11	-	-
	SIN7_1		48	43	33
	SIN7_2		117	97	77
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin.	12	-	-
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I ² C pin (operation mode 4).	49	44	34
	SOT7_2 (SDA7_2)		118	98	78
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin.	13	-	-
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I ² C pin (operation mode 4).	50	45	35
	SCK7_2 (SCL7_2)		119	99	79
	SCS70_1	Multi-function serial interface ch.7 serial chip select 0 input/output pin.	47	42	32
	SCS71_1	Multi-function serial interface ch.7 serial chip select 1 input/output pin.	51	-	-
	SCS72_1	Multi-function serial interface ch.7 serial chip select 2 input/output pin.	52	-	-
Smart Card Interface 0	IC0_VCC_0	Smart card ch.0 power enable output pin	106	91	71
	IC0_VCC_1		33	28	-
	IC0_VPEN_0	Smart card ch.0 programming output pin	105	90	70
	IC0_VPEN_1		34	29	-
	IC0_RST_0	Smart card ch.0 reset output pin	114	94	74
	IC0_RST_1		35	30	-
	IC0_CIN_0	Smart card ch.0 insert detection input pin	102	87	67
	IC0_CIN_1		37	32	22
	IC0_CLK_0	Smart card ch.0 serial interface clock output pin	107	92	72
	IC0_CLK_1		32	27	-
	IC0_DATA_0	Smart card ch.0 serial interface data input/output pin	113	93	73
	IC0_DATA_1		36	31	21
Smart Card Interface 1	IC1_VCC_0	Smart card ch.1 power enable output pin	28	23	18
	IC1_VCC_1		63	53	43
	IC1_VPEN_0	Smart card ch.1 programming output pin	27	22	17
	IC1_VPEN_1		64	54	44
	IC1_RST_0	Smart card ch.1 reset output pin	26	21	16
	IC1_RST_1		65	55	45
	IC1_CIN_0	Smart card ch.1 insert detection input pin	24	19	14
	IC1_CIN_1		67	57	47
	IC1_CLK_0	Smart card ch.1 serial interface clock output pin	29	24	19
	IC1_CLK_1		62	52	42
	IC1_DATA_0	Smart card ch.1 serial interface data input/output pin	25	20	15
	IC1_DATA_1		66	56	46
USB	UDM0	USB device/host D – pin	103	88	68
	UDP0	USB device/host D + pin	104	89	69
	UHCONX0	USB external pull-up control pin	102	87	67

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	REGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

*: PE0 is an open drain pin, cannot output high.

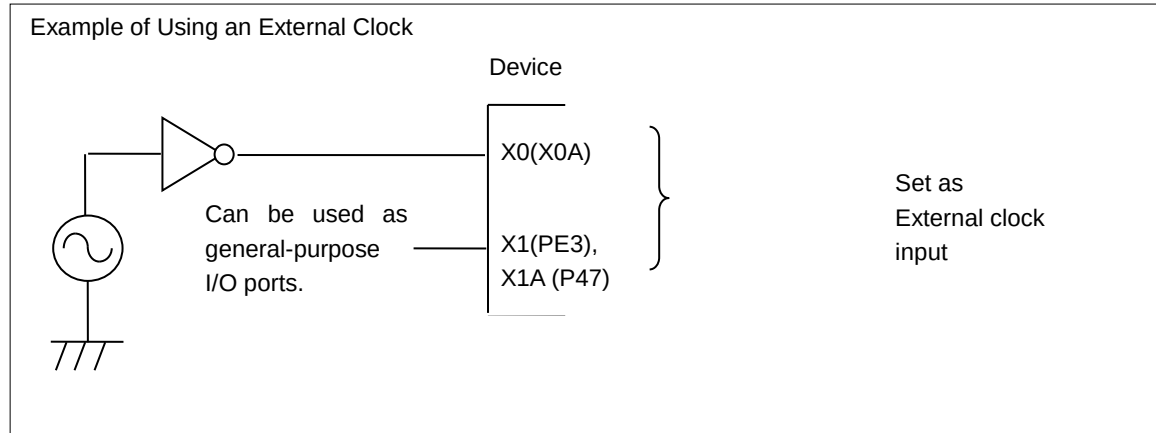
Type	Circuit	Remarks
L	 The circuit diagram for Type L shows a central pin connected to several internal components: - A P-channel MOSFET (P-ch) acting as a digital output, with its gate connected to the pin and its source to ground. - An N-channel MOSFET (N-ch) acting as a digital output, with its gate connected to the pin and its source to ground. - A pull-up resistor connected to the pin and to a pull-up resistor control signal. - A resistor R connected to the pin and to a digital input. - A Schmitt trigger connected to the pin and to a standby mode control signal. - An inverter connected to the pin and to an LCD output. - An LCD control signal connected to the pin.	• CMOS level output • CMOS level hysteresis input • With input control • 5 V tolerant • LCD segment output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • Available to control of PZR registers. • When this pin is used as an I²C pin, the digital output P-ch transistor is always off

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Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.

Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.



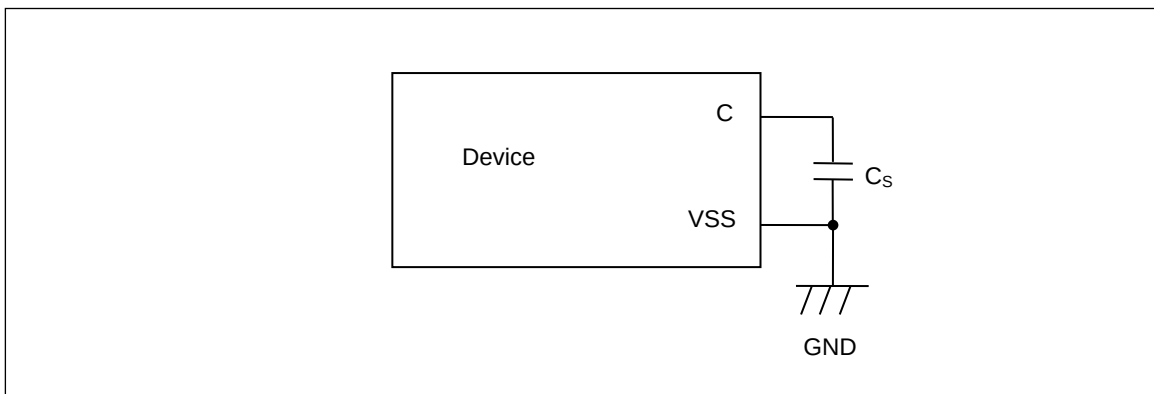
Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_s) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.

A smoothing capacitor of about 4.7 μ F would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
R	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Output maintains previous state / Internal input fixed at 0			Output maintains previous state / Internal input fixed at 0
	GPIO selected									
S	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Output Maintain previous state / Internal input fixed at 0			
	GPIO selected							Output Maintain previous state / Internal input fixed at 0		

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
W	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
X	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Output Maintain previous state / Internal input fixed at 0			
	GPIO selected									

*1: Oscillation stops in Sub timer mode, Low-speed CR timer mode, Stop mode, RTC mode.

*2: Oscillation stops in Stop mode.

11.2 Recommended Operating Conditions

 (V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V _{CC}	-	1.65 * ^b	3.6	V	*1
			2.2	3.6	V	*2
			3.0	3.6	V	*3
LCD input voltage	V _{VV4}	-	2.2	V _{CC}	V	No booster used
		-	2.2	4.7	V	Booster is used
LCD External Capacitor *6	C _f , C _{VV1} , C _{VV2} , C _{VV3} , C _{VV4}	-	0.5	1.3	μF	Booster is used
Sub Oscillation frequency *7	F _{in}	-	-	-	kHz	Typical is 32.768 kHz
Analog power supply voltage	AV _{CC}	-	1.65	3.6	V	AV _{CC} =V _{CC}
Analog reference voltage	AVRH	-	2.7	AV _{CC}	V	AV _{CC} ≥ 2.7 V
		-	AV _{CC}	AV _{CC}	V	AV _{CC} < 2.7 V
	AVRL	-	AV _{SS}	AV _{SS}	V	
Smoothing capacitor	C _S	-	1	10	μF	For regulator* ⁴
Operating temperature	T _A	-	- 40	+ 105	°C	

*1: When LCD Controller is not used.

*2: When LCD Controller is used.

*3: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

*4: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*5: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

*6: LCD external capacitor between VVx to VSS, and between C0 and C1.

*7: If a Booster is used, Sub OSC should provide operation clock at typically 32.768 kHz.

<WARNING>

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
2. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
3. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
4. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I _{CCVBAT} (VBAT)	RTC operation	T _A =25°C V _{CC} =3.0V 32 kHz Crystal oscillation	0.9	TBD	μA	*1
			T _A =25°C V _{CC} =1.65 V 32 kHz Crystal oscillation	0.8	TBD	μA	*1
			T _A =105°C V _{CC} =3.6V 32 kHz Crystal oscillation	-	TBD	μA	*1
		RTC stop	T _A =25°C V _{CC} =3.0V	0.05	TBD	μA	*1
			T _A =25°C V _{CC} =1.65 V	0.02	TBD	μA	*1
			T _A =105°C V _{CC} =3.6V	-	TBD	μA	*1

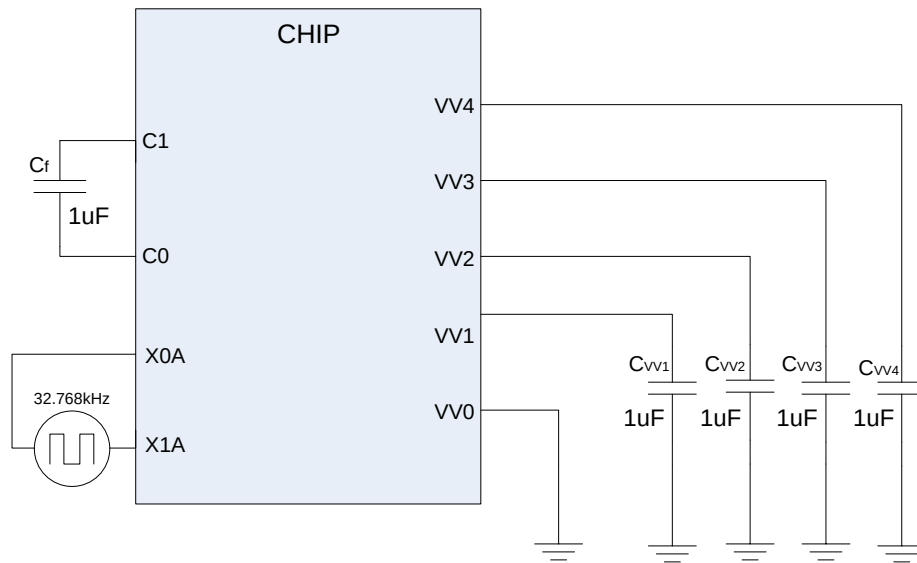
*1: All ports are fixed.

11.3.3.2 LCD Characteristic With Booster

Recommended LCD Operation Conditions With Booster

($V_{CC} = AV_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Voltage correlation	V_{CC-VV1}	VCC,VV1	0.35	-	-	V	VCC-VV1 must be larger than 0.35 V
External input tolerant voltage	V_{tole}	VV1,VV2,VV3,VV4,C0,C1	0	-	5.5	V	
Operating frequency	f_{IN}	-	-	32.768	-	kHz	Crystal oscillator
External Capacitor	$C_f, C_{VV1}, C_{VV2}, C_{VV3}, C_{VV4}$	VV1,VV2,VV3,VV4,C0,C1	0.5	1	1.3	μF	
LCD capacitor	$C_{LCD/1COM}$	-	-	1.25	8	μF	
Frame period	t_{FRAME}	-	1/150	-	1/30	s	

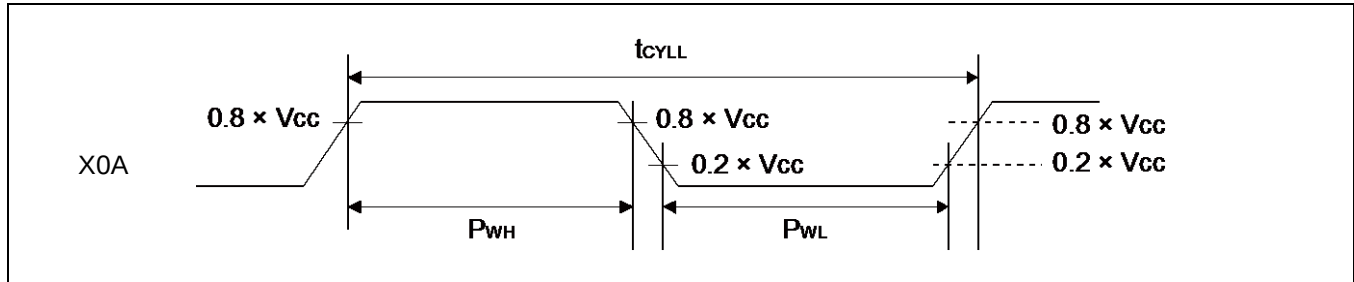


LCD Booster 1/4 mode (BIAS[1:0]=2'b10)

11.4.2 Sub Clock Input Characteristics
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C})$

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected*
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	μs	When the external clock is used
Input clock pulse width	-		$P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}$	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



SPI (SPI=1, SCINV=1)
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C})$

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4\ t_{CYCP}$	-	$4\ t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		60	-	50	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2\ t_{CYCP} - 30$	-	$2\ t_{CYCP} - 30$	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2\ t_{CYCP} - 10$	-	$2\ t_{CYCP} - 10$	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above AC characteristics are for clock synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.
For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- External load capacitance $C_L=30\text{ pF}$

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C})$

Parameter	Symbol	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- t_{CYCP} indicates the APB bus clock cycle time.
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.
For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- When the external load capacitance $C_L=30\text{ pF}$.

11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

 (T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed ^{*1}	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	t _{LVDW}	-	-	-	8160× t _{CYCP} ^{*2}	μs	
LVD detection delay time	t _{LVDL}	-	-	-	200	μs	

*1: The value of low voltage detection reset is always fixed.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

11.8 Flash Memory Write/Erase Characteristics

 (V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ*	Max*		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	μs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

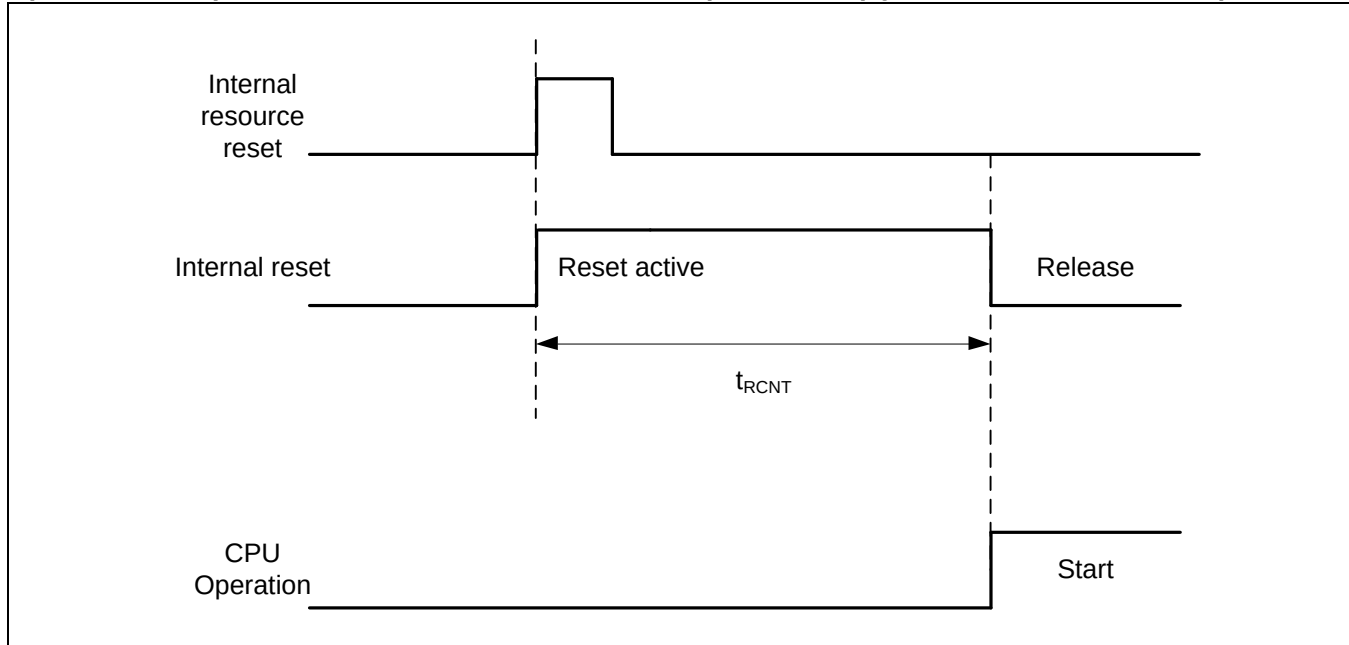
*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time (Target Value)

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes. See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".
- The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low-voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

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