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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86ehagv20000

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
49	44	34	P4C TIOB2_0 SOT7_1 CEC0_0 INT12_0 SEG29	L	R
50	45	35	P4D TIOB3_0 SCK7_1 INT13_0 WKUP6 SEG28	L	T
51	-	-	P70 TIOA4_2 SCS71_1	F	I
52	-	-	P71 TIOB4_2 SCS72_1 INT13_2	F	J
53	-	-	P72 SIN2_0 TIOA6_0 INT14_2	F	J
54	-	-	P73 SOT2_0 TIOB6_0 INT15_2	F	J
55	-	-	P74 SCK2_0	F	I
56	46	36	PE0 MD1	C	D
57	47	37	MD0	J	M
58	48	38	PE2 X0	A	A
59	49	39	PE3 X1	A	B
60	50	40	VSS	-	-
61	51	41	VCC	-	-
62	52	42	P10 IC1_CLK_1 CTS1_1 AN00 SEG27	P	K
63	53	43	P11 IC1_VCC_1 SIN1_1 FRCK0_2 INT02_1 WKUP1 AN01 SEG26	P	W

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
87	72	59	P22 SOT0_0 TIOB7_1 AN17 SEG12	P	K
88	73	60	P21 SIN0_0 INT06_1 WKUP2 AN18 SEG11	P	W
89	74	-	P20 INT05_0 CROUT_0 AN19 SEG10	P	V
90	75	-	VSS	-	-
91	76	-	VCC	-	-
92	77	61	P00 SOT3_2 INT14_1	I	J
93	78	62	P01 SWCLK	I	H
94	79	63	P02 SIN3_2 TIOB5_0	I	I
95	80	64	P03 SWDIO	I	H
96	81	65	P04 SCK3_2 INT06_2	I	J
97	82	-	P05 TIOA5_2 SIN4_2 INT00_1 WKUP10 AN20 SEG09	P	W
98	83	-	P06 TIOB5_2 SOT4_2 INT01_1 AN21 SEG08	P	V
99	84	66	P07 SCK4_2 ADTG_0 INT23_1 AN22 SEG07 SOT4_0	P	V

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
111	-	-	P65 SCK5_1 TIOB7_0 INT23_0	F	J
112	-	-	P64 SOT5_1 TIOA7_0 INT10_2	F	J
113	93	73	P63 MI2SWS5_0 INT03_0 SEG02 TIOB6_1 IC0_DATA_0	L	S
	-	-	SIN5_1		
114	94	74	P62 SCK5_0 MI2SCK5_0 ADTG_3 INT07_1 SEG01 TIOA6_1 IC0_RST_0	L	S
115	95	75	P61 SOT5_0 MI2SDO5_0 TIOB2_2 DTTI0X_2 SEG00	L	P
116	96	76	P60 SIN5_0 MI2SDI5_0 TIOA2_2 CEC1_0 INT15_1 WKUP3 IGTRG0_1	I	O
117	97	77	P80 SIN7_2 INT20_1 C0	O	J
118	98	78	P81 SOT7_2 INT11_0 C1	O	J
119	99	79	P82 SCK7_2	I	I
120	100	80	VSS	-	-

*: 5 V tolerant I/O

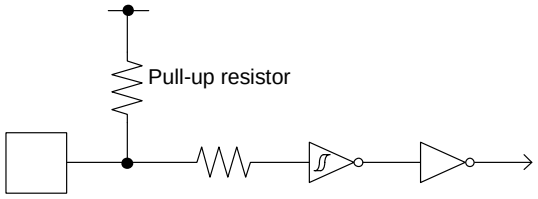
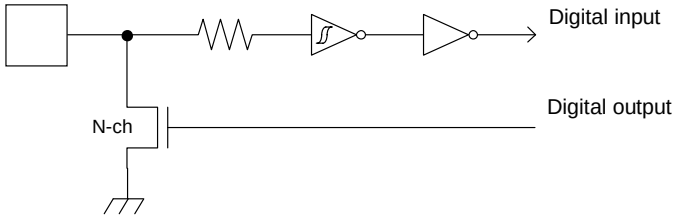
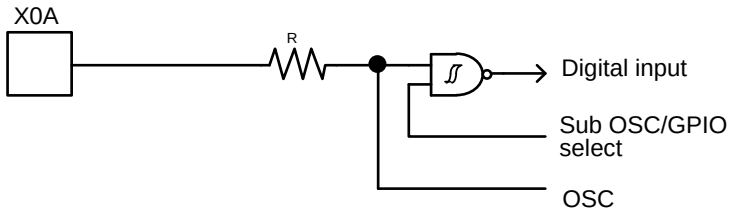
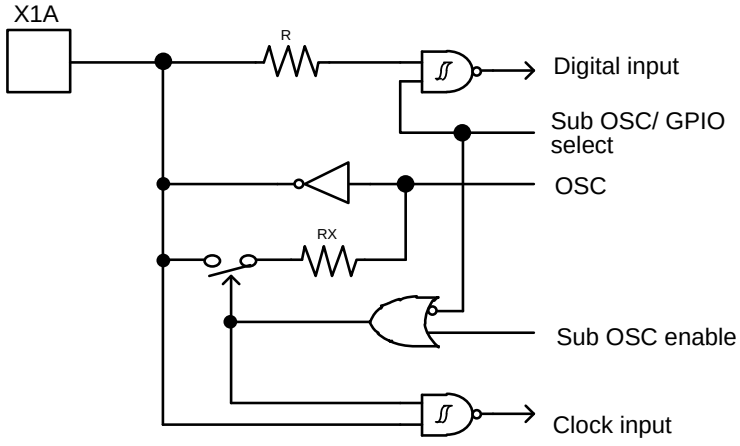
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2
	INT00_1		97	82	-
	INT00_2		102	87	67
	INT01_0	External interrupt request 01 input pin	3	3	3
	INT01_1		98	83	-
	INT02_0	External interrupt request 02 input pin	4	4	4
	INT02_1		63	53	43
	INT02_2		82	-	-
	INT03_0	External interrupt request 03 input pin	113	93	73
	INT03_1		66	56	46
	INT03_2		14	9	9
	INT04_0	External interrupt request 04 input pin	17	12	12
	INT04_1		69	59	49
	INT04_2		15	10	10
	INT05_0	External interrupt request 05 input pin	89	74	-
	INT05_1		76	66	56
	INT05_2		16	11	11
	INT06_0	External interrupt request 06 input pin	23	18	13
	INT06_1		88	73	60
	INT06_2		96	81	65
	INT07_0	External interrupt request 07 input pin	24	19	14
	INT07_1		114	94	74
	INT07_2		5	5	5
	INT08_0	External interrupt request 08 input pin	34	29	-
	INT08_1		19	14	-
	INT08_2		8	8	8
	INT09_0	External interrupt request 09 input pin	35	30	-
	INT09_1		20	15	-
	INT10_0	External interrupt request 10 input pin	36	31	21
	INT10_1		21	16	-
	INT10_2		112	-	-
	INT11_0	External interrupt request 11 input pin	118	98	78
	INT11_1		22	17	-
	INT11_2		110	-	-
	INT12_0	External interrupt request 12 input pin	49	44	34
	INT12_1		32	27	-
	INT12_2		108	-	-
	INT13_0	External interrupt request 13 input pin	50	45	35
	INT13_1		33	28	-
	INT13_2		52	-	-
	INT14_0	External interrupt request 14 input pin	67	57	47
	INT14_1		92	77	61
	INT14_2		53	-	-

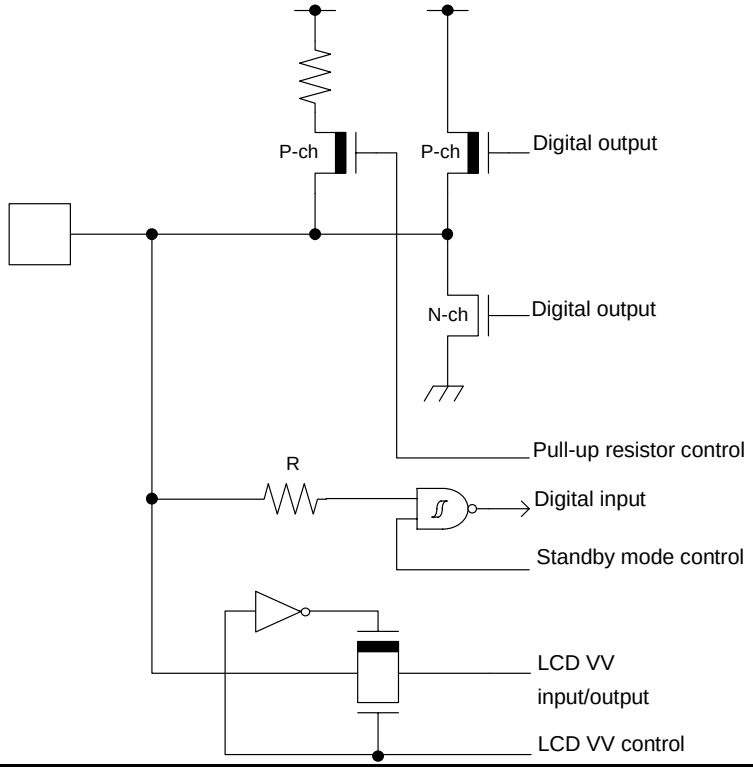
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
GPIO	P10	General-purpose I/O port 1	62	52	42
	P11		63	53	43
	P12		64	54	44
	P13		65	55	45
	P14		66	56	46
	P15		67	57	47
	P16		68	58	48
	P17		69	59	49
	P18		74	64	54
	P19		75	65	55
	P1A		76	66	56
	P1B		77	67	57
	P1C		78	68	-
	P1D		79	69	-
	P1E		80	70	-
	P20	General-purpose I/O port 2	89	74	-
	P21		88	73	60
	P22		87	72	59
	P23		86	71	58
	P24		85	-	-
	P25		84	-	-
	P26		83	-	-
	P27		82	-	-
	P28		81	-	-
	P30	General-purpose I/O port 3	14	9	9
	P31		15	10	10
	P32		16	11	11
	P33		17	12	12
	P34		18	13	-
	P35		19	14	-
	P36		20	15	-
	P37		21	16	-
	P38		22	17	-
	P39		23	18	13
	P3A		24	19	14
	P3B		25	20	15
	P3C		26	21	16
	P3D		27	22	17
	P3E		28	23	18
	P3F		29	24	19

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
LCD Controller	SEG17		76	66	56
	SEG18	LCD controller segment output pin	75	65	55
	SEG19		74	64	54
	SEG20		69	59	49
	SEG21		68	58	48
	SEG22		67	57	47
	SEG23		66	56	46
	SEG24		65	55	45
	SEG25		64	54	44
	SEG26		63	53	43
	SEG27		62	52	42
	SEG28		50	45	35
	SEG29		49	44	34
	SEG30		48	43	33
	SEG31		47	42	32
	SEG32		37	32	22
	SEG33		36	31	21
	SEG34		29	24	19
	SEG35		28	23	18
	SEG36		27	22	17
	SEG37		19	14	-
	SEG38		8	8	8
	SEG39		7	7	7
	SEG40		17	12	12
	SEG41		16	11	11
	SEG42		15	10	10
	SEG43		14	9	9
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin	107	92	72
	WKUP1		63	53	43
	WKUP2		88	73	60
	WKUP3		116	96	76
	WKUP4		14	9	9
	WKUP5		102	87	67
	WKUP6		50	45	35
	WKUP7		48	43	33
	WKUP8		28	23	18
	WKUP9		8	8	8
	WKUP10		97	82	-
	WKUP11		20	15	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	REGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

*: PE0 is an open drain pin, cannot output high.

Type	Circuit	Remarks
B		CMOS level hysteresis input Pull-up resistor : Approximately 33 kΩ
C		Open drain output CMOS level hysteresis input
D		・CMOS level output ・ Please refer to the "VBAT domain" setting of IO in of the “Peripheral Manual main part (MN710-00001)".
E		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ・Oscillation feedback resistor : Approximately 12 MΩ When the GPIO is selected. ・CMOS level hysteresis input ・Please refer to the "VBAT domain" setting of IO in the “Peripheral Manual main part (MN710-00001)" .

Type	Circuit	Remarks
Q		・CMOS level output ・CMOS level hysteresis input ・With input control ・5 V tolerant ・LCD VV input/output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I_{CCHD} (VCC)	Deep standby Stop mode	RAM off	T_A=25°C V_{CC}=3.3 V	0.75	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	0.7	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
			RAM on	T_A=25°C V_{CC}=3.3 V	1.1	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.0	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
	I_{CCRD} (VCC)	Deep standby RTC mode	RAM off	T_A=25°C V_{CC}=3.3 V	1.7	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.6	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
			RAM on	T_A=25°C V_{CC}=3.3 V	1.9	TBD	µA	*1
				T_A=25°C V_{CC}=1.65 V	1.7	TBD	µA	*1
				T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1

*1: All ports are fixed. LVD off.

LVD Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	TBD	µA	For occurrence of reset
				0.13	TBD	µA	For occurrence of interrupt

Flash Memory Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	TBD	mA	

A/D converter Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	TBD	mA	
			At stop	0.13	TBD	µA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	TBD	mA	AVRH=3.6 V
			At stop	0.1	TBD	µA	

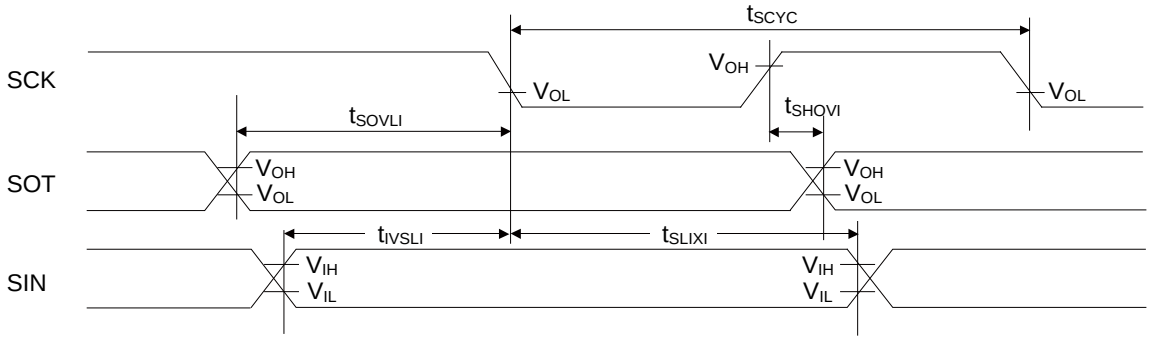
SPI (SPI=1, SCINV=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

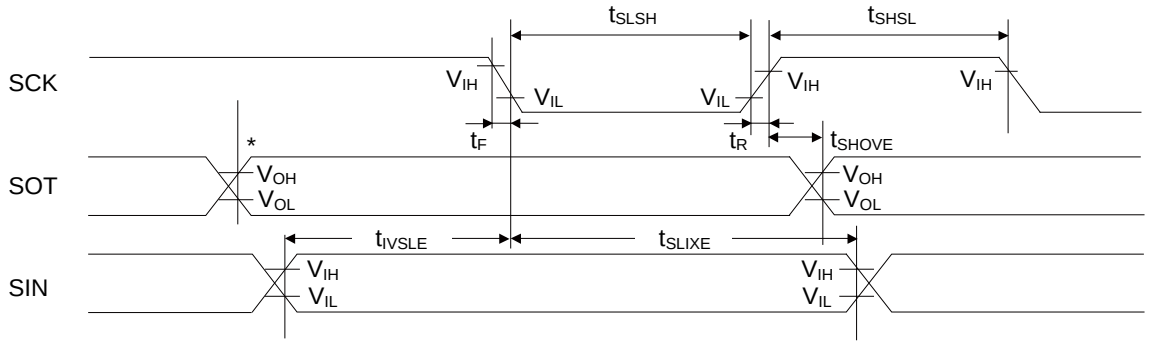
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		60	-	50	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} +10	-	t_{CYCP} +10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

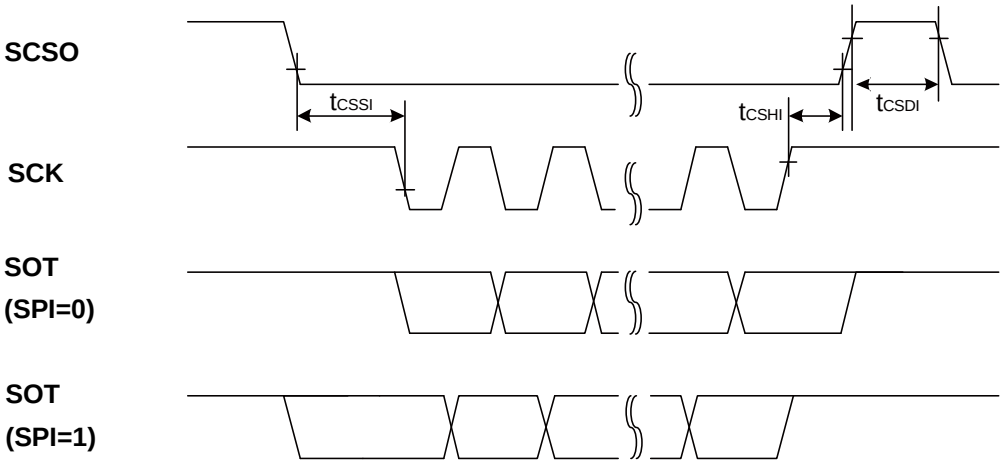


Master mode

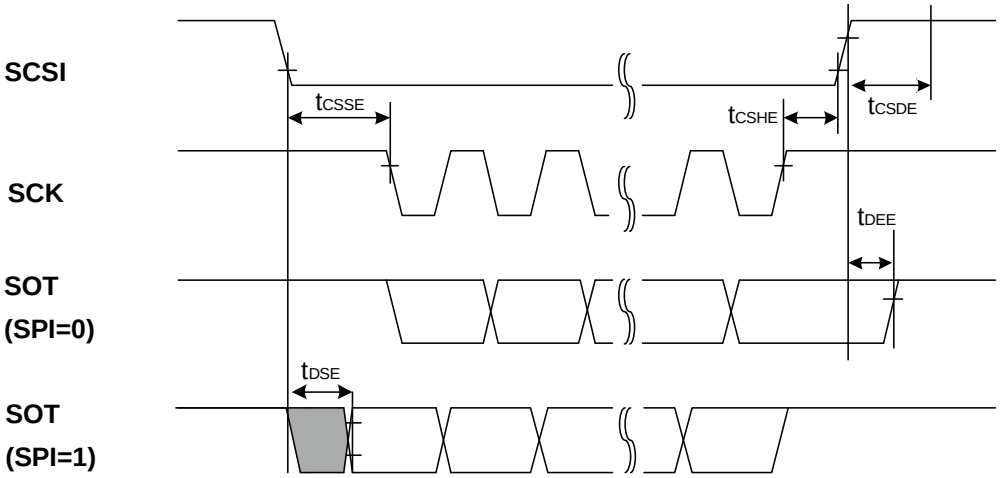


Slave mode

*: Changes when writing to TDR register



Master mode



Slave mode

11.4.11 I^2C Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

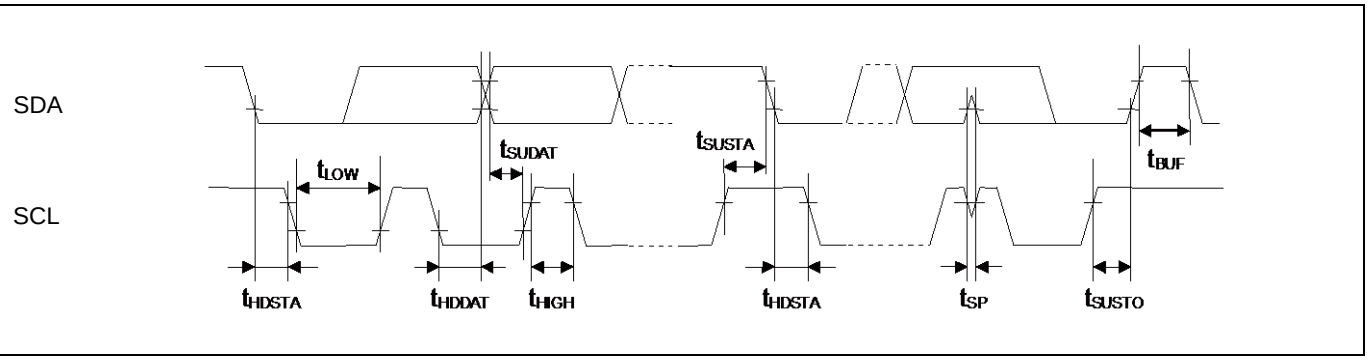
Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L=30 pF, R=(V_P/I_{OL})*1	0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R represents the pull-up resistance of the SCL and SDA lines, and C_L the load capacitance of the SCL and SDA lines. V_P represents the power supply voltage of the pull-up resistance, and I_{OL} the V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy at least the condition that the period during which the device is holding the SCL signal at L (t_{LOW}) does not extend.

*3: A Fast-mode I^2C bus device can be used in a Standard-mode I^2C bus system, provided that the condition of t_{SUDAT} ≥ 250 ns is fulfilled.

*4: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the I^2C is connected, see "8. Block Diagram".
To use Standard-mode, set the APB bus clock at 2 MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.

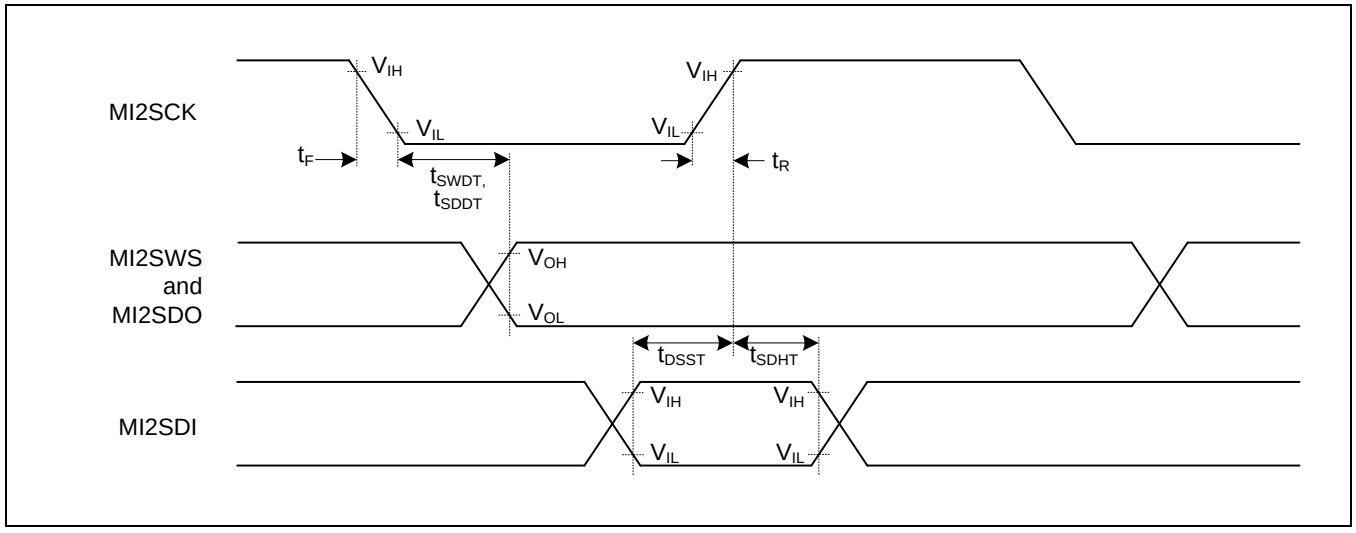


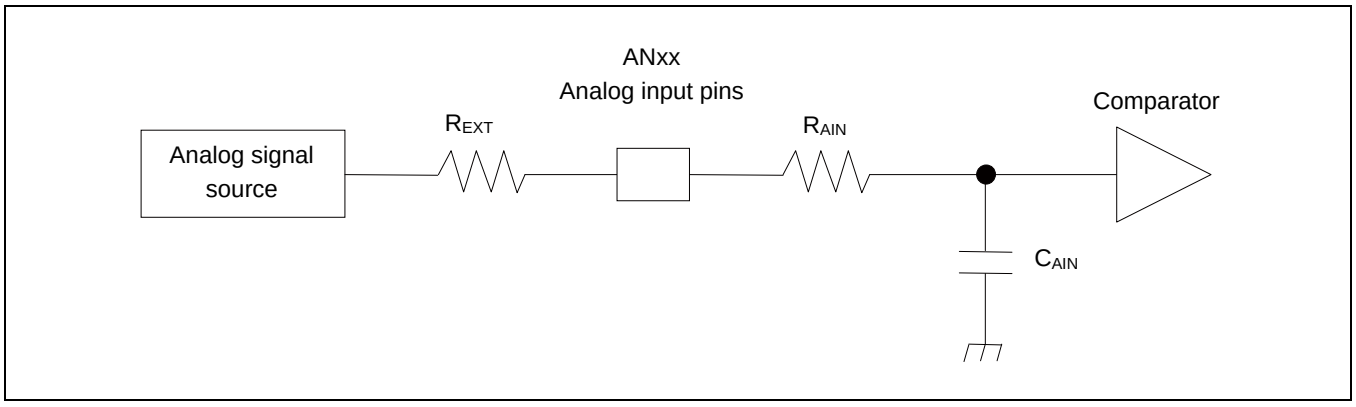
11.4.12 I²S Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency*1	f_{MI2SCK}	MI2SCKx	C_L=30 pF	-	6.144	-	6.144	MHz
I²S clock cycle time*1	t_{ICYC}	MI2SCKx		4 t_{CYCP}	-	4 t_{CYCP}	-	ns
I²S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t_{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t_{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t_{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t_{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	t_F	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	t_R	MI2SCKx		-	5	-	5	ns

*1: I²S clock should meet the multiple of PCLK (t_{ICYC}) and the frequency less than f_{MI2SCK} meantime. The detail information please refer to Chapter I²S of Communication Macro Part of Peripheral Manual.





(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D Converter = 2.2 kΩ with $2.7 \leq AV_{CC} \leq 3.6$ ch.1 to ch.14, ch.16 to ch.19
Input resistance of A/D Converter = 1.9 kΩ with $2.7 \leq AV_{CC} \leq 3.6$ ch.15
Input resistance of A/D Converter = 2.3 kΩ with $2.7 \leq AV_{CC} \leq 3.6$ ch.20 to ch.23
Input resistance of A/D Converter = 5.7 kΩ with $1.8 \leq AV_{CC} \leq 2.7$ ch.1 to ch.14, ch.16 to ch.19
Input resistance of A/D Converter = 5.6 kΩ with $1.8 \leq AV_{CC} \leq 2.7$ ch.15
Input resistance of A/D Converter = 5.8 kΩ with $1.8 \leq AV_{CC} \leq 2.7$ ch.20 to ch.23
Input resistance of A/D Converter = 12.6 kΩ with $1.65 \leq AV_{CC} \leq 1.8$ ch.1 to ch.19
Input resistance of A/D Converter = 12.7 kΩ with $1.65 \leq AV_{CC} \leq 1.8$ ch.20 to ch.23

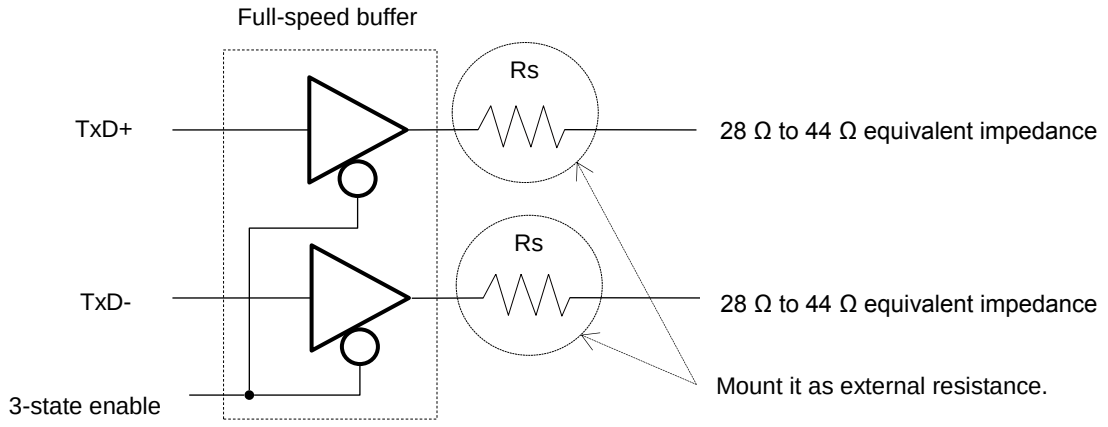
C_{AIN}: Input capacitance of A/D Converter = 9.7 pF with $2.7 \leq AV_{CC} \leq 3.6$

R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

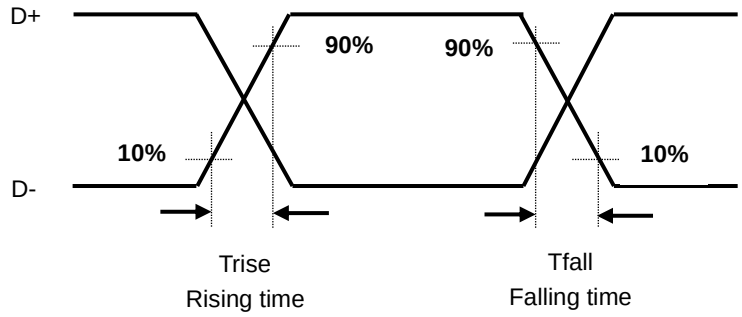
t_C: Compare time

t_{CCK} : Compare clock cycle



Rs series resistor 25 Ω to 30 Ω
Series resistor of 27 Ω (recommendation value) must be added.
And, use “resistance with an uncertainty of 5% by E24 sequence”.

*7 : They indicate rising time (Trise) and falling time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



See “Low-speed load (Compliance Load)” for condition of external load.

11.7.3 Low-Voltage Detection Interrupt 2

(T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVH2I=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH	SVH2RLI=00100	1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVH2I=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH	SVH2RLI=00101	1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVH2I=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH	SVH2RLI=00110	1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVH2I=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH	SVH2RLI=00111	1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVH2I=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH	SVH2RLI=01000	1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVH2I=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH	SVH2RLI=01001	1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVH2I=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH	SVH2RLI=01010	1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVH2I=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH	SVH2RLI=01011	1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVH2I=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH	SVH2RLI=01100	2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVH2I=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH	SVH2RLI=01101	2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVH2I=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH	SVH2RLI=01110	2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVH2I=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH	SVH2RLI=01111	2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVH2I=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH	SVH2RLI=10000	2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVH2I=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH	SVH2RLI=10001	2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVH2I=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH	SVH2RLI=10010	2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVH2I=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH	SVH2RLI=10011	3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} represents the APB1 bus clock cycle time.