

Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

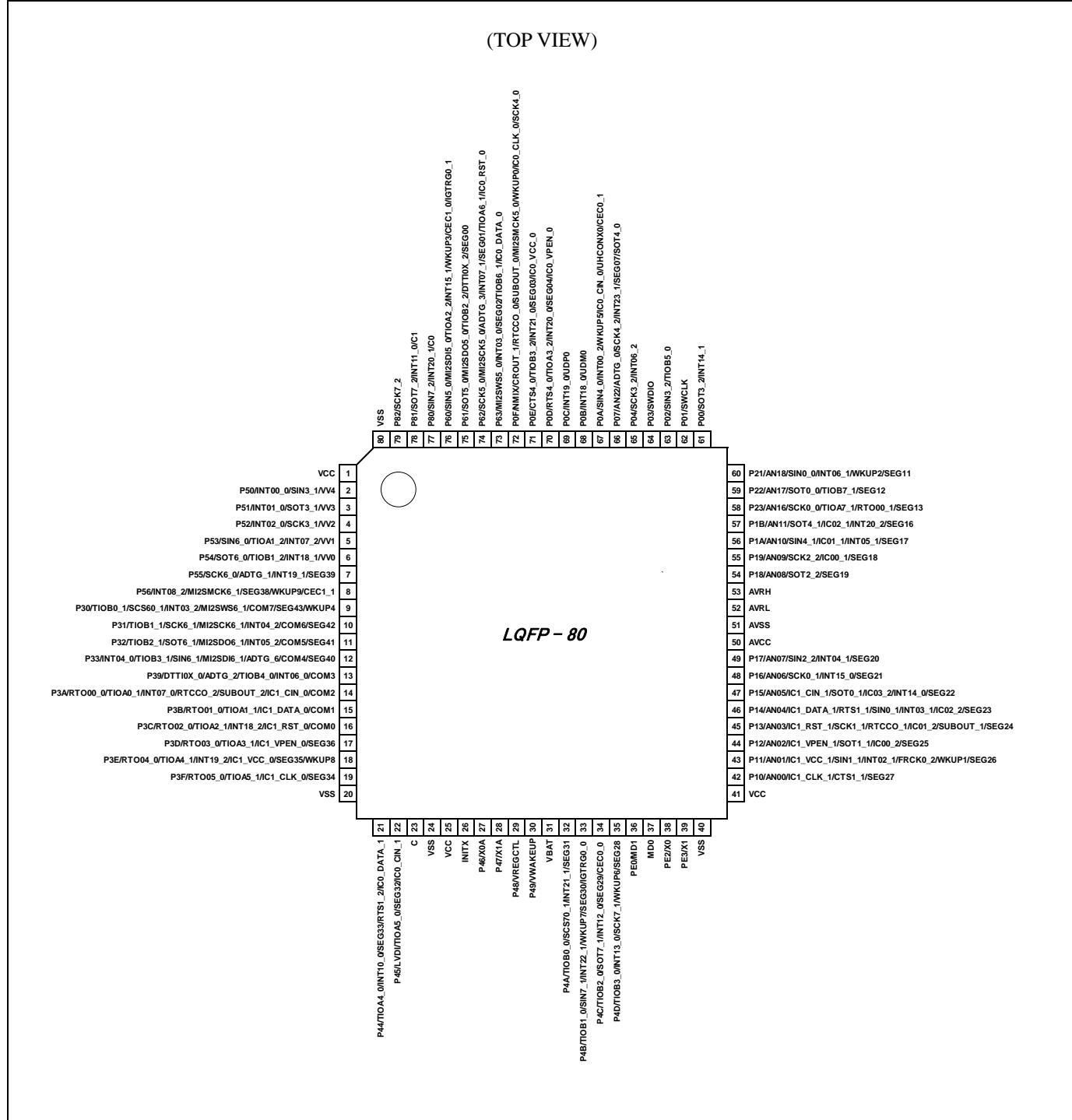
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSI0, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 23x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86f0agv20000

Table of Contents

Features.....	1
1. Product Lineup.....	7
2. Packages.....	8
3. Pin Assignment	9
4. List of Pin Functions.....	12
5. I/O Circuit Type.....	36
6. Handling Precautions	46
6.1 Precautions for Product Design.....	46
6.2 Precautions for Package Mounting.....	47
6.3 Precautions for Use Environment.....	49
7. Handling Devices	50
8. Block Diagram.....	53
9. Memory Map	54
10. Pin Status in Each CPU State.....	57
11. Electrical Characteristics	67
11.1 Absolute Maximum Ratings.....	67
11.2 Recommended Operating Conditions.....	68
11.3 DC Characteristics.....	69
11.3.1 Current Rating.....	69
11.3.2 Pin Characteristics	74
11.3.3 LCD Characteristic	75
11.4 AC Characteristics.....	79
11.4.1 Main Clock Input Characteristics.....	79
11.4.2 Sub Clock Input Characteristics	80
11.4.3 Built-in CR Oscillation Characteristics	81
11.4.4 Operating Conditions of Main PLL (In the Case of Using the Main Clock as the Input Clock of the PLL)	82
11.4.5 Operating Conditions of Main PLL (In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)	82
11.4.6 Reset Input Characteristics	83
11.4.7 Power-on Reset Timing.....	83
11.4.8 Base Timer Input Timing	84
11.4.9 CSIO/SPI/UART Timing	85
11.4.10 External Input Timing	102
11.4.11 I ² C Timing.....	103
11.4.12 I ² S Timing	104
11.4.13 Smart Card Interface Characteristics	105
11.4.14 SW-DP Timing.....	106
11.5 12-bit A/D Converter.....	107
11.6 USB Characteristics	110
11.7 Low-Voltage Detection Characteristics	115
11.7.1 Low-Voltage Detection Reset.....	115
11.7.2 Low-Voltage Detection Interrupt.....	116
11.7.3 Low-Voltage Detection Interrupt 2.....	117
11.8 Flash Memory Write/Erase Characteristics	118
11.9 Return Time from Low-Power Consumption Mode	119
11.9.1 Return Factor: Interrupt/WKUP	119
11.9.2 Return Factor: Reset.....	121
12. Ordering Information	123

3. Pin Assignment

FPT-80P-M21



4. List of Pin Functions

List of Pin Numbers

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
1	1	1	VCC	-	
2	2	2	P50	Q	X
			SIN3_1		
			INT00_0		
			VV4		
			P51		
3	3	3	SOT3_1	Q	X
			INT01_0		
			VV3		
			P52		
4	4	4	SCK3_1	Q	X
			INT02_0		
			VV2		
			P53		
5	5	5	SIN6_0	Q	X
			TIOA1_2		
			INT07_2		
			VV1		
			P54		
6	6	6	SOT6_0	Q	X
			TIOB1_2		
			INT18_1		
			VV0		
			P55	L	S
7	7	7	SCK6_0		
			ADTG_1		
			INT19_1		
			SEG39		
			P56		
8	8	8	MI2SMCK6_1	L	U
			CEC1_1		
			INT08_2		
			WKUP9		
			SEG38		
			SIN1_0		
			P57		
9	-	-	SOT1_0	F	I
10	-	-	P58	F	I
11	-	-	SCK1_0	F	J
			P59		
			SIN7_0		
			INT16_1		

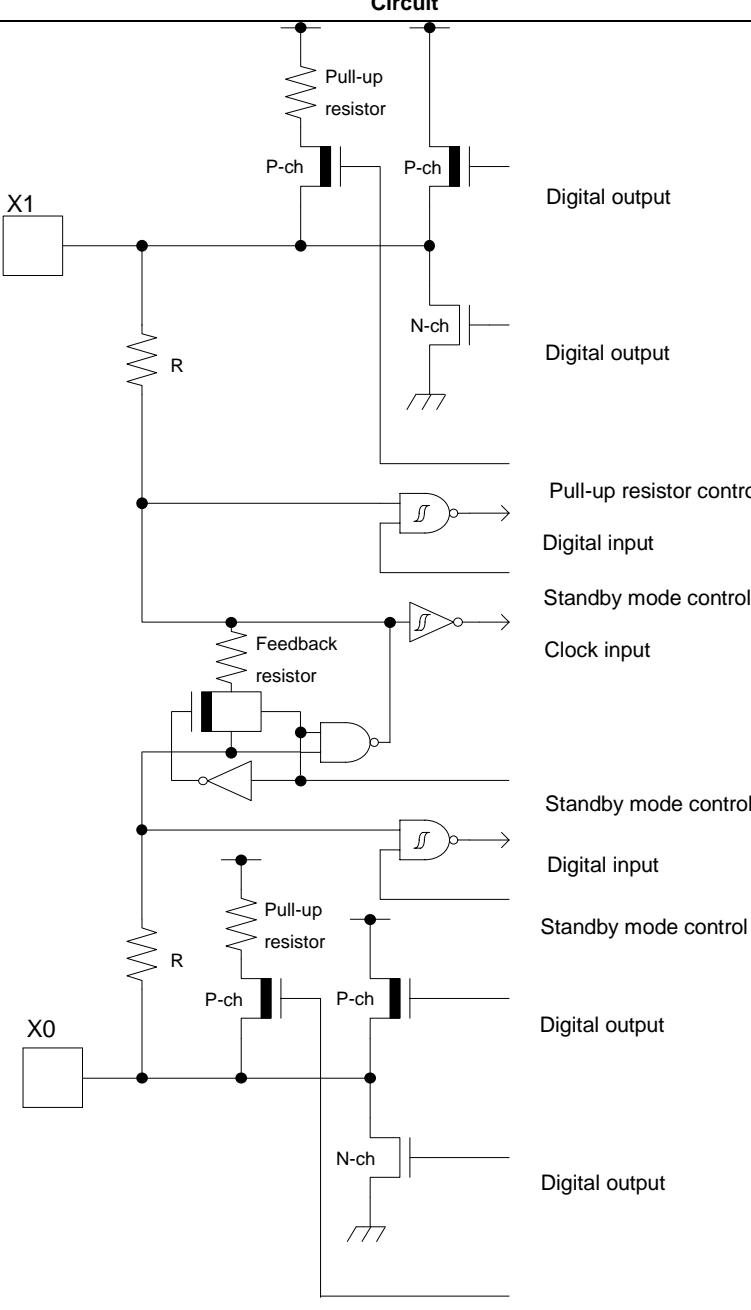
Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
33	28	-	P41	F	J
			TIOA1_0		
			SOT1_2		
			IC0_VCC_1		
			INT13_1		
34	29	-	P42	F	J
			TIOA2_0		
			SCK1_2		
			IC0_VPEN_1		
			INT08_0		
35	30	-	P43	F	J
			TIOA3_0		
			CTS1_2		
			ADTG_7		
			IC0_RST_1		
			INT09_0		
36	31	21	P44	L	S
			TIOA4_0		
			IC0_DATA_1		
			INT10_0		
			RTS1_2		
			SEG33		
37	32	22	P45	L	P
			TIOA5_0		
			IC0_CIN_1		
			LVDI		
			SEG32		
38	33	23	C	-	-
39	34	24	VSS	-	-
40	35	25	VCC	-	-
41	36	26	INITX	B	C
42	37	27	P46	D	E
			X0A		
43	38	28	P47	E	F
			X1A		
44	39	29	P48	I	I
			VREGCTL		
45	40	30	P49	I	I
			VWAKEUP		
46	41	31	VBAT	-	-
47	42	32	P4A	L	S
			TIOB0_0		
			SCS70_1		
			INT21_1		
			SEG31		
48	43	33	P4B	L	T
			TIOB1_0		
			SIN7_1		
			INT22_1		
			WKUP7		
			SEG30		
			IGTRG0_0		

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Real-time Clock	RTCCO_0	0.5-seconds pulse output pin of Real-time clock	107	92	72
	RTCCO_1		65	55	45
	RTCCO_2		24	19	14
HDMI-CEC/ Remote Control Reception	SUBOUT_0	Sub clock output pin	107	92	72
	SUBOUT_1		65	55	45
	SUBOUT_2		24	19	14
HDMI-CEC/ Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	49	44	34
	CEC0_1		102	87	67
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	116	96	76
	CEC1_1		8	8	8
LCD Controller	VV0	LCD controller power supply I/O pin	6	6	6
	VV1		5	5	5
	VV2		4	4	4
	VV3		3	3	3
	VV4		2	2	2
	C0	LCD controller flying capacitor output pin	117	97	77
	C1		118	98	78
	COM0	LCD controller common output pin	26	21	16
	COM1		25	20	15
	COM2		24	19	14
	COM3		23	18	13
	COM4		17	12	12
	COM5		16	11	11
	COM6		15	10	10
	COM7		14	9	9
	SEG00	LCD controller segment output pin	115	95	75
	SEG01		114	94	74
	SEG02		113	93	73
	SEG03		106	91	71
	SEG04		105	90	70
	SEG05		101	86	-
	SEG06		100	85	-
	SEG07		99	84	66
	SEG08		98	83	-
	SEG09		97	82	-
	SEG10		89	74	-
	SEG11		88	73	60
	SEG12		87	72	59
	SEG13		86	71	58
	SEG14		79	69	-
	SEG15		78	68	-
	SEG16		77	67	57

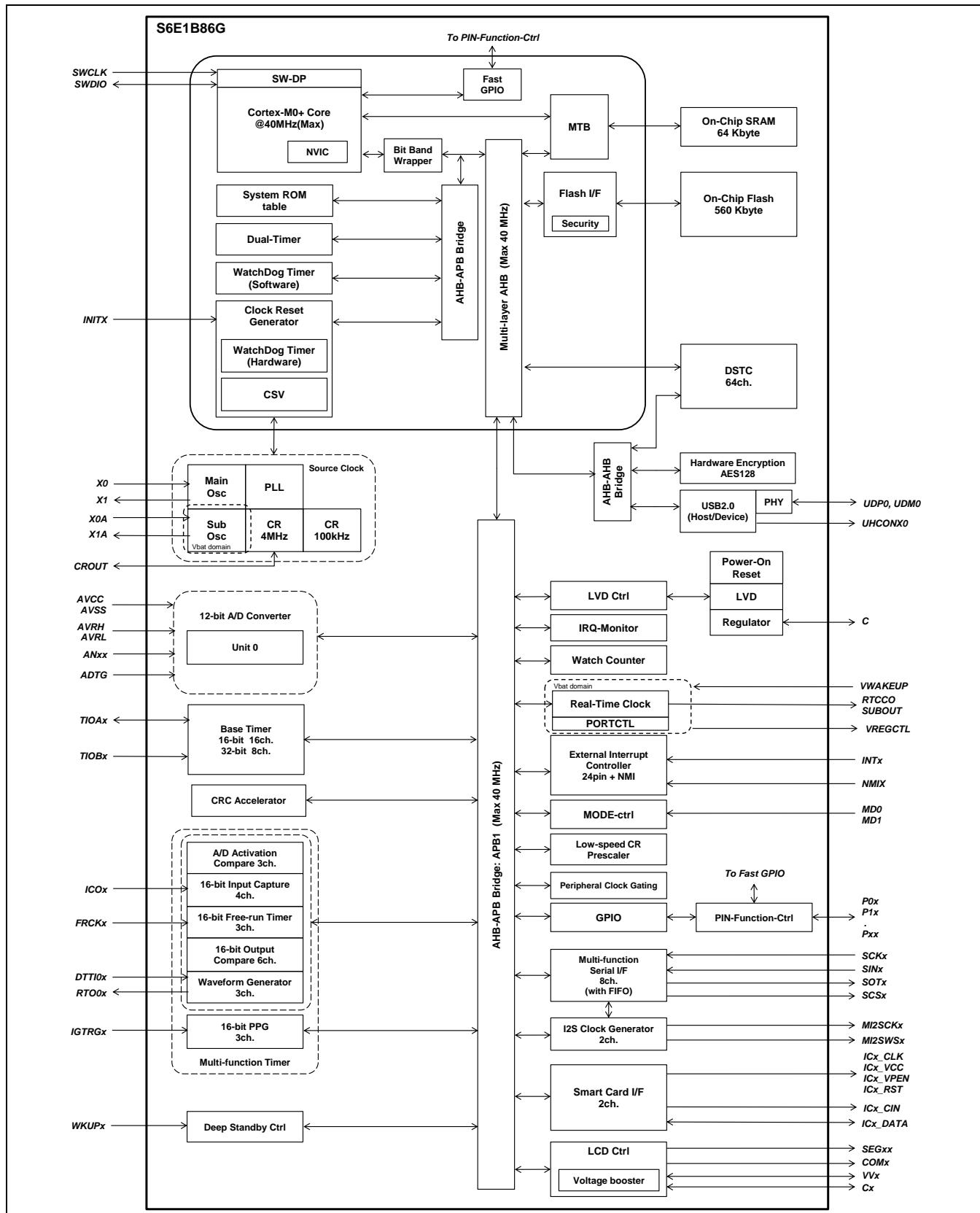
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	REGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

*: PE0 is an open drain pin, cannot output high.

5. I/O Circuit Type

Type	Circuit	Remarks
A	 <p>The diagram illustrates the internal structure of Type A I/O circuits. It shows two oscillators, X1 and X0, each consisting of a resistor R and a P-channel MOSFET. The outputs of these oscillators feed into a complex logic network. This network includes P-channel and N-channel MOSFETs, diodes, and various control logic blocks such as AND gates, inverters, and comparators. The logic is designed to support multiple functions: digital output, pull-up resistor control, digital input, standby mode control, clock input, and CMOS level output. Specific notes include the use of approximately 1 MΩ for oscillation feedback resistors and 33 kΩ for pull-up resistors. Current values are noted as $I_{OH} = -4\text{mA}$ and $I_{OL} = 4 \text{ mA}$. The logic also includes CMOS level hysteresis inputs and a feedback path for oscillation control.</p>	<p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected. Oscillation feedback resistor : Approximately 1 MΩ</p> <p>With standby mode control</p> <p>When the GPIO is selected. CMOS level output. CMOS level hysteresis input With pull-up resistor control With standby mode control Pull-up resistor : Approximately 33 kΩ $I_{OH} = -4\text{mA}$, $I_{OL} = 4 \text{ mA}$</p>

8. Block Diagram



Peripheral Address Map

Start Address	End Address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function Timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		LCD Controller
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/ Remote Control Receiver
0x4003_5000	0x4003_5FFF		Low-Voltage Detection / DS mode / Vref Calibration
0x4003_6000	0x4003_6FFF		USB Clock Generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_FFFF		Reserved
0x4003_C900	0x4003_C9FF		Smart Card Interface
0x4003_CA00	0x4003_CAFF		I ² S Clock Generator
0x4003_CB00	0x4003_FFFF		Reserved
0x4004_0000	0x4005_FFFF	AHB	USB ch.0
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		DSTC
0x4006_2000	0x41FF_FFFF		Reserved

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State		
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable		
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1		
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-		
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Input enabled	Input enabled	Input enabled		
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected		
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected		
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state		
F	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state/When oscillation stops*, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*, Hi-Z / Internal input fixed at 0		
G	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected		
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0					
	GPIO selected											

Parameter	Symbol (Pin Name)	Conditions	Value		Unit	Remarks
			Typ	Max		
Power supply current	I_{CCH} (VCC)	Stop mode	$T_A=25^\circ C$ $V_{CC}=3.3 V$	10	TBD	μA
			$T_A=25^\circ C$ $V_{CC}=1.65 V$	9	TBD	μA
			$T_A=105^\circ C$ $V_{CC}=3.6 V$	-	TBD	μA
	I_{CCT} (VCC)	Sub timer mode	$T_A=25^\circ C$ $V_{CC}=3.3 V$ 32 kHz Crystal oscillation	13	TBD	μA
			$T_A=25^\circ C$ $V_{CC}=1.65 V$ 32 kHz Crystal oscillation	12	TBD	μA
			$T_A=105^\circ C$ $V_{CC}=3.6 V$ 32 kHz Crystal oscillation	-	TBD	μA
	I_{CCR} (VCC)	RTC mode	$T_A=25^\circ C$ $V_{CC}=3.3 V$ 32 kHz Crystal oscillation	10.5	TBD	μA
			$T_A=25^\circ C$ $V_{CC}=1.65 V$ 32 kHz Crystal oscillation	9.5	TBD	μA
			$T_A=105^\circ C$ $V_{CC}=3.6 V$ 32 kHz Crystal oscillation	-	TBD	μA

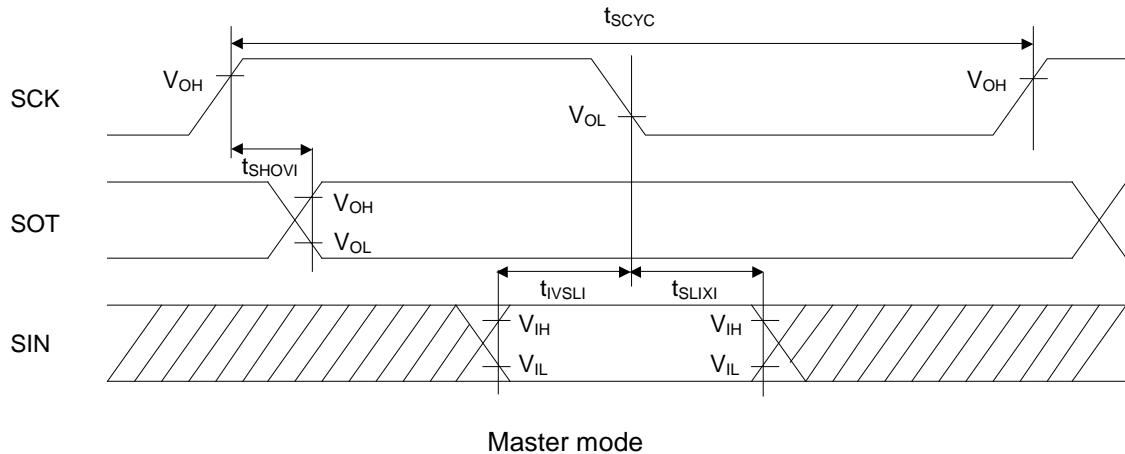
*1: All ports are fixed. LVD off. Flash off.

CSIO (SPI=0, SCINV=1)
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^\circ\text{C to }+105^\circ\text{C})$

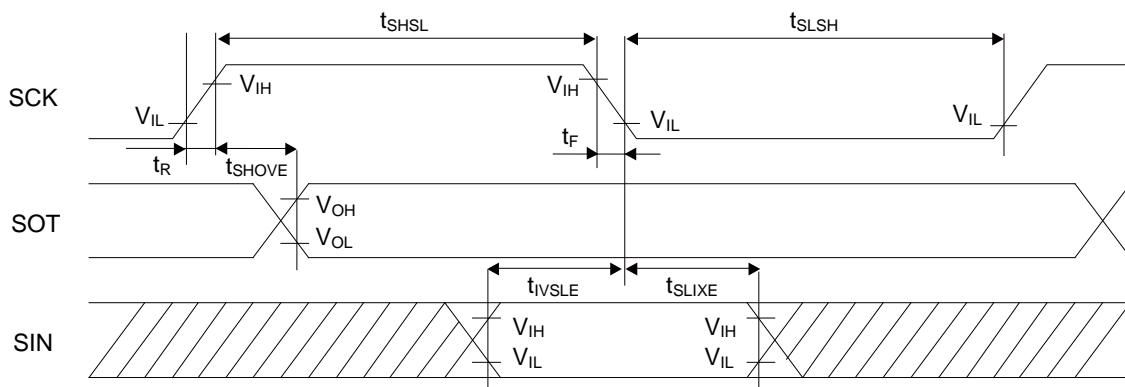
Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKx	Master mode	4 t _{CYCP}	-	4 t _{CYCP}	-	ns
SCK \uparrow \rightarrow SOT delay time	t _{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN \rightarrow SCK \downarrow setup time	t _{IVSLI}	SCKx, SINx		60	-	50	-	ns
SCK \downarrow \rightarrow SIN hold time	t _{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx	Slave mode	2 t _{CYCP} - 10	-	2 t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx		t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK \uparrow \rightarrow SOT delay time	t _{SHOVE}	SCKx, SOTx		-	65	-	52	ns
SIN \rightarrow SCK \downarrow setup time	t _{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK \downarrow \rightarrow SIN hold time	t _{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t _F	SCKx		-	5	-	5	ns
SCK rising time	t _R	SCKx		-	5	-	5	ns

Notes:

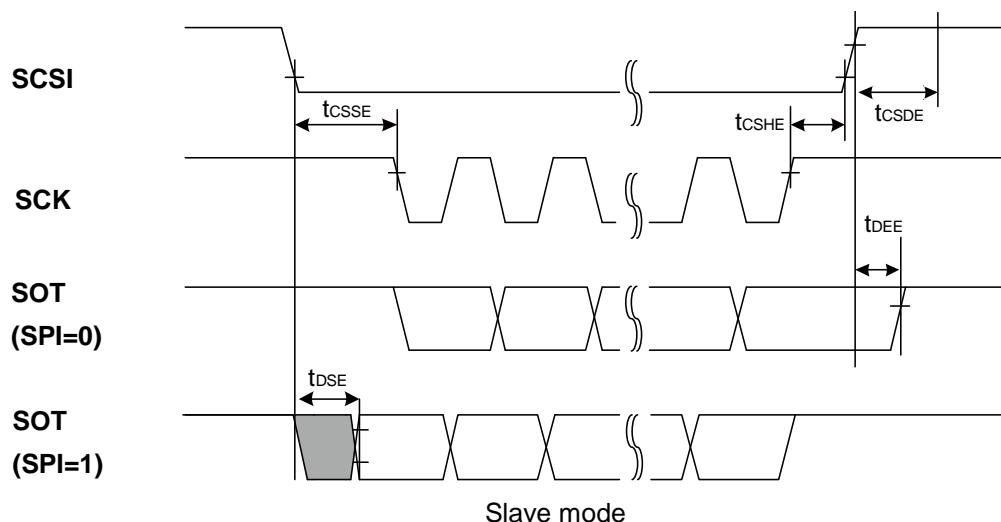
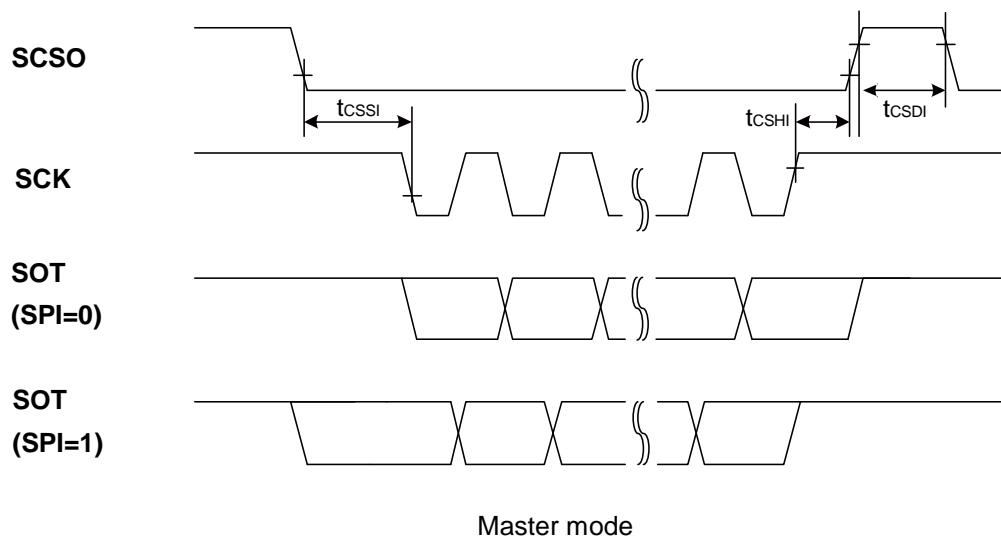
- The above AC characteristics are for clock synchronous mode.
- t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.
For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- External load capacitance C_L=30 pF



Master mode



Slave mode



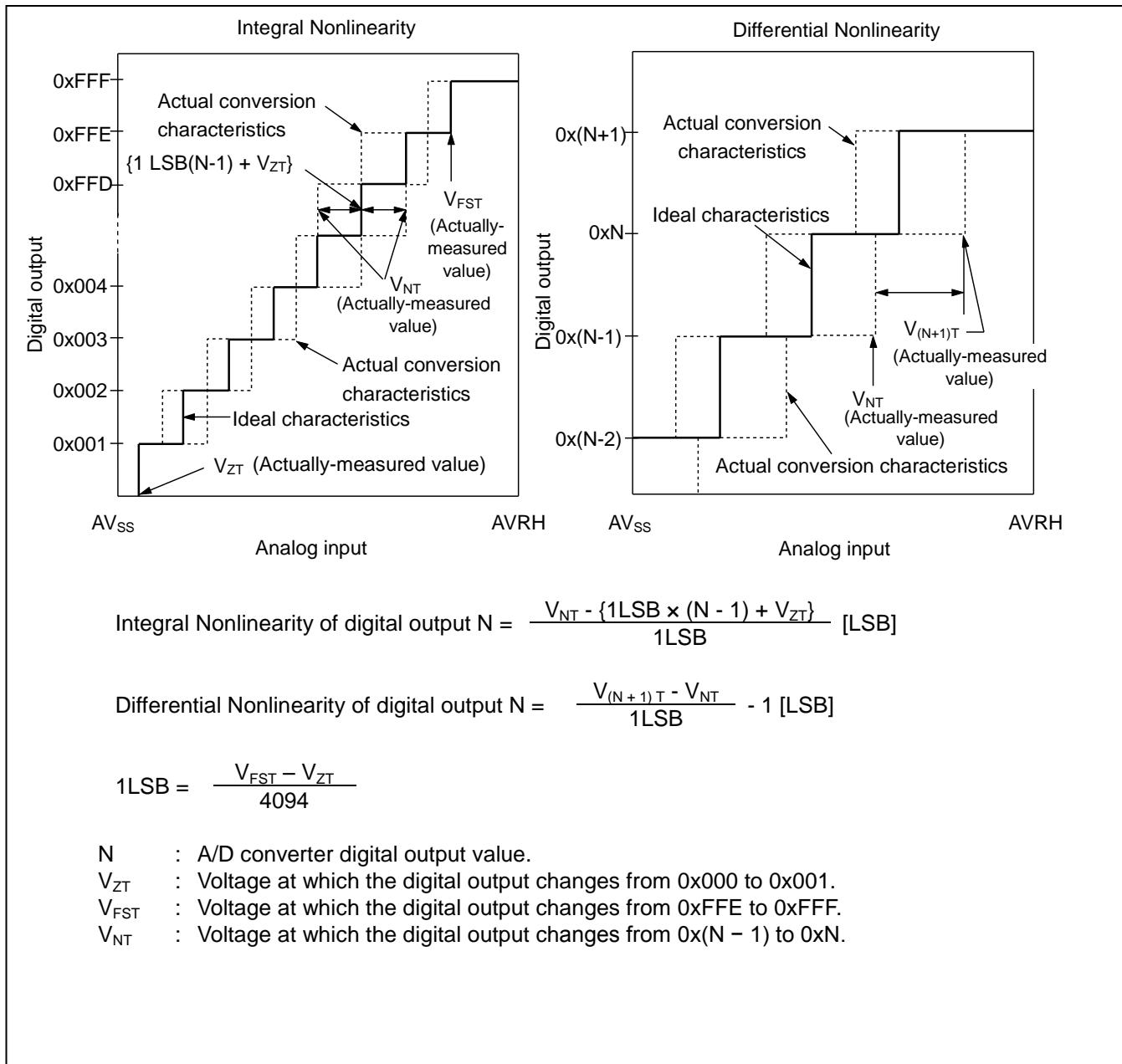
11.4.13 Smart Card Interface Characteristics
 $(V_{CC}=1.65 \text{ V to } 3.3 \text{ V}, V_{SS}=0 \text{ V}, T_A=-40^\circ\text{C to } +105^\circ\text{C})$

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t_R	ICx_VCC, ICx_RST, ICx_CLK, ICx_DATA	$C_L=30 \text{ pF}$	4	20	ns	
Output falling time	t_F			4	20	ns	
Output clock frequency	f_{CLK}			-	20	MHz	
Duty cycle	Δ			45%	55%		

- External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx_CIN pin when it's used as smart card reader function.

Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 \longleftrightarrow 0b000000000001) and the full-scale transition point (0b111111111110 \longleftrightarrow 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed ^{*1}	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	$8160 \times t_{CYCP}^{*2}$	μs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	μs	

*1: The value of low voltage detection reset is always fixed.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

11.8 Flash Memory Write/Erase Characteristics

($V_{CC}=1.65$ V to 3.6 V, $T_A=-40^\circ\text{C}$ to $+105^\circ\text{C}$)

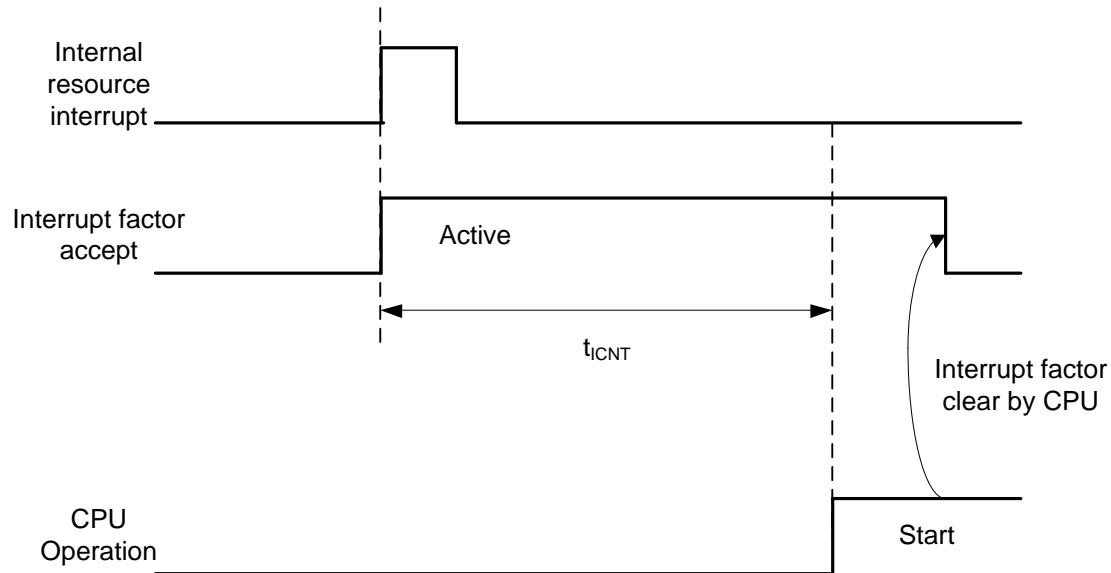
Parameter	Value			Unit	Remarks	
	Min	Typ*	Max*			
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	μs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time (Target Value)

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

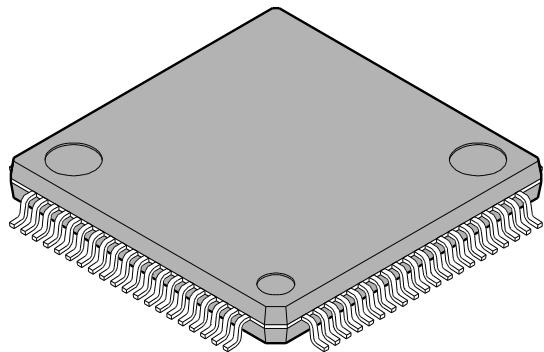
*: At average $+85^\circ\text{C}$

Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt*)


*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes.
See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".

80-pin plastic LQFP

(FPT-80P-M21)
Lead pitch 0.50 mm

Package width × package length 12 mm × 12 mm

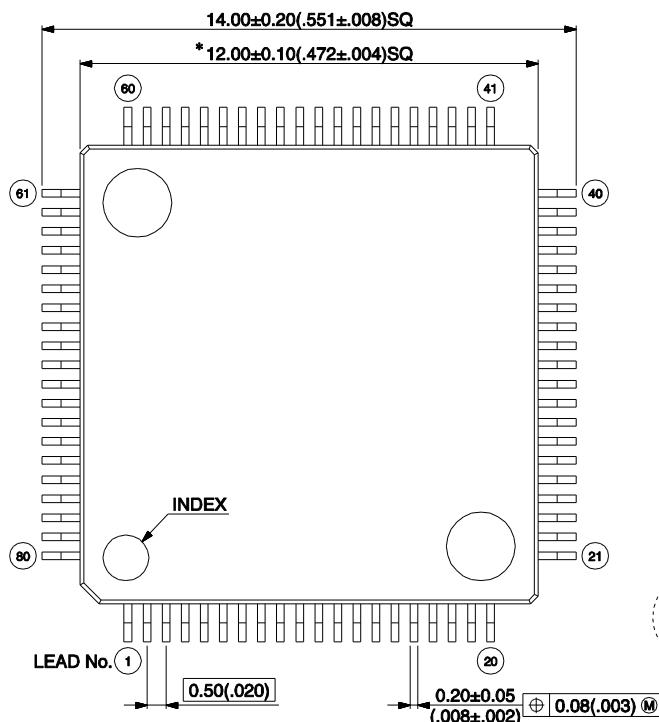
Lead shape Gullwing

Sealing method Plastic mold

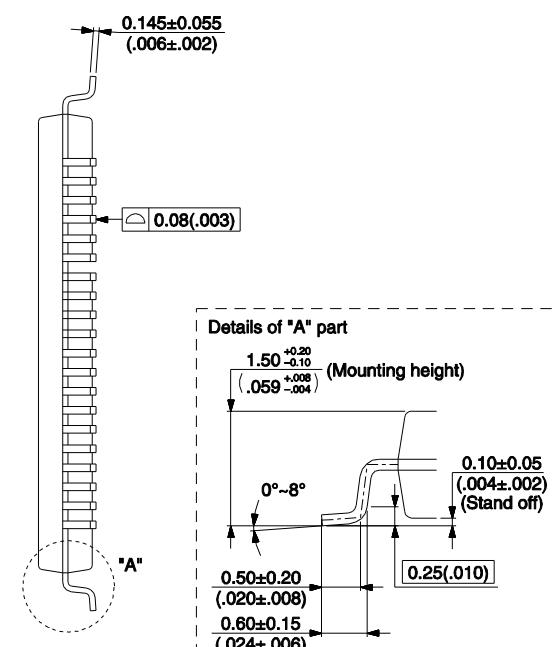
Mounting height 1.70 mm Max

Weight 0.47 g

**Code
(Reference)** P-LFQFP80-12×12-0.50

**80-pin plastic LQFP
(FPT-80P-M21)**


Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
 Note: The values in parentheses are reference values