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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 23x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86fhagv20000

1. Product Lineup

Memory Size

Product Name		S6E1B84E/F/G	S6E1B86E/F/G
On-chip Flash memory	Upper Bank	256 Kbytes	512 Kbytes
	Lower Bank	48 Kbytes	48 Kbytes
On-chip SRAM		32 Kbytes	64 Kbytes

Function

Product Name			S6E1B84E0A S6E1B86E0A S6E1B84EHA S6E1B86EHA	S6E1B84F0A S6E1B86F0A S6E1B84FHA S6E1B86FHA	S6E1B84G0A S6E1B86G0A S6E1B84GHA S6E1B86GHA
Pin count			80	100	120
CPU			Cortex-M0+		
	Frequency		40.8 MHz		
Power supply voltage range			1.65 V to 3.6 V		
USB 2.0 (Device/Host)			1 unit		
DSTC			64ch		
Multi-function Serial Interface (UART/CSIO (SPI)/I^{2}C/I^{2}S)			8ch (Max) with 128 bytes FIFO I^{2}S: ch.5, ch.6		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch (Max)		
LCD controller			20SEG x 8COM(Max) / 24SEG x 4COM(Max)	32SEG x 8COM(Max) / 36SEG x 4COM(Max)	40SEG x 8COM(Max) / 44SEG x 4COM(Max)
Multi-function Timer	A/D activation compare	6ch	1 unit		
	Input capture	4ch			
	Free-run timer	3ch			
	Output compare	6ch			
	Waveform generator	3ch			
	PPG	3ch			
Dual Timer			1 unit		
HDMI-CEC/ Remote Control Receiver			2ch (max)		
Smart Card Interface			2ch (max)		
Real-time Clock			1 unit (with battery power)		
Watch Counter			1 unit		
CRC Accelerator			Yes		
Watchdog timer			1ch (SW) + 1ch (HW)		
External Interrupt			24 pins (Max), NMI × 1		
I/O port			65 pins (Max)	82 pins (Max)	102 pins (Max)
12-bit A/D converter			16ch (1 unit)	23ch (1 unit)	24ch (1 unit)
CSV (Clock Supervisor)			Yes		
LVD (Low-voltage Detection)			2ch		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug Function			SW-DP		
Unique ID			Yes		
AES Calculator			-	Yes*1	-	Yes*1	-	Yes*1

*1: AES Calculator is built in following products.
S6E1B86GHA, S6E1B84GHA, S6E1B86FHA, S6E1B84FHA, S6E1B86EHA, S6E1B84EHA

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
  See "11 Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
12	-	-	P5A SOT7_0 INT16_2	F	J
13	-	-	P5B SCK7_0 INT17_2	F	J
14	9	9	P30 TIOB0_1 SCS60_1 MI2SWS6_1 INT03_2 WKUP4 COM7 SEG43	M	T
15	10	10	P31 TIOB1_1 SCK6_1 MI2SCK6_1 INT04_2 COM6 SEG42	M	S
16	11	11	P32 TIOB2_1 SOT6_1 MI2SDO6_1 INT05_2 COM5 SEG41	M	S
17	12	12	P33 TIOB3_1 SIN6_1 MI2SDI6_1 INT04_0 ADTG_6 COM4 SEG40	M	S
18	13	-	P34 SCS61_1 FRCK0_0 TIOB4_1	I	I
19	14	-	P35 SCS62_1 IC03_0 TIOB5_1 INT08_1 SEG37	L	S
20	15	-	P36 IC02_0 SIN5_2 INT09_1 WKUP11	I	N
21	16	-	P37 IC01_0 SOT5_2 INT10_1	I	J

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
22	17	-	P38 IC00_0 SCK5_2 INT11_1	F	J
23	18	13	P39 DTTI0X_0 TIOB4_0 ADTG_2 INT06_0 COM3	N	S
24	19	14	P3A RTO00_0 TIOA0_1 RTCCO_2 SUBOUT_2 IC1_CIN_0 INT07_0 COM2	N	S
25	20	15	P3B RTO01_0 TIOA1_1 IC1_DATA_0 COM1	N	P
26	21	16	P3C RTO02_0 TIOA2_1 INT18_2 IC1_RST_0 COM0	N	S
27	22	17	P3D RTO03_0 TIOA3_1 IC1_VPEN_0 SEG36	L	P
28	23	18	P3E RTO04_0 TIOA4_1 IC1_VCC_0 INT19_2 WKUP8 SEG35	L	T
29	24	19	P3F RTO05_0 TIOA5_1 IC1_CLK_0 SEG34	L	P
30	25	20	VSS	-	-
31	26	-	VCC	-	-
32	27	-	P40 TIOA0_0 IC0_CLK_1 INT12_1 SIN1_2	F	J

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
76	66	56	P1A SIN4_1 IC01_1 INT05_1 AN10 SEG17	P	V
77	67	57	P1B SOT4_1 IC02_1 INT20_2 AN11 SEG16	P	V
78	68	-	P1C SCK4_1 IC03_1 INT21_2 AN12 SEG15	P	V
79	69	-	P1D CTS4_1 DTTI0X_1 INT22_2 AN13 SEG14	P	V
80	70	-	P1E RTS4_1 FRCK0_1 ADTG_5 INT23_2 AN14	H	L
81	-	-	P28 RTO05_1 TIOB6_2 ADTG_4	F	I
82	-	-	P27 RTO04_1 TIOA6_2 INT02_2 AN15	G	L
83	-	-	P26 SCK2_1 RTO03_1	F	I
84	-	-	P25 SOT2_1 RTO02_1	F	I
85	-	-	P24 SIN2_1 RTO01_1 INT17_1	F	J
86	71	58	P23 SCK0_0 TIOA7_1 RTO00_1 AN16 SEG13	P	K

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
ADC	ADTG_0	A/D converter external trigger input pin	99	84	66
	ADTG_1		7	7	7
	ADTG_2		23	18	13
	ADTG_3		114	94	74
	ADTG_4		81	-	-
	ADTG_5		80	70	-
	ADTG_6		17	12	12
	ADTG_7		35	30	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	42
	AN01		63	53	43
	AN02		64	54	44
	AN03		65	55	45
	AN04		66	56	46
	AN05		67	57	47
	AN06		68	58	48
	AN07		69	59	49
	AN08		74	64	54
	AN09		75	65	55
	AN10		76	66	56
	AN11		77	67	57
	AN12		78	68	-
	AN13		79	69	-
	AN14		80	70	-
	AN15		82	-	-
	AN16		86	71	58
	AN17		87	72	59
	AN18		88	73	60
	AN19		89	74	-
	AN20		97	82	-
	AN21		98	83	-
	AN22		99	84	66
	AN23		100	85	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-
	TIOA0_1		24	19	14
	TIOA0_2		100	85	-
	TIOB0_0	Base timer ch.0 TIOB pin	47	42	32
	TIOB0_1		14	9	9
	TIOB0_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator controlling RTO00 to RTO05 outputs of Multi-function Timer 0.	23	18	13
	DTTI0X_1		79	69	-
	DTTI0X_2		115	95	75
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	18	13	-
	FRCK0_1		80	70	-
	FRCK0_2		63	53	43
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	22	17	-
	IC00_1		75	65	55
	IC00_2		64	54	44
	IC01_0		21	16	-
	IC01_1		76	66	56
	IC01_2		65	55	45
	IC02_0		20	15	-
	IC02_1		77	67	57
	IC02_2		66	56	46
	IC03_0		19	14	-
	IC03_1		78	68	-
	IC03_2		67	57	47
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	24	19	14
	RTO00_1 (PPG00_1)		86	71	58
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	25	20	15
	RTO01_1 (PPG00_1)		85	-	-
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	26	21	16
	RTO02_1 (PPG02_1)		84	-	-
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	27	22	17
	RTO03_1 (PPG02_1)		83	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	28	23	18
	RTO04_1 (PPG04_1)		82	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	29	24	19
	RTO05_1 (PPG04_1)		81	-	-
	IGTRG0_0	PPG IGBT mode external trigger input pin	48	43	33
	IGTRG0_1		116	96	76

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

Stabilizing Supply Voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

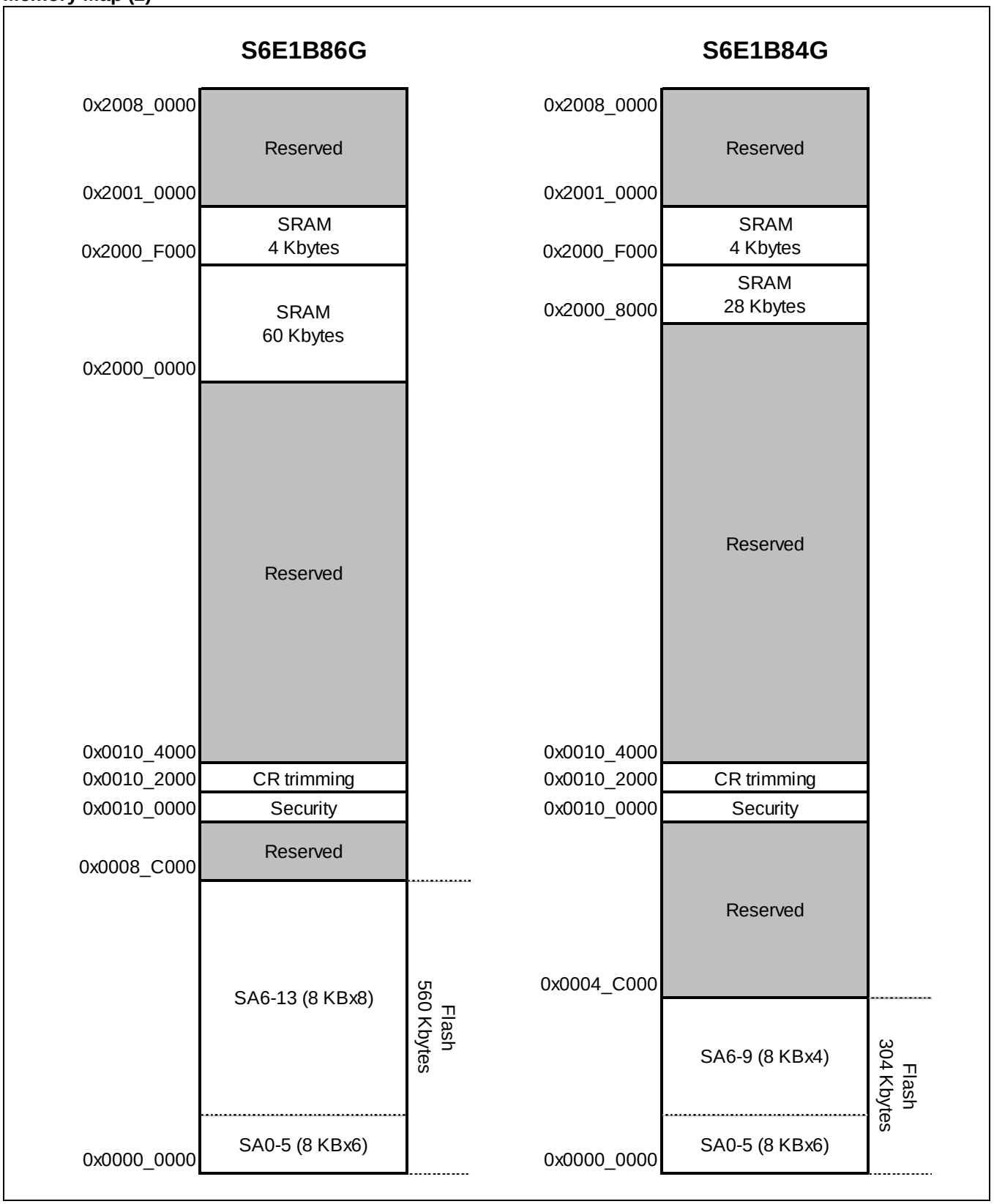
Size: More than 3.2 mm × 1.5 mm

Load capacitance: Approximately 6 pF to 7 pF

■Lead type

Load capacitance: Approximately 6 pF to 7 pF

Memory Map (2)



*: See "S6E1B8 Series Flash Programming Manual" to check details of the Flash memory.

11.2 Recommended Operating Conditions

(V_{SS}=AV_{SS}=0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65 *5	3.6	V	*1
			2.2	3.6	V	*2
			3.0	3.6	V	*3
LCD input voltage	V_{VV4}	-	2.2	V_{CC}	V	No booster used
		-	2.2	4.7	V	Booster is used
LCD External Capacitor *6	C_f,C_{VV1}, C_{VV2},C_{VV3}, C_{VV4}	-	0.5	1.3	µF	Booster is used
Sub Oscillation frequency *7	Fin	-	-	-	kHz	Typical is 32.768 kHz
Analog power supply voltage	AV_{CC}	-	1.65	3.6	V	AV_{CC}=V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	AV_{CC} ≥ 2.7 V
			AV_{CC}	AV_{CC}	V	AV_{CC} < 2.7 V
	AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	µF	For regulator*4
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: When LCD Controller is not used.

*2: When LCD Controller is used.

*3: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

*4: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*5: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

*6: LCD external capacitor between VVx to VSS, and between C0 and C1.

*7: If a Booster is used, Sub OSC should provide operation clock at typically 32.768 kHz.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCVBAT} (VBAT)	RTC operation	T_A=25°C V_{CC}=3.0V 32 kHz Crystal oscillation	0.9	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V 32 kHz Crystal oscillation	0.8	TBD	µA	*1
			T_A=105°C V_{CC}=3.6V 32 kHz Crystal oscillation	-	TBD	µA	*1
		RTC stop	T_A=25°C V_{CC}=3.0V	0.05	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V	0.02	TBD	µA	*1
			T_A=105°C V_{CC}=3.6V	-	TBD	µA	*1

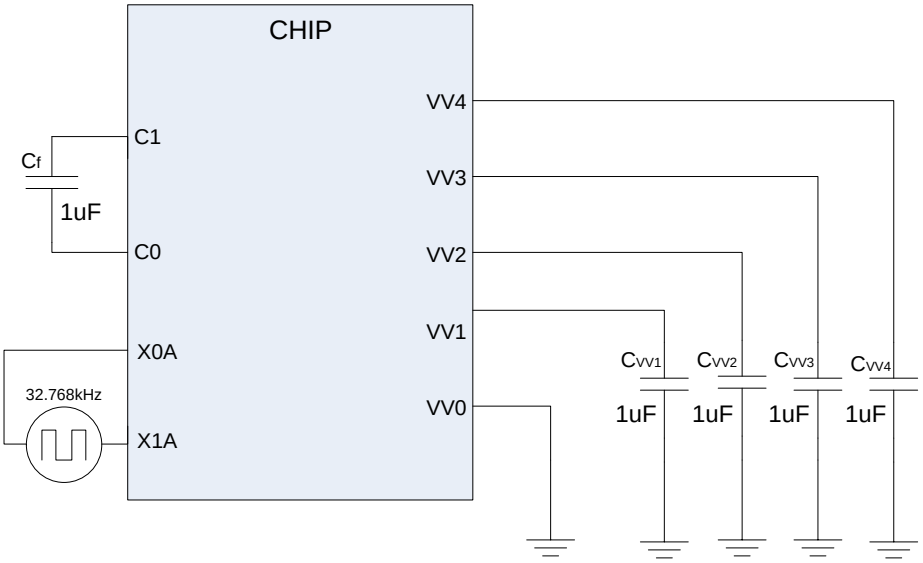
*1: All ports are fixed.

11.3.3.2 LCD Characteristic With Booster

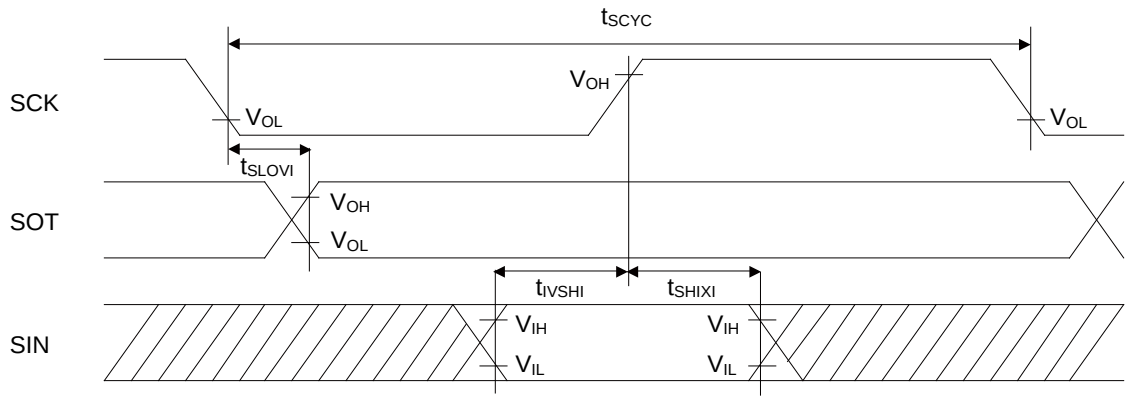
Recommended LCD Operation Conditions With Booster

(V_{CC} =AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

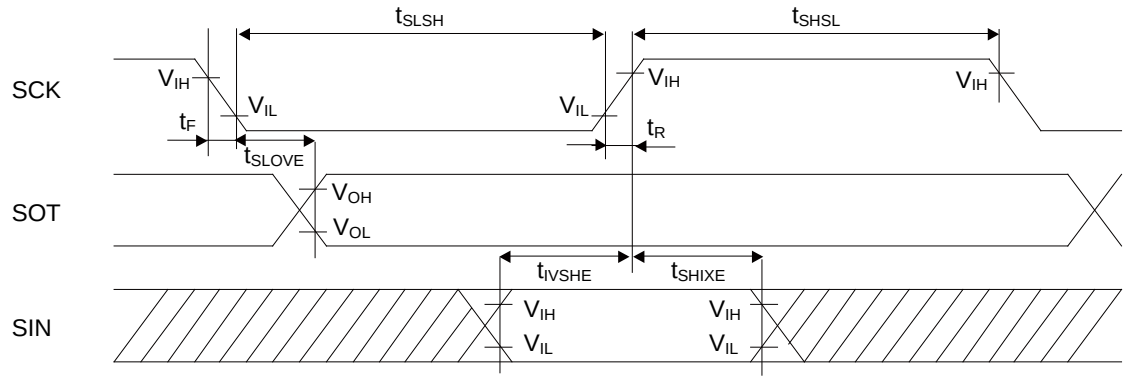
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Voltage correlation	VCC-VV1	VCC,VV1	0.35	-	-	V	VCC-VV1 must be larger than 0.35 V
External input tolerant voltage	V_{tole}	VV1,VV2,VV3,VV4,C0,C1	0	-	5.5	V	
Operating frequency	f_{IN}	-	-	32.768	-	kHz	Crystal oscillator
External Capacitor	C_f,C_{VV1}, C_{VV2},C_{VV3}, C_{VV4}	VV1,VV2,VV3,VV4,C0,C1	0.5	1	1.3	µF	
LCD capacitor	$C_{LCD/1COM}$	-	-	1.25	8	µF	
Frame period	t_{FRAME}	-	1/150	-	1/30	s	



LCD Booster 1/4 mode （BIAS[1:0]=2'b10)



Master mode



Slave mode

SPI (SPI=1, SCINV=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		60	-	50	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} +10	-	t_{CYCP} +10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

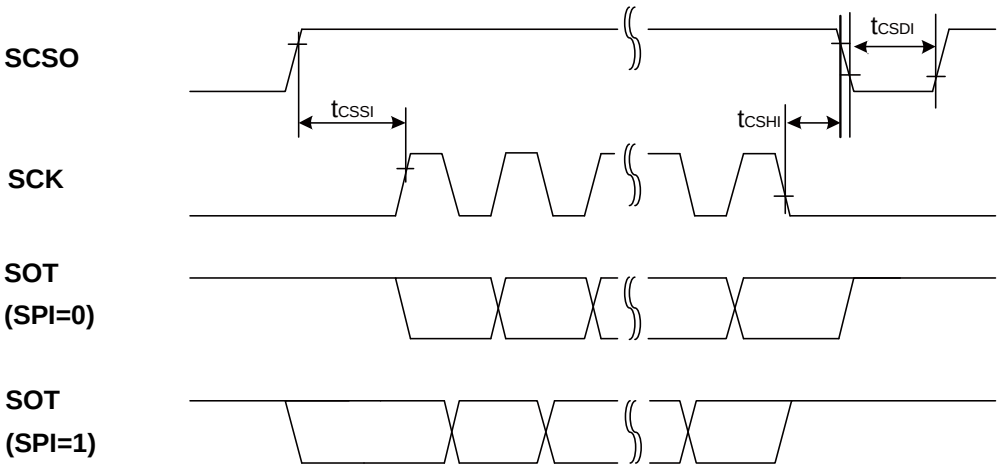
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

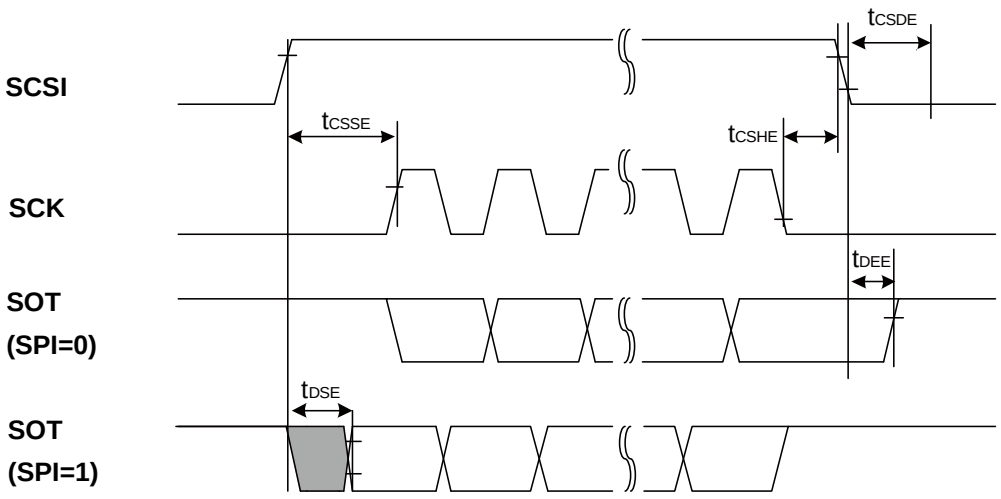
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode



Slave mode

11.4.10 External Input Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

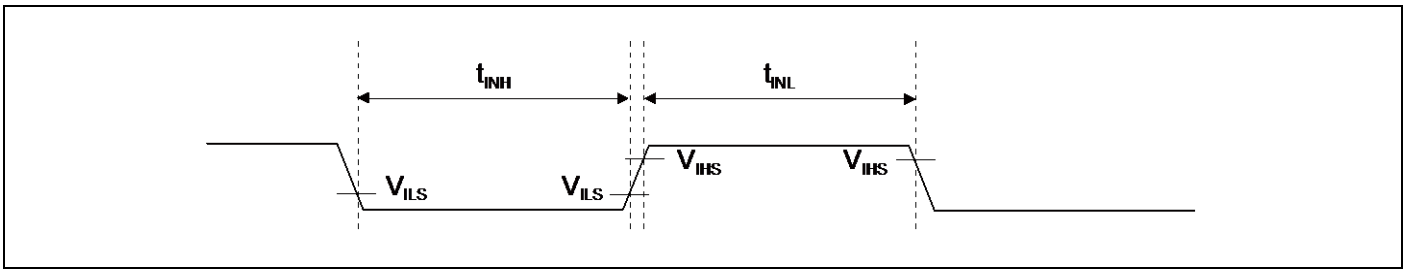
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	2 t_{CYCP}*1	-	ns	Wave form generator
		INTxx, NMIX	*2	2 t_{CYCP} +100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

*1: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

*2: In Run mode and Sleep mode

*3: In Timer mode and RTC mode and Stop mode

*4: In Deep Standby RTC mode and Deep Standby Stop mode

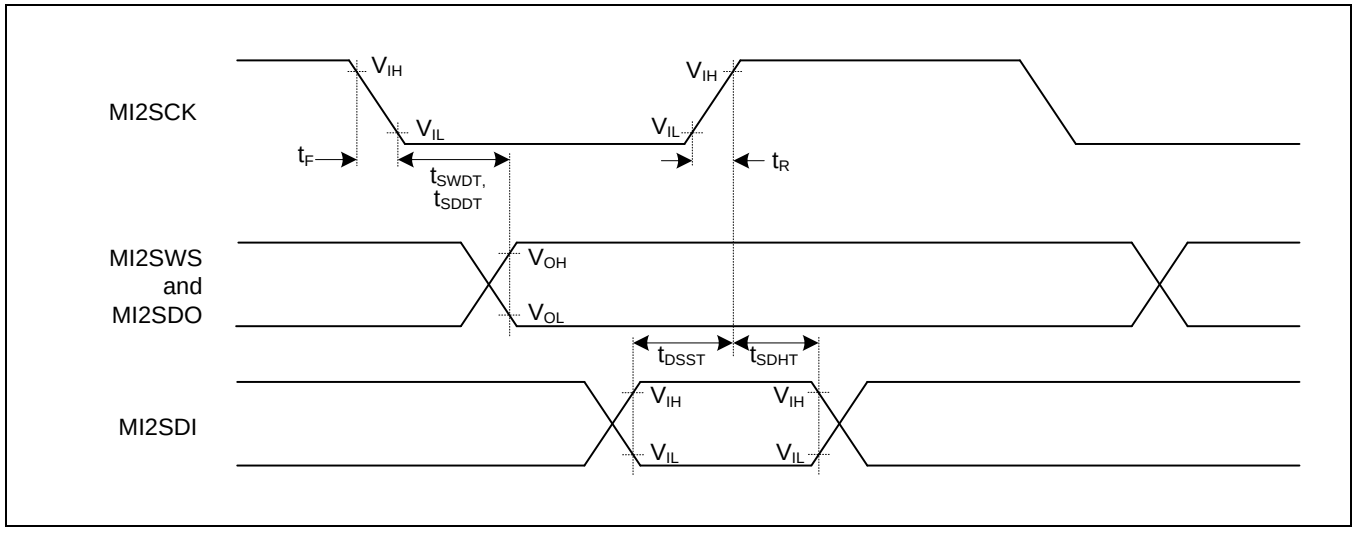


11.4.12 I²S Timing

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

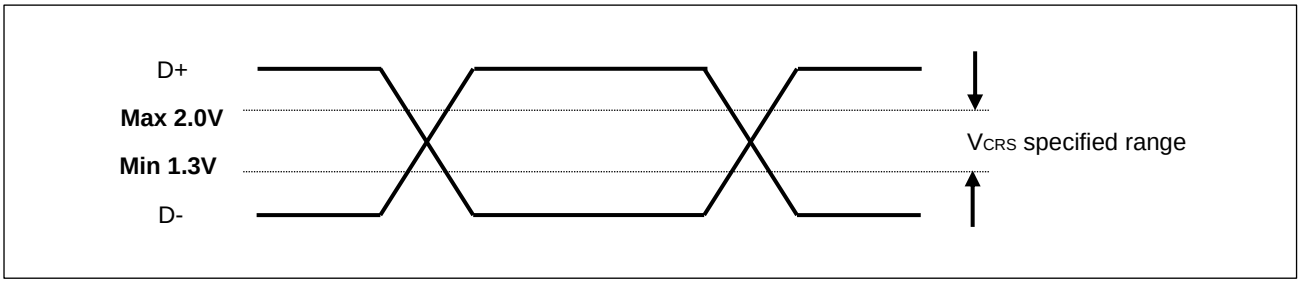
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency*1	f_{MI2SCK}	MI2SCKx	C_L=30 pF	-	6.144	-	6.144	MHz
I²S clock cycle time*1	t_{ICYC}	MI2SCKx		4 t_{CYCP}	-	4 t_{CYCP}	-	ns
I²S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t_{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t_{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t_{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t_{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	t_F	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	t_R	MI2SCKx		-	5	-	5	ns

*1: I²S clock should meet the multiple of PCLK (t_{ICYC}) and the frequency less than f_{MI2SCK} meantime. The detail information please refer to Chapter I²S of Communication Macro Part of Peripheral Manual.

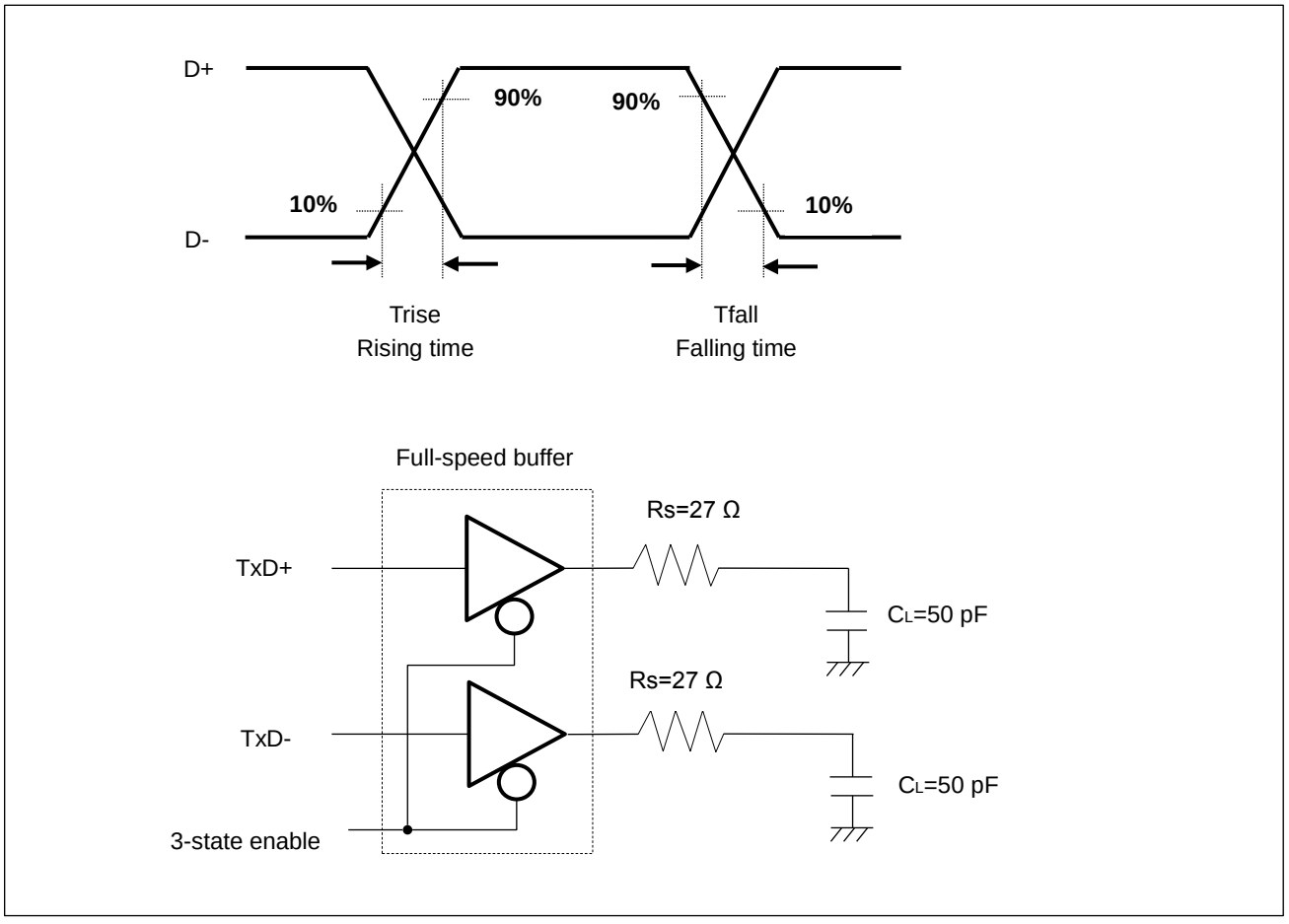


*3 : The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the VSS and 1.5 kΩ load) at high-state (V_{OH})

*4 : The cross voltage of the external differential output signal (D+ / D-) of USB I/O buffer is within 1.3 V to 2.0 V.



*5 : The indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ±10% to minimize RFI emission.



*6 : USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28Ω to 44Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 33 Ω (recommendation value : 27 Ω) series resistor Rs.

11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed*1	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	8160× t_{CYCP}*2	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

*1: The value of low voltage detection reset is always fixed.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.