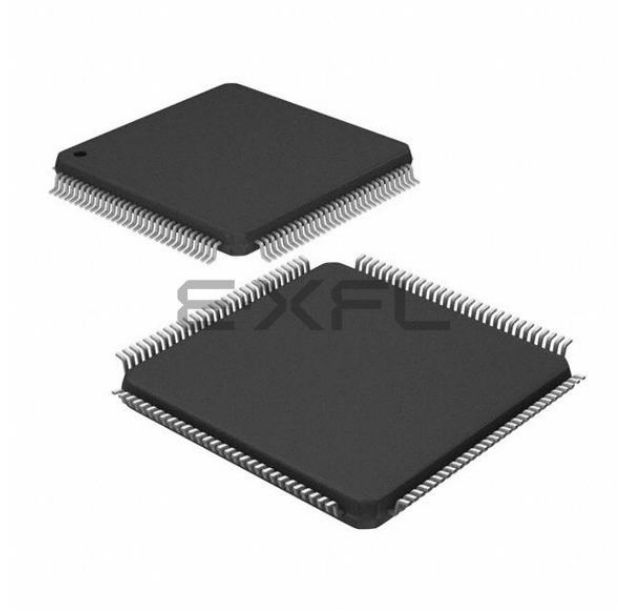

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	102
Program Memory Size	560KB (560K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1b86ghagv20000

2. Packages

Product Name / Package	S6E1B84E/S6E1B86E	S6E1B84F/S6E1B86F	S6E1B84G/S6E1B86G
LQFP: FPT-80P-M21 (0.50 mm pitch)	❍	-	-
LQFP: FPT-100P-M20 (0.50 mm pitch)	-	❍	-
LQFP: FPT-120P-M21 (0.50 mm pitch)	-	-	❍

❍: Available

Note:

- *See "13. Package Dimensions" for detailed information on each package.*

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
12	-	-	P5A SOT7_0 INT16_2	F	J
13	-	-	P5B SCK7_0 INT17_2	F	J
14	9	9	P30 TIOB0_1 SCS60_1 MI2SWS6_1 INT03_2 WKUP4 COM7 SEG43	M	T
15	10	10	P31 TIOB1_1 SCK6_1 MI2SCK6_1 INT04_2 COM6 SEG42	M	S
16	11	11	P32 TIOB2_1 SOT6_1 MI2SDO6_1 INT05_2 COM5 SEG41	M	S
17	12	12	P33 TIOB3_1 SIN6_1 MI2SDI6_1 INT04_0 ADTG_6 COM4 SEG40	M	S
18	13	-	P34 SCS61_1 FRCK0_0 TIOB4_1	I	I
19	14	-	P35 SCS62_1 IC03_0 TIOB5_1 INT08_1 SEG37	L	S
20	15	-	P36 IC02_0 SIN5_2 INT09_1 WKUP11	I	N
21	16	-	P37 IC01_0 SOT5_2 INT10_1	I	J

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
49	44	34	P4C TIOB2_0 SOT7_1 CEC0_0 INT12_0 SEG29	L	R
50	45	35	P4D TIOB3_0 SCK7_1 INT13_0 WKUP6 SEG28	L	T
51	-	-	P70 TIOA4_2 SCS71_1	F	I
52	-	-	P71 TIOB4_2 SCS72_1 INT13_2	F	J
53	-	-	P72 SIN2_0 TIOA6_0 INT14_2	F	J
54	-	-	P73 SOT2_0 TIOB6_0 INT15_2	F	J
55	-	-	P74 SCK2_0	F	I
56	46	36	PE0 MD1	C	D
57	47	37	MD0	J	M
58	48	38	PE2 X0	A	A
59	49	39	PE3 X1	A	B
60	50	40	VSS	-	-
61	51	41	VCC	-	-
62	52	42	P10 IC1_CLK_1 CTS1_1 AN00 SEG27	P	K
63	53	43	P11 IC1_VCC_1 SIN1_1 FRCK0_2 INT02_1 WKUP1 AN01 SEG26	P	W

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
64	54	44	P12 IC1_VPEN_1 SOT1_1 IC00_2 AN02 SEG25	P	K
65	55	45	P13 IC1_RST_1 SCK1_1 RTCCO_1 IC01_2 SUBOUT_1 AN03 SEG24	P	K
66	56	46	P14 IC1_DATA_1 RTS1_1 SIN0_1 IC02_2 INT03_1 AN04 SEG23	P	V
67	57	47	P15 IC1_CIN_1 SOT0_1 IC03_2 INT14_0 AN05 SEG22	P	V
68	58	48	P16 SCK0_1 INT15_0 AN06 SEG21	P	V
69	59	49	P17 SIN2_2 INT04_1 AN07 SEG20	P	V
70	60	50	AVCC	-	-
71	61	51	AVSS	-	-
72	62	52	AVRL	-	-
73	63	53	AVRH	-	-
74	64	54	P18 SOT2_2 AN08 SEG19	P	K
75	65	55	P19 SCK2_2 IC00_1 AN09 SEG18	P	K

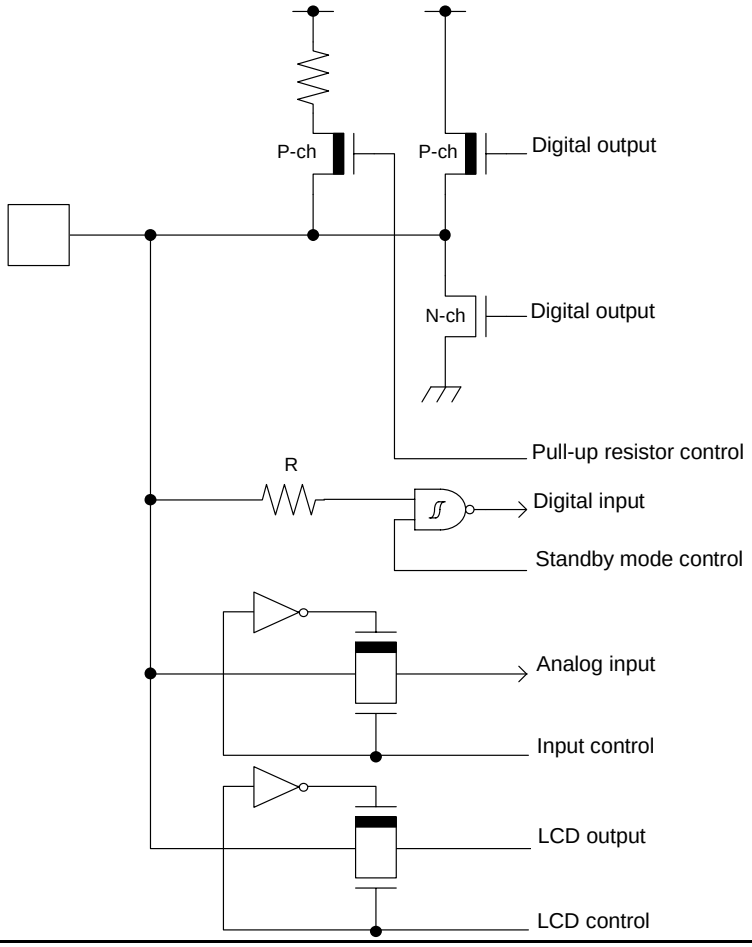
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2
	INT00_1		97	82	-
	INT00_2		102	87	67
	INT01_0	External interrupt request 01 input pin	3	3	3
	INT01_1		98	83	-
	INT02_0	External interrupt request 02 input pin	4	4	4
	INT02_1		63	53	43
	INT02_2		82	-	-
	INT03_0	External interrupt request 03 input pin	113	93	73
	INT03_1		66	56	46
	INT03_2		14	9	9
	INT04_0	External interrupt request 04 input pin	17	12	12
	INT04_1		69	59	49
	INT04_2		15	10	10
	INT05_0	External interrupt request 05 input pin	89	74	-
	INT05_1		76	66	56
	INT05_2		16	11	11
	INT06_0	External interrupt request 06 input pin	23	18	13
	INT06_1		88	73	60
	INT06_2		96	81	65
	INT07_0	External interrupt request 07 input pin	24	19	14
	INT07_1		114	94	74
	INT07_2		5	5	5
	INT08_0	External interrupt request 08 input pin	34	29	-
	INT08_1		19	14	-
	INT08_2		8	8	8
	INT09_0	External interrupt request 09 input pin	35	30	-
	INT09_1		20	15	-
	INT10_0	External interrupt request 10 input pin	36	31	21
	INT10_1		21	16	-
	INT10_2		112	-	-
	INT11_0	External interrupt request 11 input pin	118	98	78
	INT11_1		22	17	-
	INT11_2		110	-	-
	INT12_0	External interrupt request 12 input pin	49	44	34
	INT12_1		32	27	-
	INT12_2		108	-	-
	INT13_0	External interrupt request 13 input pin	50	45	35
	INT13_1		33	28	-
	INT13_2		52	-	-
	INT14_0	External interrupt request 14 input pin	67	57	47
	INT14_1		92	77	61
	INT14_2		53	-	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-
	SIN3_1		2	2	2
	SIN3_2		94	79	63
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I^2C pin (operation mode 4).	109	-	-
	SOT3_1 (SDA3_1)		3	3	3
	SOT3_2 (SDA3_2)		92	77	61
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I^2C pin (operation mode 4).	108	-	-
	SCK3_1 (SCL3_1)		4	4	4
	SCK3_2 (SCL3_2)		96	81	65
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	102	87	67
	SIN4_1		76	66	56
	SIN4_2		97	82	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I^2C pin (operation mode 4).	99	84	66
	SOT4_1 (SDA4_1)		77	67	57
	SOT4_2 (SDA4_2)		98	83	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I^2C pin (operation mode 4).	107	92	72
	SCK4_1 (SCL4_1)		78	68	-
	SCK4_2 (SCL4_2)		99	84	66
	CTS4_0	Multi-function serial interface ch4 CTS input pin	106	91	71
	CTS4_1		79	69	-
	CTS4_2		100	85	-
	RTS4_0	Multi-function serial interface ch4 RTS input pin	105	90	70
	RTS4_1		80	70	-
	RTS4_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 5	SIN5_0 (MI2SDI5_0)	Multi-function serial interface ch.5 input pin. SIN5_0 pin operates as I2SIN5_0 when used as an I^2S pin (operation mode 2).	116	96	76
	SIN5_1		113	-	-
	SIN5_2		20	15	-
	SOT5_0 (SDA5_0) (MI2SDO5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA5 when used as an I^2C pin (operation mode 4). SOT5_0 pin operates as MI2SDO5_0 when used as an I^2S pin (operation mode 2).	115	95	75
	SOT5_1 (SDA5_1)		112	-	-
	SOT5_2 (SDA5_2)		21	16	-
	SCK5_0 (SCL5_0) (MI2SCK5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when used as a CSIO (operation mode 2) and as SCL5 when used as an I^2C pin (operation mode 4). SCK5_0 pin operates as MI2SCK5_0 when used as an I^2S pin (operation mode 2).	114	94	74
	SCK5_1 (SCL5_1)		111	-	-
	SCK5_2 (SCL5_2)		22	17	-
	MI2SWS5_0	I^2S word select (WS) output	113	93	73
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin. SIN6_1 pin operates as I2SIN6_1 when used as an I^2S pin (operation mode 2).	5	5	5
	SIN6_1 (MI2SDI6_1)		17	12	12
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I^2C pin (operation mode 4). SOT6_1 pin operates as MI2SDO6_1 when used as an I^2S pin (operation mode 2).	6	6	6
	SOT6_1 (SDA6_1) (MI2SDO6_1)		16	11	11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I^2C pin (operation mode 4). SCK6_6 pin operates as MI2SCK6_1 when used as an I^2S pin (operation mode 2).	7	7	7
	SCK6_1 (SCL6_1) (MI2SCK6_1)		15	10	10
	SCS60_1	Multi-function serial interface ch.6 serial chip select 0 input/output pin.	14	9	9
	SCS61_1	Multi-function serial interface ch.6 serial chip select 1 input/output pin.	18	13	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 input/output pin.	19	14	-
	MI2SWS6_1	I^2S word select (WS) output	14	9	9

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	REGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

*: PE0 is an open drain pin, cannot output high.

Type	Circuit	Remarks
P		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・5 V tolerant ・LCD segment output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

> CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:
>
> (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
>
> (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
L level maximum output current*4	I_{OL}	-	10	mA	
			39	mA	P0B / P0C
L level average output current*5	I_{OLAV}	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	I_{OH}	-	- 10	mA	
			- 39	mA	P0B / P0C
H level average output current*5	I_{OHAV}	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	250	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0 V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not to exceed V_{CC} + 0.5 V at power-on.

*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

*7: When P0C/UDP0 and P0B/UDM0 pins are used as GPIO (P0C, P0B).

*8: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

<WARNING>

- *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

11.3 DC Characteristics

11.3.1 Current Rating

Symbol (Pin Name)	Conditions		HCLK Frequency[*4]	Value Typ[*1]	Value Max[*2]	Unit	Remarks
I_{CC} (VCC)	Run mode, code executed from Flash	4 MHz external clock input, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.7	TBD	mA	*3
			8 MHz	1.15	TBD		
			20 MHz	2.25	TBD		
			40 MHz	4.5	TBD		
		4 MHz external clock input, PLL ON[*8] Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4 MHz	0.75	TBD	mA	*3
			8 MHz	1.25	TBD		
			20 MHz	2.5	TBD		
			40 MHz	5.0	TBD		
		4 MHz crystal oscillation, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.8	TBD	mA	*3
			8 MHz	1.4	TBD		
			20 MHz	2.75	TBD		
			40 MHz	5.5	TBD		
	Run mode, code executed from RAM	4 MHz external clock input, PLL ON[*8] NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.2	TBD		
			20 MHz	2.4	TBD		
			40 MHz	4.8	TBD		
	Run mode, code executed from Flash	4 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHz	2.6	TBD	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR[*5] NOP code executed All peripheral clock stopped by CKENx	4 MHz	1.2	TBD	mA	*3
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHz	96	TBD	µA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHz	120	TBD	µA	*3
I_{CCS} (VCC)	Sleep operation	4 MHz external clock input, PLL ON[*8] All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.1	TBD		
			20 MHz	1.9	TBD		
			40 MHz	3.2	TBD		
		Built-in high speed CR[*5] All peripheral clock stopped by CKENx	4 MHz	0.5	TBD	mA	*3
		32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHz	94	TBD	µA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100 kHz	105	TBD	µA	*3

*1 : T_A=+25°C,V_{CC}=3.3 V
*2 : T_A=+105°C,V_{CC}=3.6 V
*3 : All ports are fixed
*4 : PCLK0 is set to divided rate 8
*5 : The frequency is set to 4 MHz by trimming
*6 : Flash sync down is set to FRWTR.RWT=11 and FSYNDN.SD=1111
*7 : VCC=1.65 V
*8 : When HCLK=4 MHz, PLL OFF

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCH} (VCC)	Stop mode	T_A=25°C V_{CC}=3.3 V	10	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V	9	TBD	µA	*1
			T_A=105°C V_{CC}=3.6 V	-	TBD	µA	*1
	I_{CCT} (VCC)	Sub timer mode	T_A=25°C V_{CC}=3.3 V 32 kHz Crystal oscillation	13	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V 32 kHz Crystal oscillation	12	TBD	µA	*1
			T_A=105°C V_{CC}=3.6 V 32 kHz Crystal oscillation	-	TBD	µA	*1
	I_{CCR} (VCC)	RTC mode	T_A=25°C V_{CC}=3.3 V 32 kHz Crystal oscillation	10.5	TBD	µA	*1
			T_A=25°C V_{CC}=1.65 V 32 kHz Crystal oscillation	9.5	TBD	µA	*1
			T_A=105°C V_{CC}=3.6 V 32 kHz Crystal oscillation	-	TBD	µA	*1

*1: All ports are fixed. LVD off. Flash off.

LVD Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	TBD	µA	For occurrence of reset
				0.13	TBD	µA	For occurrence of interrupt

Flash Memory Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	TBD	mA	

A/D converter Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	TBD	mA	
			At stop	0.13	TBD	µA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	TBD	mA	AVRH=3.6 V
			At stop	0.1	TBD	µA	

11.4.3 Built-in CR Oscillation Characteristics

Built-in High-Speed CR

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS} =AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_A = -20°C to +85°C	3.96	4	4.04	MHz	During trimming*1
		T_A = -40°C to +105°C	3.92	4	4.08		
		T_A = - 40°C to +105°C	2.6	4	5.2		Not during trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2
					300	µs	If TRT is changed.*2

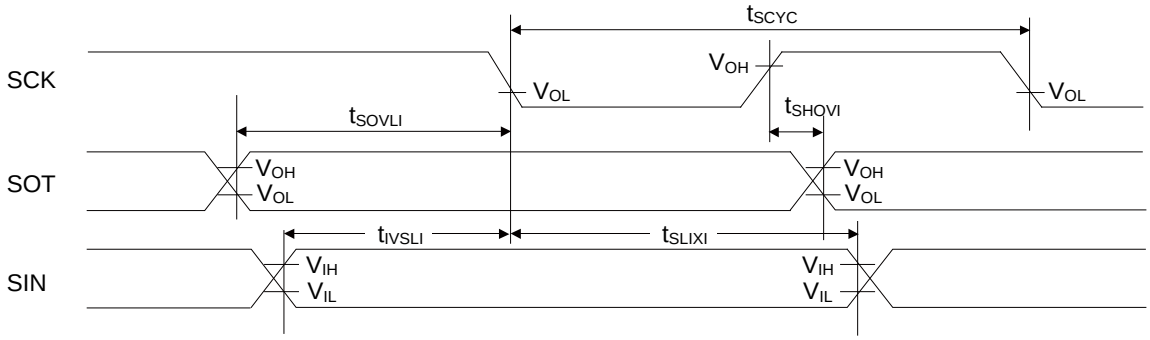
*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock.
After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

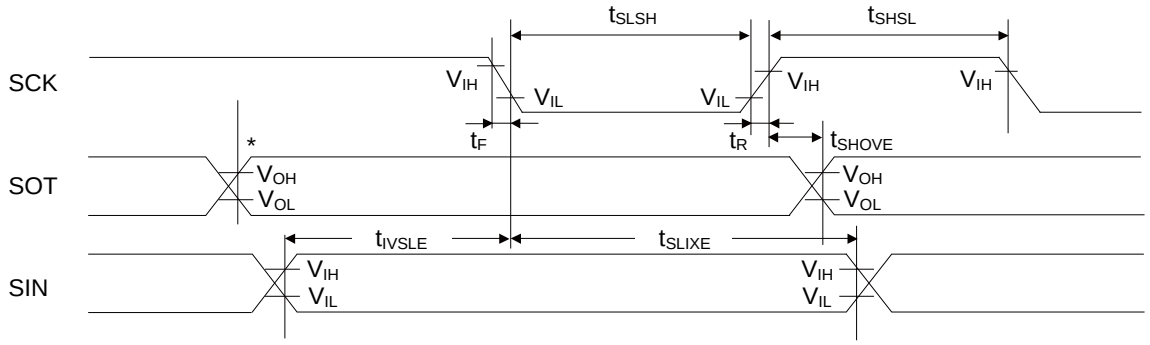
Built-in Low-Speed CR

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	



Master mode



Slave mode

*: Changes when writing to TDR register

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}=AV_{CC}=1.65 V to 3.6 V, V_{SS}=AV_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	43	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram ".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

11.4.13 Smart Card Interface Characteristics

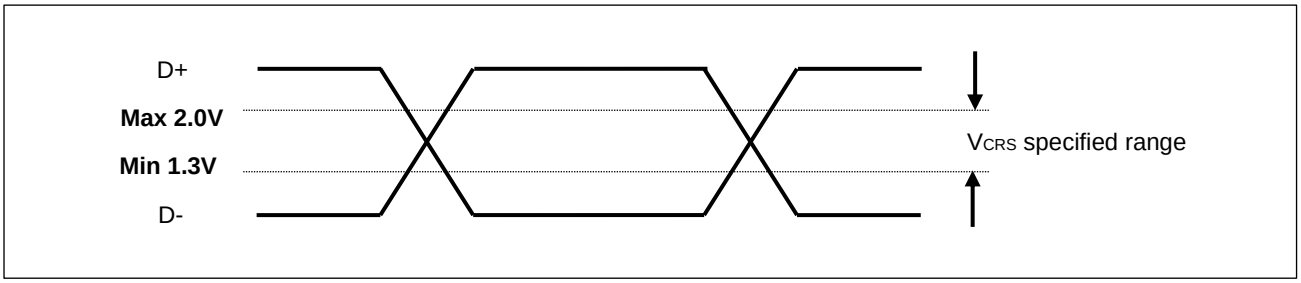
(V_{CC}=1.65 V to 3.3 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t_R	ICx_VCC, ICx_RST, ICx_CLK, ICx_DATA	C_L=30 pF	4	20	ns	
Output falling time	t_F			4	20	ns	
Output clock frequency	f_{CLK}	ICx_CLK		-	20	MHz	
Duty cycle	Δ			45%	55%		

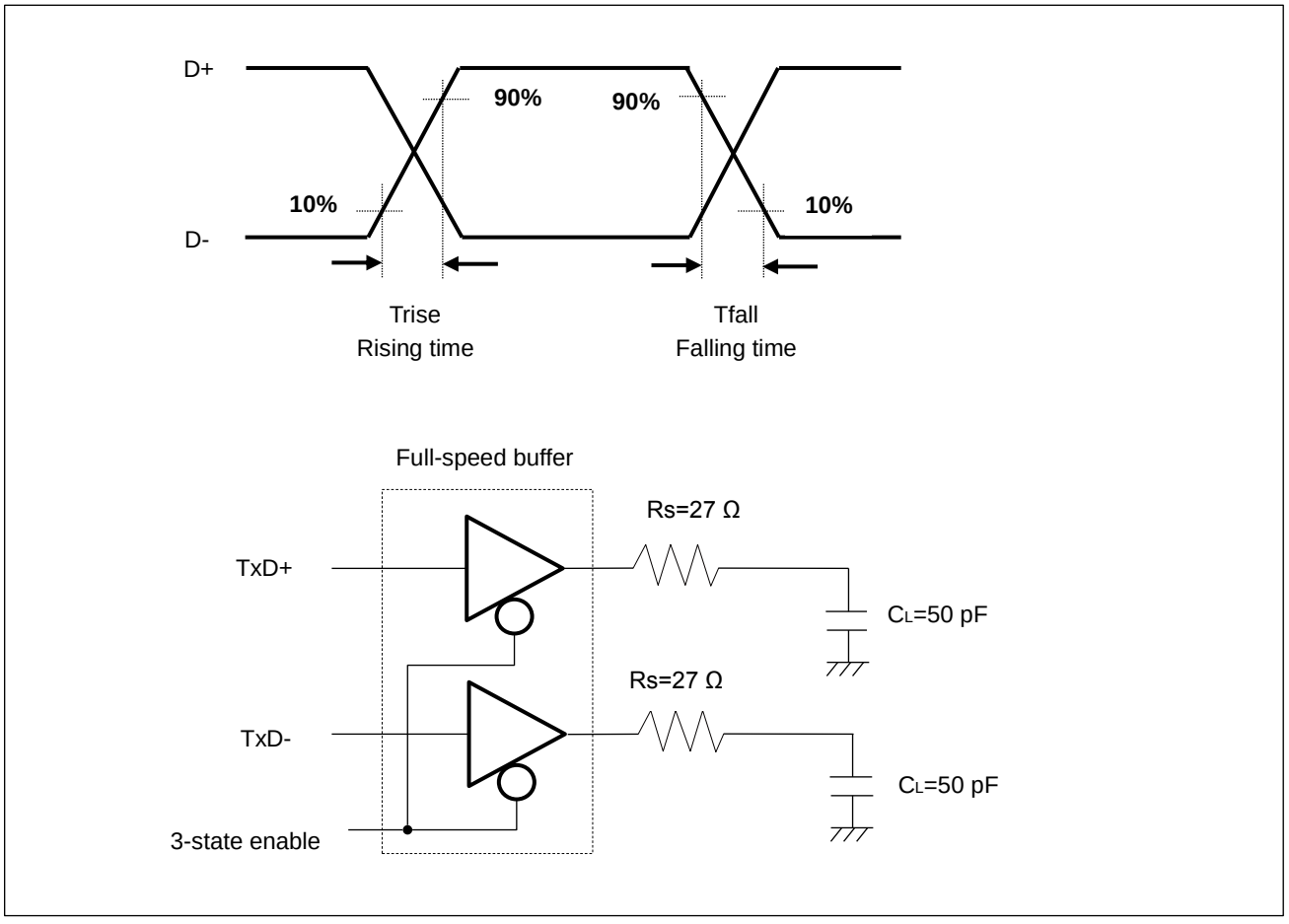
■External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx_CIN pin when it's used as smart card reader function.

*3 : The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the VSS and 1.5 kΩ load) at high-state (V_{OH})

*4 : The cross voltage of the external differential output signal (D+ / D-) of USB I/O buffer is within 1.3 V to 2.0 V.



*5 : The indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ±10% to minimize RFI emission.



*6 : USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28Ω to 44Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 33 Ω (recommendation value : 27 Ω) series resistor Rs.