Lattice Semiconductor Corporation - LAE5U-12F-7BG381E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1500
Number of Logic Elements/Cells	12000
Total RAM Bits	589824
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.04V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae5u-12f-7bg381e

Contents

Tables

2.2.1. Slice

Each slice contains two LUT4s feeding two registers. In Distributed SRAM mode, Slice 0 through Slice 2 are configured as distributed memory, and Slice 3 is used as Logic or ROM. Table 2.1 shows the capability of the slices along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. There is control logic to perform set/reset functions, which can be programmed as synchronous/asynchronous, clock select, chip-select, and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU (Used in Distributed SRAM)		PFU (Not used as Distributed SRAM)	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	RAM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals: 13 signals from routing and 1 signal from the carry-chain routed from the adjacent slice or PFU. There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7, and LUT8. Table 2.2 and Figure 2.3 list the signals associated with all the slices. Figure 2.4 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7, and LUT8.

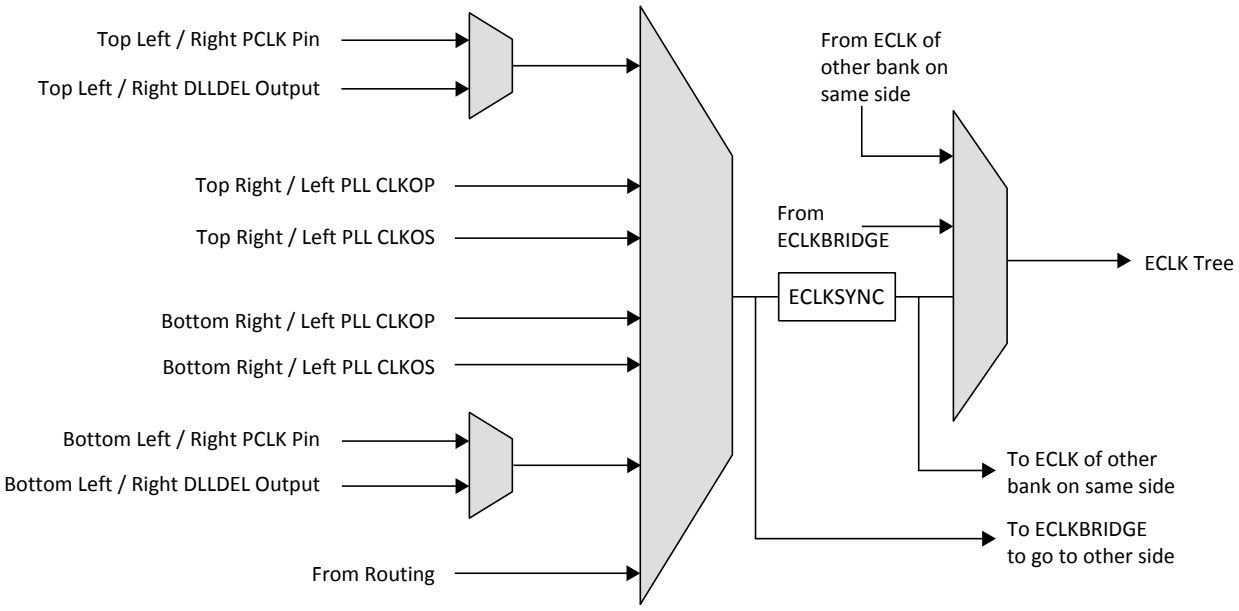


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide.

2.11. Clock Dividers

ECP5 Automotive devices have two clock dividers, one on the left side and the other on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal.

The clock dividers can be fed from selected PLL outputs, external primary clock pins multiplexed with the DDRDEL Slave Delay or from routing. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The SLIP signal slips the outputs one cycle relative to the input clock. For further information on clock dividers, refer to TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide. Figure 2.9 shows the clock divider connections.

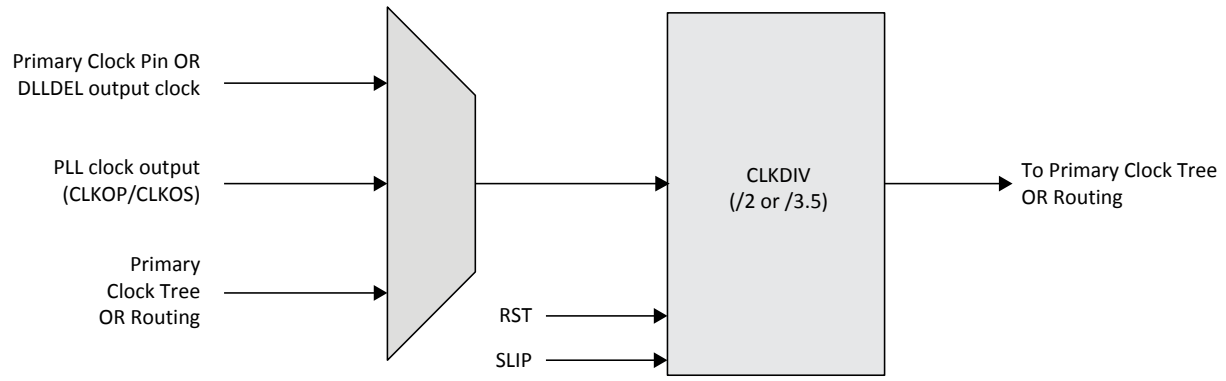


Figure 2.9. ECP5 Automotive Clock Divider Sources

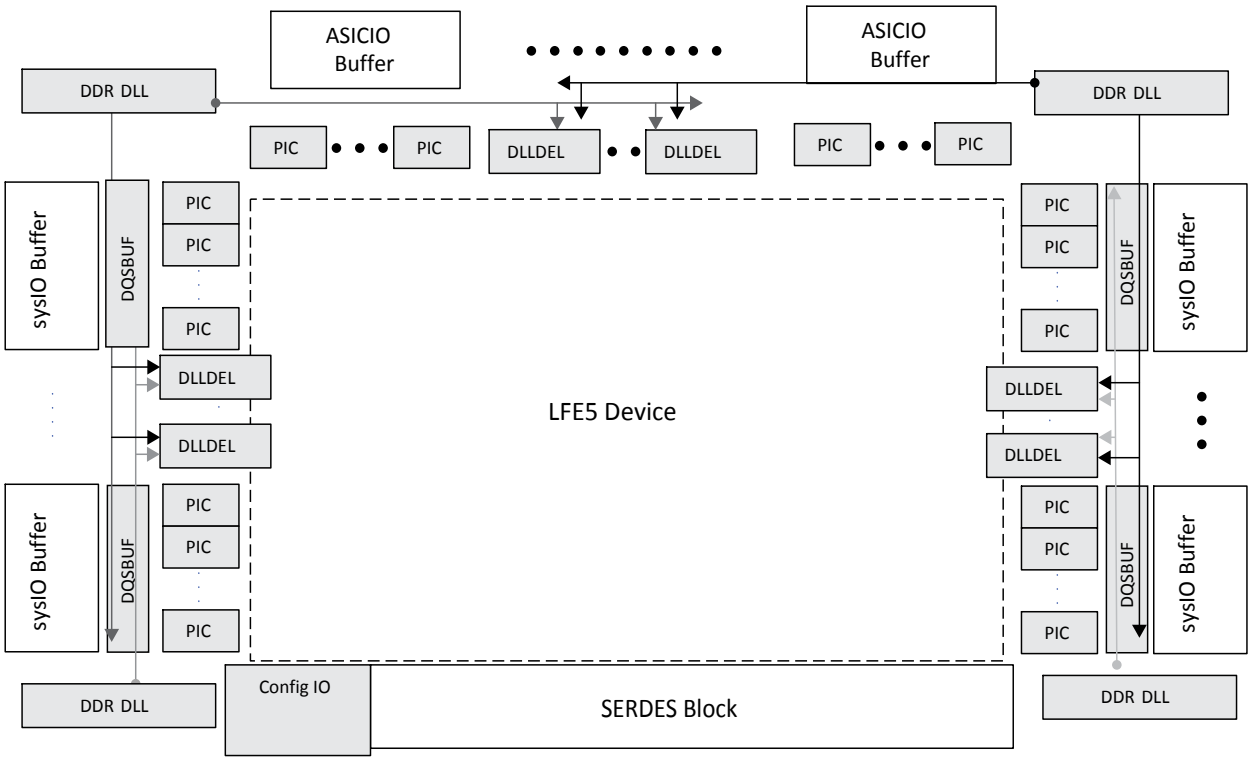


Figure 2.11. ECP5 Automotive DLL Top Level View for LFE-45

2.13. sysMEM Memory

ECP5 Automotive devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM, and FIFO buffers via external PFUs.

2.13.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 23. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to TN1264, ECP5 and ECP5-5G Memory Usage Guide.

2.14. sysDSP™ Slice

The ECP5 Automotive family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.14.1. sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. In the ECP5 Automotive device family, there are many DSP slices that can be used to support different data widths. This allows designers to use highly parallel implementations of DSP functions. Designers can optimize DSP performance vs. area by choosing appropriate levels of parallelism. Figure 2.13 compares the fully serial implementation to the mixed parallel and serial implementation.

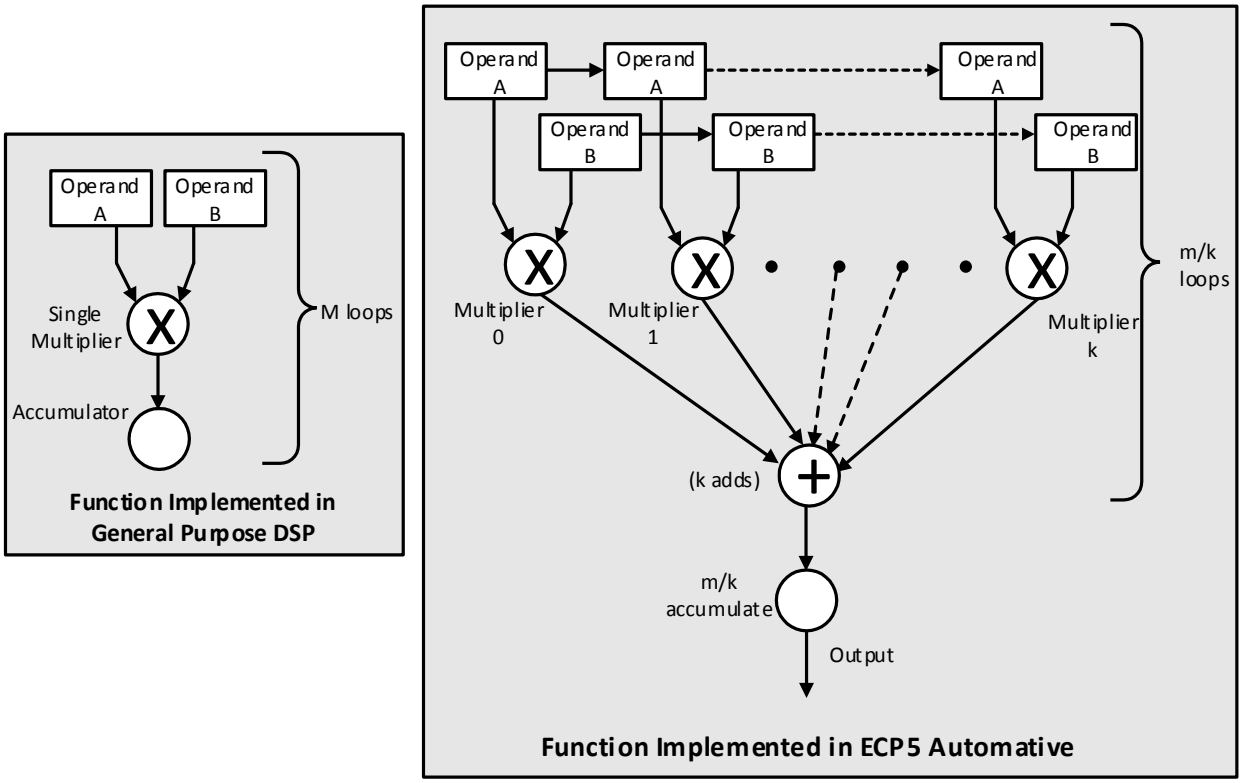


Figure 2.13. Comparison of General DSP and ECP5 Automotive Approaches

2.17.1.1. Input FIFO

The ECP5 Automotive PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section on page 34.

Table 2.8. Input Block Port

Name	Type	Description
D	Input	High speed data input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low speed data to the device core
RST	Input	Reset to the output block
SCLK	Input	Slow speed system clock
ECLK	Input	High speed edge clock
DQS	Input	Clock from DQS control block used to clock DDR memory data
ALIGNWD	Input	Data alignment signal from device core

2.17.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

ECP5 Automotive output data path has output programmable flip flops and output gearing logic. On the left and right sides the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks will support 1x gearing. ECP5 Automotive output data path diagram is shown in Figure 2.19. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

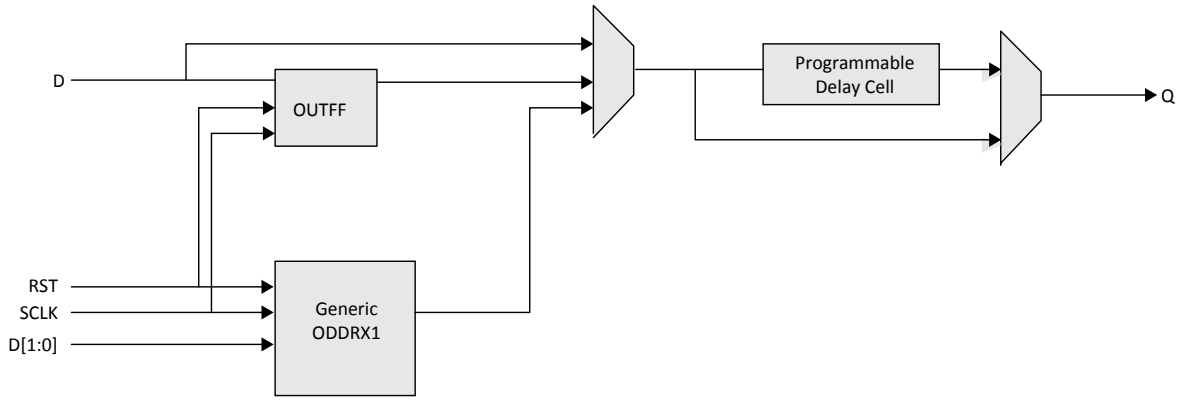


Figure 2.19. Output Register Block on Top Side

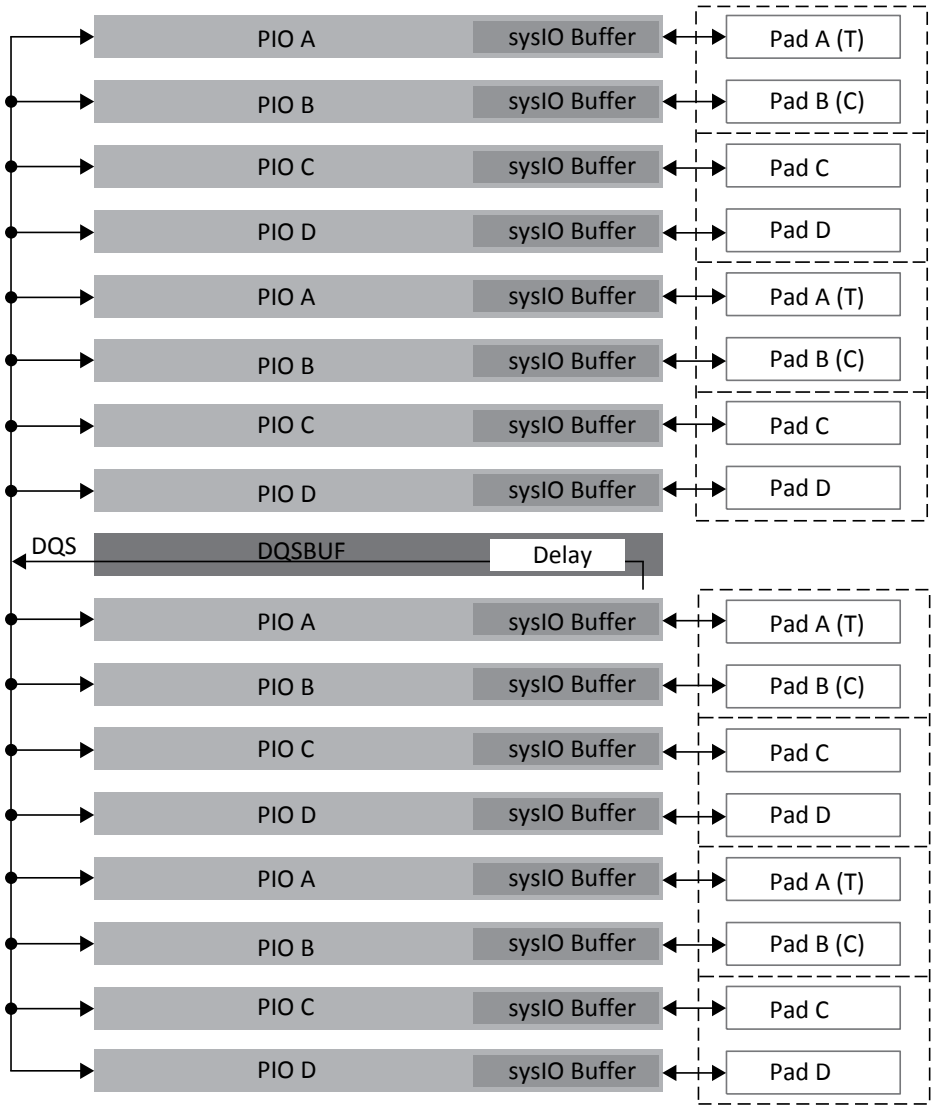


Figure 2.23. DQS Grouping on the Left and Right Edges

2.19.2. DLL Calibrated DQS Delay and Control Block (DQSBUF)

To support DDR memory interfaces, DDR2/3, LPDDR2/3, the DQS strobe signal from the memory must be used to capture the data DQ in the PIC registers during memory reads. This signal is output from the DDR memory device aligned to data transitions and must be time shifted before it can be used to capture data in the PIC. This time shifting is achieved by using DQSDEL programmable delay line in the DQS Delay Block. The DQSDEL is implemented as a slave delay line and works in conjunction with a master DDRDLL.

This block also includes slave delay line to generate delayed clocks used in the write side to generate DQ and DQS with correct phases within one DQS group. There is a third delay line inside this block used to provide write leveling feature for DDR write if needed.

Each of the read or write side delays can be dynamically shifted using margin control signals that can be controlled by the core logic.

FIFO Control Block included here generates the Read and Write Pointers for the FIFO block inside the Input Register Block. These pointers are generated to control the DQS to ECLK domain crossing using the FIFO module.

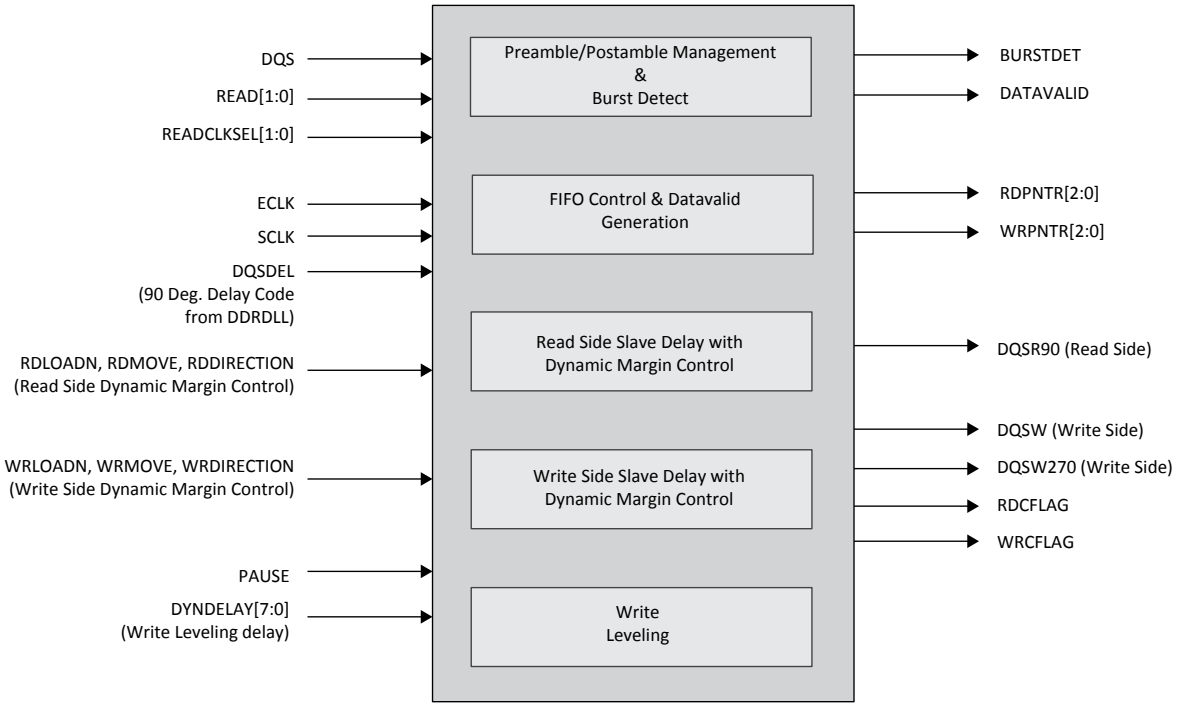


Figure 2.24. DQS Control and Delay Block (DQSBUF)

Table 2.11. DQSBUF Port list description

Name	Type	Description
DQS	Input	DDR memory DQS strobe
READ[1:0]	Input	Read Input from DDR controller
READCLKSEL[1:0]	Input	Read pulse selection
SCLK	Input	Slow system clock
ECLK	Input	High speed edge clock with the same frequency as that of the DDR memory)
DQSDEL	Input	90-degree delay code from DDRDLL
RDLOADN, RDMOVE, RDDIRECTION	Input	Dynamic margin control ports for Read delay
WRLOADN, WRMOVE, WRDIRECTION	Input	Dynamic margin control ports for Write delay
PAUSE	Input	Used by DDR controller to pause write side signals during DDRDLL code update or Write leveling
DYNDELAY[7:0]	Input	Dynamic Write leveling delay control
DQSR90	Output	90-degree delay DQS used for Read
DQSW270	Output	90-degree delay clock used for DQ Write
DQSW	Output	Clock used for DQS Write
RDPNTR[2:0]	Output	Read pointer for IFIFO module
WRPNTR[2:0]	Output	Write pointer for IFIFO module
DATAVALID	Output	Signal indicating start of valid data
BURSTDET	Output	Burst detect indicator
RDFLAG	Output	Read dynamic margin control output to indicate max value
WRFLAG	Output	Write dynamic margin control output to indicate max value

2.20. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTL, LVPECL, and MIPI.

2.20.1. sysI/O Buffer Banks

ECP5 Automotive devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank, Bank 8, is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O.

In ECP5 Automotive devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage V_{CCIO}. In addition, the banks on the Left or Right side of the device, have voltage reference input, V_{REF1} per bank, which allow it to be completely independent of each other. This voltage reference input is a shared I/O pin. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5 Automotive devices, single-ended output buffers and ratioed input buffers, LVTTL, and LVCMOS, are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25, and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

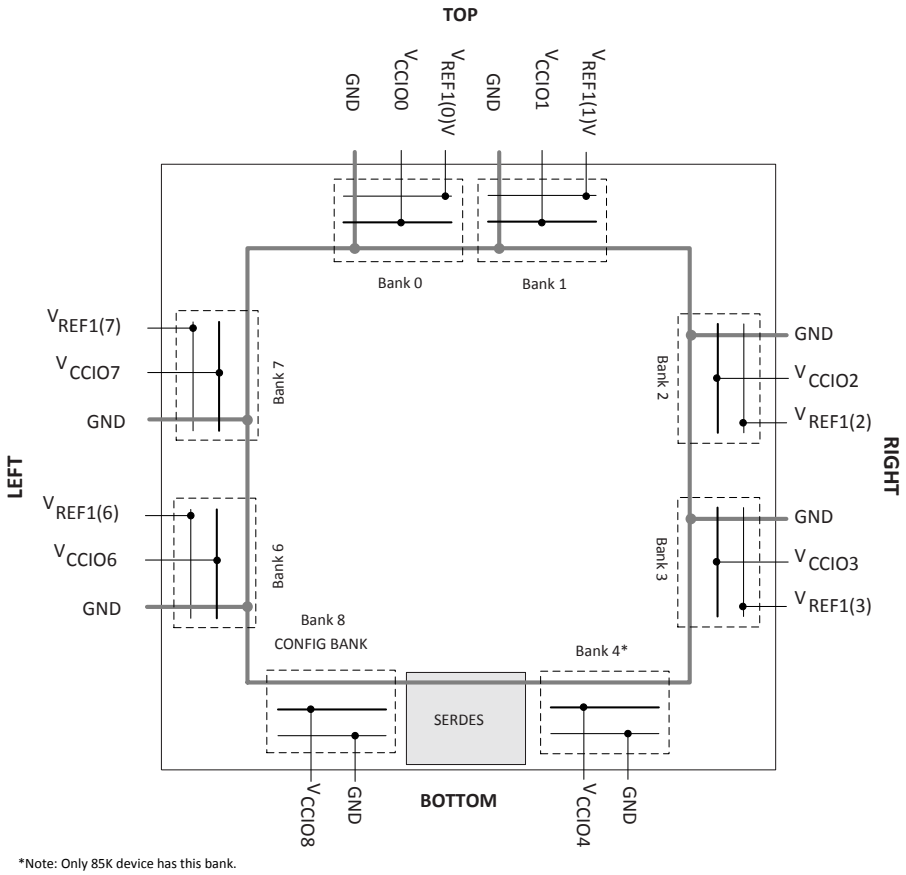
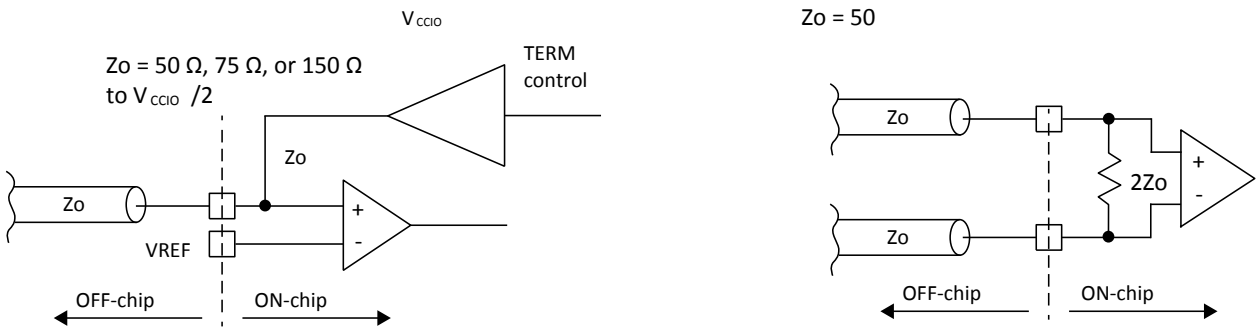


Figure 2.25. ECP5 Automotive Device Family Banks

2.20.4. On-Chip Programmable Termination

The ECP5 Automotive devices support a variety of programmable on-chip terminations options including:

- Dynamically switchable Single-ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.



Parallel Single-Ended Input **Differential Input**

Figure 2.26. On-chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2$*	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Note**:

TERMINATE to single-ended $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance ±20%.

Refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide for on-chip termination usage and value ranges.

2.20.5. Hot Socketing

ECP5 Automotive devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the Hot Socketing Specifications section on page 47.

There are some restrictions to be aware of when using spread spectrum clocking. When a dual shares a PCI Express x1 channel with a non-PCI Express channel, ensure that the reference clock for the dual is compatible with all protocols within the dual. For example, a PCI Express spread spectrum reference clock is not compatible with most Gigabit Ethernet applications because of tight CTC ppm requirements.

While the LAE5UM architecture will allow the mixing of a PCI Express channel and a Gigabit Ethernet, or SGMII channel within the same dual, using a PCI Express spread spectrum clocking as the transmit reference clock will cause a violation of the Gigabit Ethernet, and SGMII transmit jitter specifications.

For further information on SERDES, refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide.

2.23. IEEE 1149.1-Compliant Boundary Scan Testability

All ECP5 Automotive devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port uses V_{CCIO8} for power supply.

For more information, refer to TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide.

2.24. Device Configuration

All ECP5 Automotive devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port, support dual-byte, byte, and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are dedicated pins for TAP and sysConfig support, which are TDI, TDO, TCK, TMS, CFG[2:0], PROGRAMN, DONE, INITN, and CCLK. The remaining sysCONFIG pins are used as dual function pins. Refer to TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure an ECP5 Automotive device:

- JTAG
- Standard Serial Peripheral Interface (SPI) to boot PROM Support x1, x2, x4 wide SPI memory interfaces.
- System microprocessor to drive a x8 CPU port in Slave Parallel Configuration Mode (SPCM) mode.
- System microprocessor to drive a serial slave SPI port (SSPI mode).
- Slave Serial Configuration Mode (SCM)

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

ECP5 Automotive devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

2.24.1. Enhanced Configuration Options

ECP5 Automotive devices have enhanced configuration features such as: decryption support, decompression support, TransFR™ I/O, and dual-boot and multi-boot image support.

TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice Semiconductor technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. Refer to TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.

3.12. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide.
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power.
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide for details.

Table 3.20. ECP5 Automotive External Switching Characteristics *(Continued)*

Parameter	Description	Device	–6		Unit
			Min	Max	
f_{DATA_DDR2} f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	624	Mb/s
f_{MAX_DDR2} f_{MAX_DDR3} f_{MAX_DDR3L} f_{MAX_LPDDR2} f_{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	312	MHz
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 WRITE (DQ Output Data are Centered to DQS)					
t_{DQVBS_DDR2} t_{DQVBS_DDR3} t_{DQVBS_DDR3L} t_{DQVBS_LPDDR2} t_{DQVBS_LPDDR3}	Data Output Valid before DQS Output	All Devices	—	-0.25	UI
t_{DQVAS_DDR2} t_{DQVAS_DDR3} t_{DQVAS_DDR3L} t_{DQVAS_LPDDR2} t_{DQVAS_LPDDR3}	Data Output Valid after DQS Output	All Devices	0.25	—	UI
f_{DATA_DDR2} f_{DATA_DDR3} f_{DATA_DDR3L} f_{DATA_LPDDR2} f_{DATA_LPDDR3}	DDR Memory Data Rate	All Devices	—	624	Mb/s
f_{MAX_DDR2} f_{MAX_DDR3} f_{MAX_DDR3L} f_{MAX_LPDDR2} f_{MAX_LPDDR3}	DDR Memory CLK Frequency (ECLK)	All Devices	—	312	MHz

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Diamond software.
2. General I/O timing numbers are based on LVCMOS 2.5, 12 mA, Fast Slew Rate, 0pf load.
   Generic DDR timing are numbers based on LVDS I/O.
   DDR2 timing numbers are based on SSTL18.
   DDR3 timing numbers are based on SSTL15.
   LPDDR2 and LPDDR3 timing numbers are based on HSUL12.
3. Uses LVDS I/O standard for measurements.
4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
5. All numbers are generated with the Diamond software.

3.20. SERDES High-Speed Data Transmitter

Table 3.22. Serial Output Timing and Levels

Symbol	Description	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Peak-Peak Differential voltage on selected amplitude[1, 2]	–25%	—	25%	mV, p-p
$V_{TX-CM-DC}$	Output common mode voltage	—	V_{CCHTX} / 2	—	mV, p-p
T_{TX-R}	Rise time (20% to 80%)	50	—	—	ps
T_{TX-F}	Fall time (80% to 20%)	50	—	—	ps
$T_{TX-CM-AC-P}$	RMS AC peak common-mode output voltage	—	—	20	mV
Z_{TX_SE}	Single ended output impedance for 50/75 Ω	–20%	50/75	20%	Ω
	Single ended output impedance for 6K Ω	–25%	6K	25%	Ω
RL_{TX_DIFF}	Differential return loss with package included [3]	—	—	–10	dB
RL_{TX_COM}	Common mode return loss with package included [3]	—	—	–6	dB

Notes:

1. Measured with 50 Ω Tx Driver impedance at V_{CCHTX}±5%.
2. Refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide for settings of Tx amplitude.
3. Return los = −10 dB (differential), –6 dB (common mode) for 100 MHz ≤ f <= 1.6 GHz with 50 Ω output impedance configuration. This includes degradation due to package effects.

Table 3.23. Channel Output Jitter

Description	Frequency	Min	Typ	Max	Unit
Deterministic	3.125 Gb/s	—	—	0.17	UI, p-p
Random	3.125 Gb/s	—	—	0.25	UI, p-p
Total	3.125 Gb/s	—	—	0.35	UI, p-p
Deterministic	2.5 Gb/s	—	—	0.17	UI, p-p
Random	2.5 Gb/s	—	—	0.20	UI, p-p
Total	2.5 Gb/s	—	—	0.35	UI, p-p
Deterministic	1.25 Gb/s	—	—	0.10	UI, p-p
Random	1.25 Gb/s	—	—	0.22	UI, p-p
Total	1.25 Gb/s	—	—	0.24	UI, p-p

Note:

Values are measured with PRBS 2^7-1, all channels operating, FPGA logic active, I/Os around SERDES pins quiet, reference clock @ 10X mode.

3.22. SERDES High-Speed Data Receiver

Table 3.25. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss without package	—	—	–10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.26. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Note:

Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.

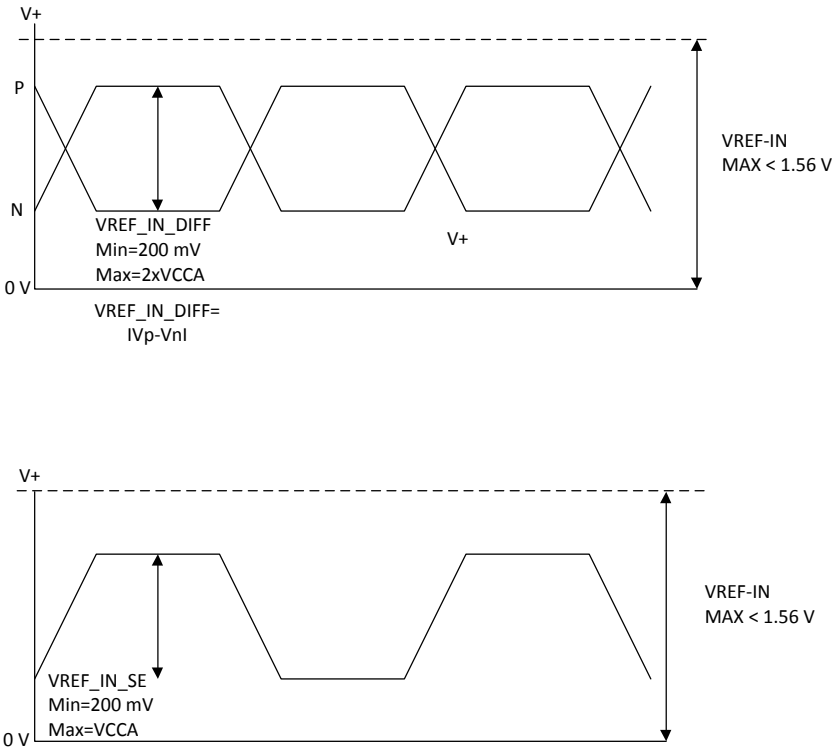
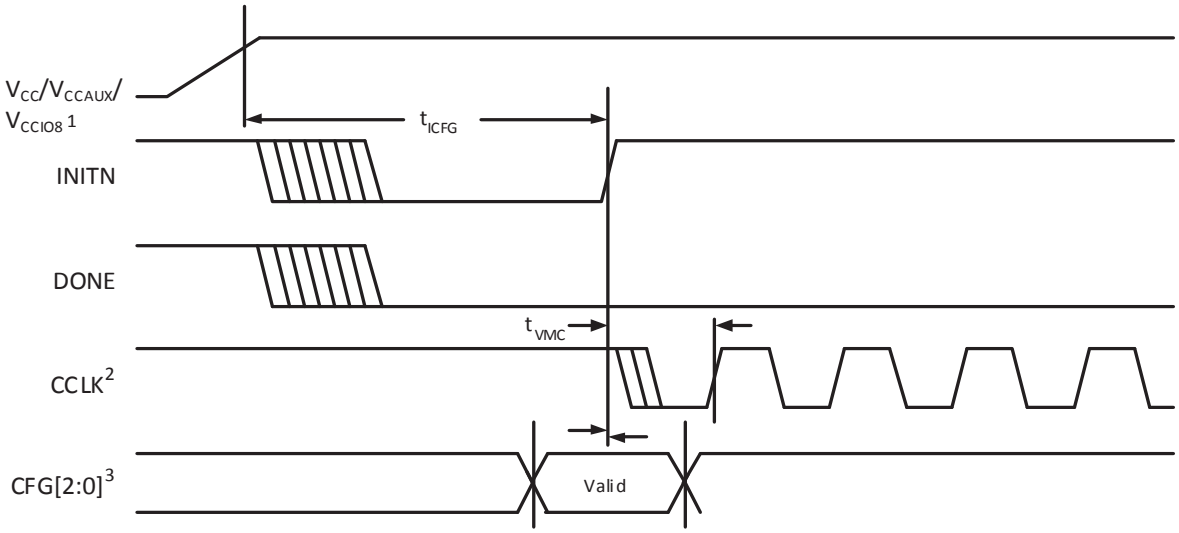


Figure 3.14. SERDES External Reference Clock Waveforms



Notes:
1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hardwired).

Figure 3.18. Power-On-Reset (POR) Timing

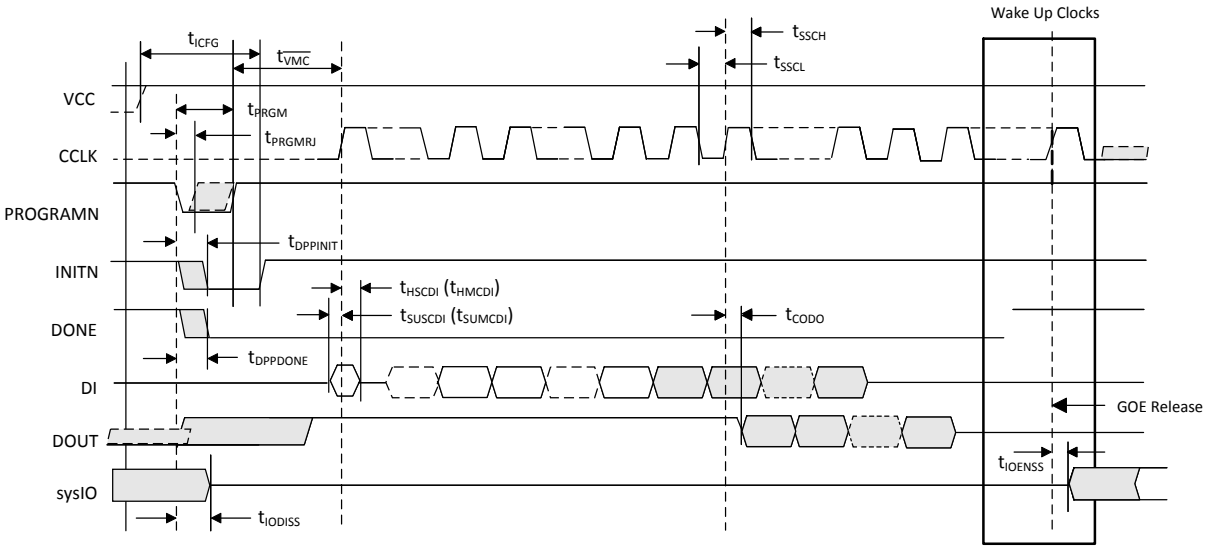


Figure 3.19. sysCONFIG Port Timing

4.3. Pin Information Summary

4.3.1. LAE5UM

Pin Information Summary		LAE5UM -25	LAE5UM-45
Pin Type		**381 caBGA**	**381 caBGA**
General Purpose Inputs/Outputs per Bank	Bank 0	24	27
	Bank 1	32	33
	Bank 2	32	32
	Bank 3	32	33
	Bank 4	0	0
	Bank 6	32	33
	Bank 7	32	32
	Bank 8	13	13
Total Single-Ended User I/O		197	203
V_{CC}		20	20
V_{CCAUX} (Core)		4	4
V_{CCIO}	Bank 0	2	2
	Bank 1	2	2
	Bank 2	3	3
	Bank 3	3	3
	Bank 4	0	0
	Bank 6	3	3
	Bank 7	3	3
	Bank 8	2	2
TAP		4	4
Miscellaneous Dedicated Pins		7	7
GND		59	59
NC		8	2
Reserved		2	2
SERDES		28	28
V_{CCA} (SERDES)	V_{CCA0}	2	2
	V_{CCA1}	2	2
V_{CCAUX} (SERDES)	$V_{CCAUXA0}$	2	2
	$V_{CCAUXA1}$	2	2
GNDA (SERDES)	—	26	26
Total Balls	—	381	381
High Speed Differential Input / Output Pairs	Bank 0	0	0
	Bank 1	0	0
	Bank 2	16/8	16/8
	Bank 3	16/8	16/8
	Bank 4	0	0
	Bank 6	16/8	16/8
	Bank 7	16/8	16/8
	Bank 8	0	0

Supplemental Information

For Further Information

A variety of technical notes for the ECP5 Automotive family are available.

- TN1184, LatticeECP3, ECP-5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide
- TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide
- TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide
- TN1262, ECP5 and ECP5-5G sysIO Usage Guide
- TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide
- TN1264, ECP5 and ECP5-5G Memory Usage Guide
- TN1265, ECP5 and ECP5-5G High-Speed I/O Interface
- TN1266, Power Consumption and Management for ECP5 and ECP5-5G Devices
- TN1267, ECP5 and ECP5-5G sysDSP Usage Guide

For further information on interface standards, refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL): www.jedec.org
- PCI: www.pcisig.com

Revision History

Date	Version	Section	Change Summary
September 2016	1.0	All	Initial preliminary release.