Lattice Semiconductor Corporation - LAE5UM-25F-6BG381E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.04V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae5um-25f-6bg381e

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1. General Description

The ECP5 Automotive family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5 Automotive device family covers look-up-table (LUT) capacity to 44K logic elements and supports up to 203 user I/Os. The ECP5 Automotive device family also offers up to 72 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5 Automotive FPGA fabric is optimized to reach high performance with low power and low cost in mind. The ECP5 Automotive devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5 Automotive device family supports a broad range of interface standards, including DDR2/3, LPDDR2/3, XGMII and 7:1 LVDS.

The ECP5 Automotive device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE, XAUI, and SGMII), and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5 Automotive devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

The Lattice Semiconductor Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5 Automotive FPGA family. Synthesis library support for ECP5 Automotive devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5 Automotive device.

The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for the ECP5 Automotive family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of the design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 44K LUTs
  - 197 to 203 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, XAUI, and SGMII,), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 1.944 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 351K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
  - Four DLLs and four PLLs in LAE5-45; two DLLs and two PLLs in LAE5-25 and LAE5-12
- Pre-engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices

2. Architecture

2.1. Overview

Each ECP5 Automotive device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing slices, as shown in Figure 2.1. LAE5-45 devices have two rows. Both LAE5-25 and LAE5-12 devices have one row. In addition, the LAE5UM devices contain SERDES Duals on the bottom of the device.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM, and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array.

The ECP5 Automotive devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large, dedicated 18 Kb fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths as RAM or ROM. In addition, ECP5 Automotive devices contain up to three rows of DSP slices. Each DSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The ECP5 Automotive devices feature up to four embedded 3.2 Gb/s SERDES (Serializer/Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding/decoding, polarity adjust and elastic buffer logic. Each group of two SERDES channels, along with its Physical Coding Sublayer (PCS) block, creates a dual DCU (Dual Channel Unit). The functionality of the SERDES/PCS duals can be controlled by SRAM cell settings during device configuration or by registers that are addressable during device operation. The registers in every dual can be programmed via the SERDES Client Interface (SCI). These DCUs (up to two) are located at the bottom of the devices.

Each PIC block encompasses two PIOs, PIO pair, with their respective sysI/O buffers. The sysI/O buffers of the ECP5 Automotive devices are arranged in seven banks allowing the implementation of a wide variety of I/O standards. One of these banks (Bank 8) is shared with the programming interfaces. 50% of the PIO pairs on the left and right edges of the device can be configured as LVDS transmit pairs, and all pairs on left and right can be configured as LVDS receive pairs. The PIC logic in the left and right banks also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as XGMII, 7:1 LVDS, along with memory interfaces including DDR3 and LPDDR3.

The ECP5 Automotive registers in PFU and sysI/O can be configured to be SET or RESET. After power up, the device is configured and then enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided PLLs, DLLs, and configuration functions. The ECP5 Automotive architecture provides up to four Delay Locked Loops (DLLs) and up to four Phase Locked Loops (PLLs). The PLL and DLL blocks are located at the corners of each device.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates, and dual-boot support is located at the bottom of each device, to the left of the SERDES blocks. Every device in the ECP5 Automotive family supports a sysCONFIG™ port located in that same corner, powered by V_{CCIO8}, allowing for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The ECP5 Automotive devices use 1.1 V as their core voltage.

2.8. Dynamic Clock Control

The Dynamic Clock Control (DCC), Quadrant Clock enable/disable feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, the clock signal is static and not toggle. All the logic fed by that clock will not toggle, reducing the overall power consumption of the device. The disable function will not create glitch and increase the clock latency to the primary clock network.

This DCC controls the clock sources from the Primary CLOCK MIDMUX before they are fed to the Primary Center MUXs that drive the quadrant clock network. For more information about the DCC, refer to TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide.

2.9. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources. Depending on the operation modes, it switches between two independent input clock sources either with or without any glitches. This is achieved regardless of when the selected signal is toggled. Both input clocks must be running to achieve functioning glitch-less DCS output clock, but it does not require running clocks when being used as non-glitch-less normal clock multiplexer.

There are two DCS blocks per device that are fed to all quadrants. The inputs to the DCS block come from all the output of MIDMUXs and Clock from CIB located at the center of the PLC array core. The output of the DCS is connected to one of the inputs of Primary Clock Center MUX.

Figure 2.7 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide.

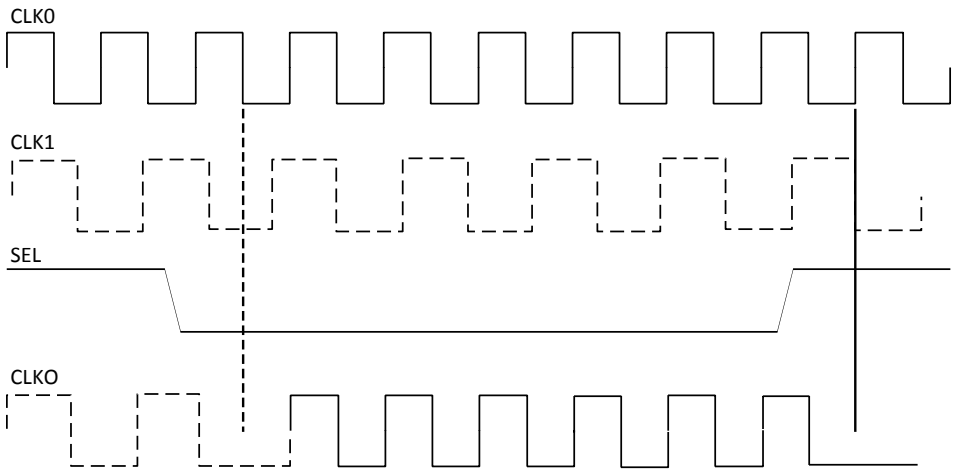


Figure 2.7. DCS Waveforms

2.10. Edge Clock

ECP5 Automotive devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are two ECLK networks per bank IO on the Left and Right sides of the devices.

Each Edge Clock can be sourced from the following:

- Dedicated Clock input pins (PCLK)
- DLLDEL output (Clock delayed by 90°)
- PLL outputs (CLKOP and CLKOS)
- ECLKBRIDGE
- Internal Nodes

2.12. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90-degree phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90-degree shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL and DLLDEL, which takes a clock input, and generates a 90-degree shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90-degree clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

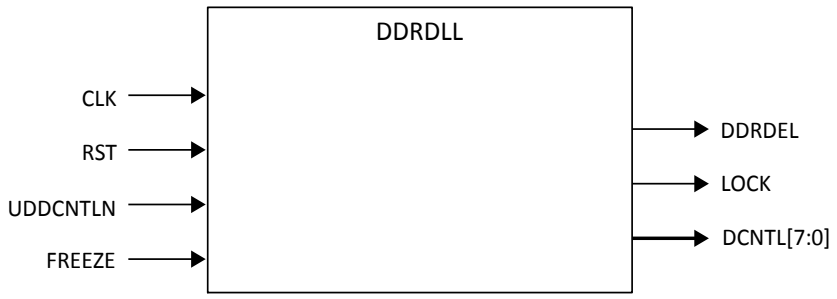


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delayed.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. When UDDCNTLN goes LOW, the delay code out the DDRDLL is updated. Should not be active during a read or a write cycle.
FREEZE	Input	FREEZE goes HIGH and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes LOW, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are identical DDRDLLs, four in each corner in LAE5-45 device and two in upper corners in both LAE5-25 and LAE5-12 devices. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL, DQSBUF, and DLLDEL use the code to delay the signal, to create the phase shifted signal used for either DDR memory, or to create 90-degree shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

The ECP5 Automotive sysDSP block supports the following basic elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2.7 shows the capabilities of each of the ECP5 Automotive slices versus the above functions.

Table 2.7. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1*	1/2	—

***Note**: One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the above four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation”, the following operations are possible:

- In the Add/Sub option, the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

For further information, refer to TN1267, ECP5 and ECP5-5G sysDSP Usage Guide.

2.16. Programmable I/O Cells

The programmable logic associated with an I/O is called a PIO. The individual PIO is connected to their respective sysIO buffers and pads. On the ECP5 Automotive devices, the Programmable I/O cells (PIC) are assembled into groups of four PIO cells that are called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the ECP5 Automotive devices, two adjacent PIOs can be combined to provide a complementary output driver pair. All PIO pairs can implement differential receivers. Half of the PIO pairs on the left and right edges of these devices can be configured as true LVDS transmit pairs.

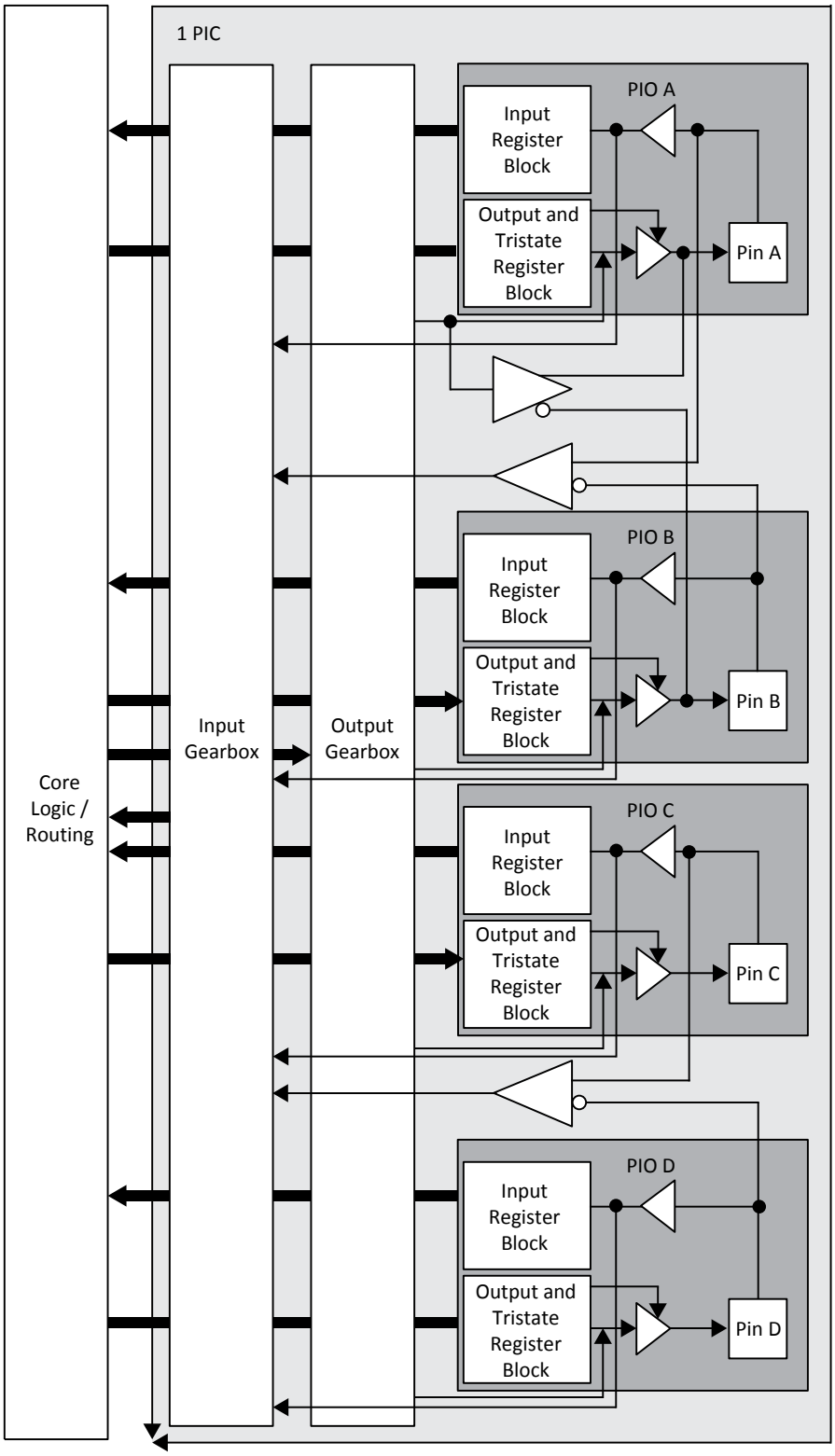


Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Side

2.17. PIO

The PIO contains three blocks: an input register block, an output register block, and a tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

2.17.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The Top side of the device will support IDDRX1 gearing function. For more information on gearing function, refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

Figure 2.17 shows the input register block for the PIOs on the top edge.

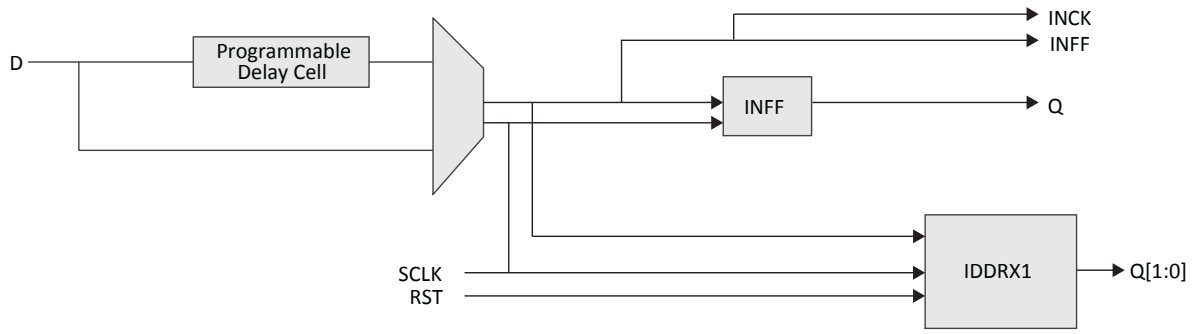
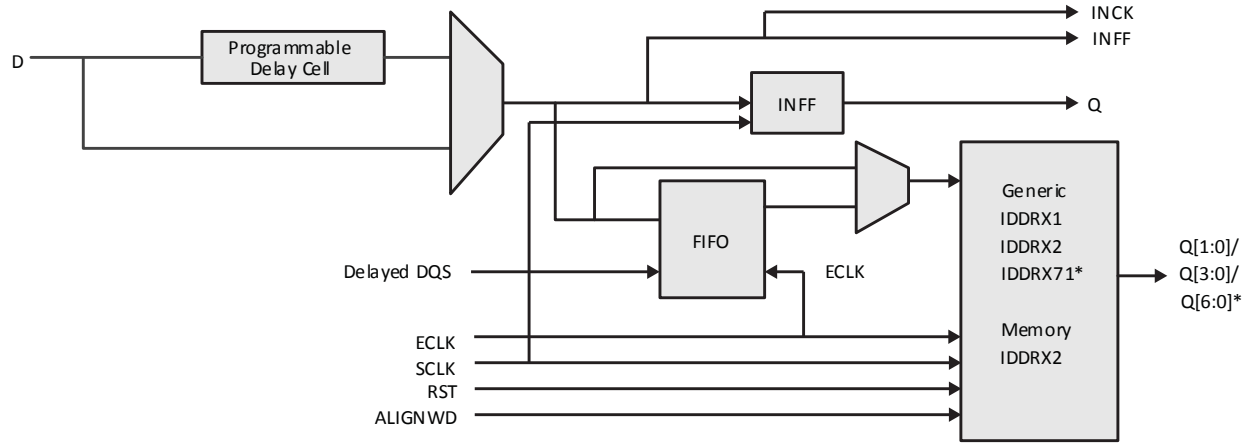


Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



*Note: For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.18. Input Register Block for PIO on Left or Right Side of the Device

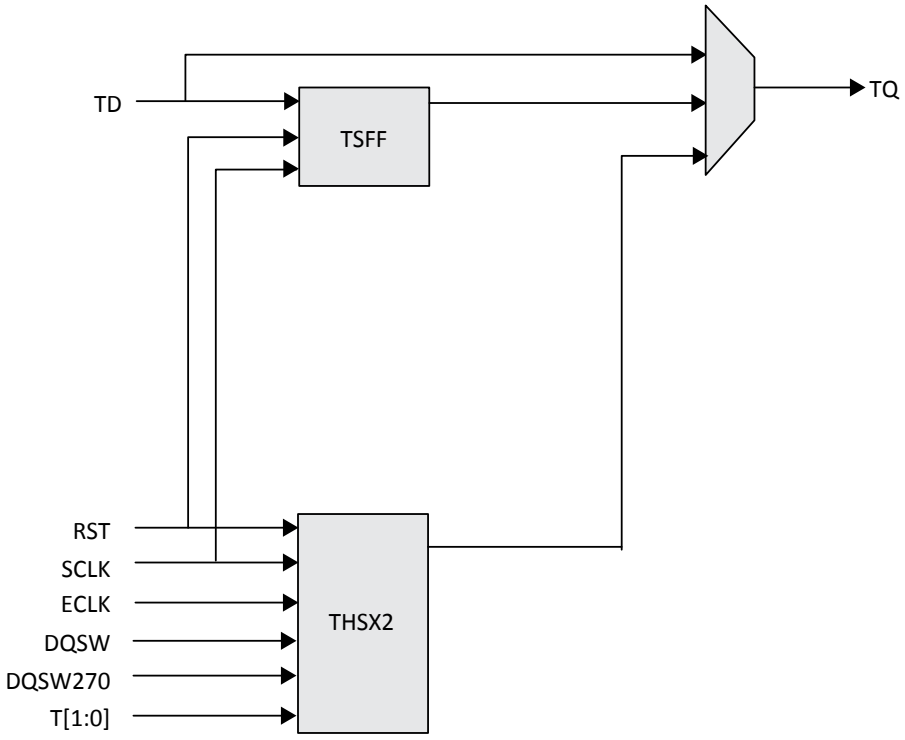


Figure 2.22. Tristate Register Block on Left or Right Side

Table 2.10. Tristate Block Port

Name	Type	Description
TD	Input	Tristate Input to Tristate SDR register
RST	Input	Reset to the Tristate block
TD[1:0]	Input	Tristate input to TSHX2 function
SCLK	Input	Slow Speed system clock
ECLK	Input	High speed edge clock
DQSW	Input	Clock from DQS control block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control block used to generate DDR memory DQ output
TQ	Output	Output of the Tristate block

2.19. DDR Memory Support

2.19.1. DQS Grouping for DDR Memory

Some PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. The support varies by the edge of the device as detailed below.

The left and right sides of the PIC have fully functional elements supporting DDR2, DDR3, LPDDR2 or LPDDR3 memory interfaces. Every 16 PIOs on the left and right sides are grouped into one DQS group, as shown in Figure 2.23. Within each DQS group, there are two pre-placed pins for DQS and DQS# signals. The rest of the pins in the DQS group can be used as DQ signals and DM signal. The number of pins in each DQS group bonded out is package dependent. DQS groups with less than 11 pins bonded out can only be used for LPDDR2/3 Command/ Address busses. For DQS groups with more than 11 pins bonded out, two pre-defined pins can be assigned as "virtual" V_{CCIO} by driving these pins to HIGH. These pins are required to be connected to V_{CCIO} power supply. These connections create "soft" connections to V_{CCIO} through these output pins, and make better connections on VCCIO to help to reduce SSO noise. For details, refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

ECP5 Automotive devices contain two types of sysI/O buffer pairs:

- Top, Bank 0 and Bank 1, and Bottom, Bank 8 and Bank 4, single-ended sysIO Buffer Pairs

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and are configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top or bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for being used as emulated differential signaling.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Semiconductor Diamond tool.
- Left and right banks have 50% differential sysI/O buffer pairs and 100% single-ended outputs.

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers, both ratioed and referenced, and half of the sysI/O buffer pairs, PIOA/B pairs. Also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.20.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5 Automotive devices, see the list of technical documentation in Supplemental Information section on page 96.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.20.3. Supported sysI/O Standards

The ECP5 Automotive sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide.

3.11. SERDES Power Supply Requirements

Over recommended operating conditions.

Table 3.9. ECP5UM

Symbol	Description	Typ	Max	Unit
Standby (Power Down)				
I_{CCA-SB}	V_{CCA}, Power Supply Current per Channel	4	—	mA
$I_{CCHRX-SB}$[1]	V_{CCHRX}, Input Buffer Current per Channel	—	—	mA
$I_{CCHTX-SB}$	V_{CCHTX}, Output Buffer Current per Channel	—	—	mA
Operating (Data Rate = 3.125 Gb/s)				
I_{CCA-OP}	V_{CCA}, Power Supply Current per Channel	43	—	mA
$I_{CCHRX-OP}$[2]	V_{CCHRX}, Input Buffer Current per Channel	0.4	—	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current per Channel	10	—	mA
Operating (Data Rate = 2.5 Gb/s)				
I_{CCA-OP}	V_{CCA}, Power Supply Current per Channel	40	—	mA
$I_{CCHRX-OP}$[2]	V_{CCHRX}, Input Buffer Current per Channel	0.4	—	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current per Channel	10	—	mA
Operating (Data Rate = 1.25 Gb/s)				
I_{CCA-OP}	V_{CCA}, Power Supply Current per Channel	34	—	mA
$I_{CCHRX-OP}$[2]	V_{CCHRX}, Input Buffer Current per Channel	0.4	—	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current per Channel	10	—	mA
Operating (Data Rate = 270 Mb/s)				
I_{CCA-OP}	V_{CCA}, Power Supply Current per Channel	28	—	mA
$I_{CCHRX-OP}$[2]	V_{CCHRX}, Input Buffer Current per Channel	0.4	—	mA
$I_{CCHTX-OP}$	V_{CCHTX}, Output Buffer Current per Channel	8	—	mA

Notes:

1. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
2. Refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.

3.14.8. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 for SLVS-400 standard. This standard evolved from the traditional LVDS standard relies on the advantage of its use of smaller voltage swings and a lower common-mode voltage. The 200 mV, or 400 mV p-p, SLVS swing contributes to a reduction in power.

The ECP5 Automotive devices can receive differential input up to 800 Mb/s with its LVDS input buffer. This LVDS input buffer is used to meet the SLVS input standard specified by the JEDEC standard. The SLVS output parameters are compared to ECP5 Automotive LVDS input parameters, as listed in Table 3.16.

Table 3.16. Input to SLVS

Parameter	ECP5 Automotive LVDS Input	SLVS Output	Unit
Vcm (min)	50	150	mV
Vcm (max)	2350	250	mV
Differential Voltage (min)	100	140	mV
Differential Voltage (max)	—	270	mV

ECP5 Automotive does not support SLVS output. However, SLVS output can be created using ECP5 Automotive LVDS outputs by level shift to meet the low Vcm/Vod levels required by SLVS. Figure 3.5 shows how the LVDS output can be shifted externally to meet SLVS levels.

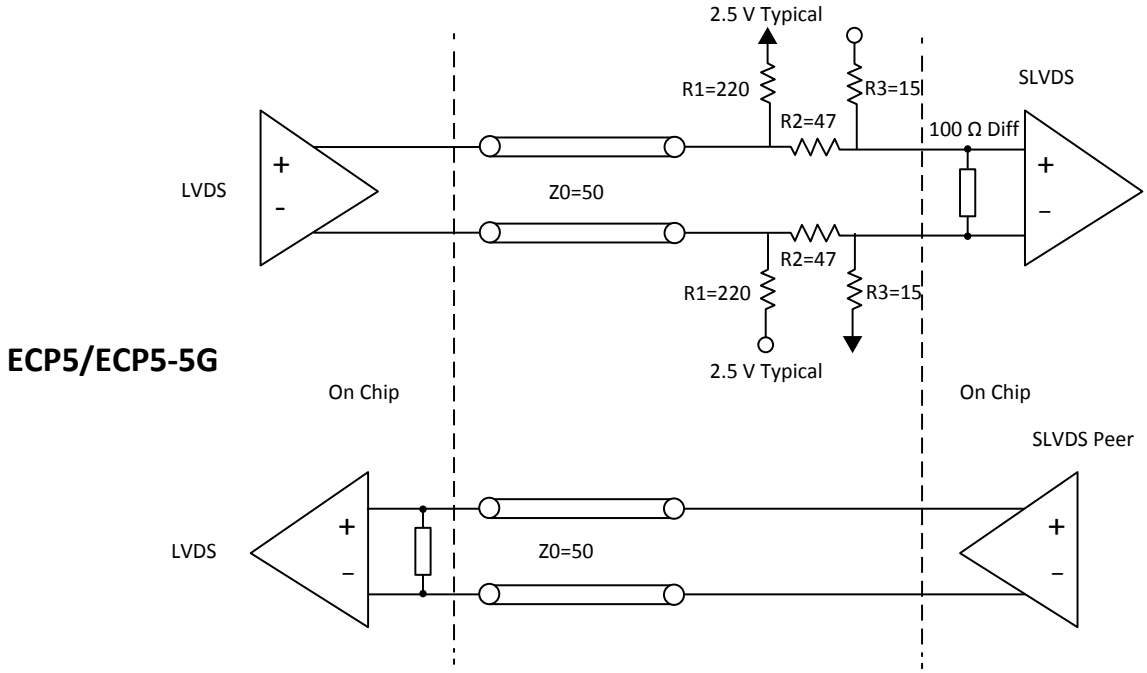


Figure 3.5. SLVS Interface

3.21. SERDES/PCS Block Latency

Table 3.24 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.24. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

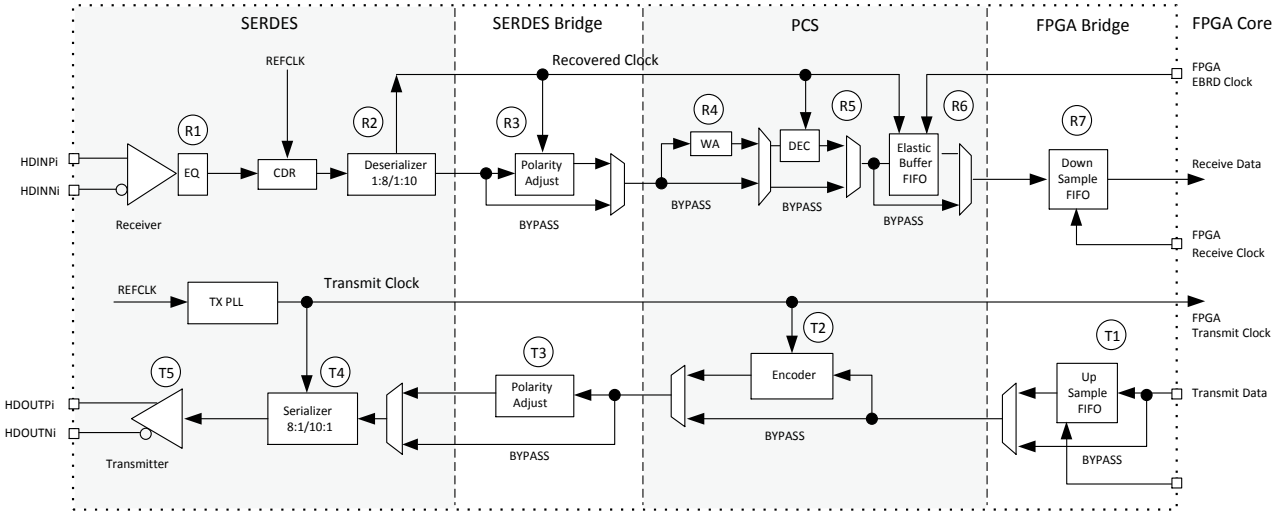
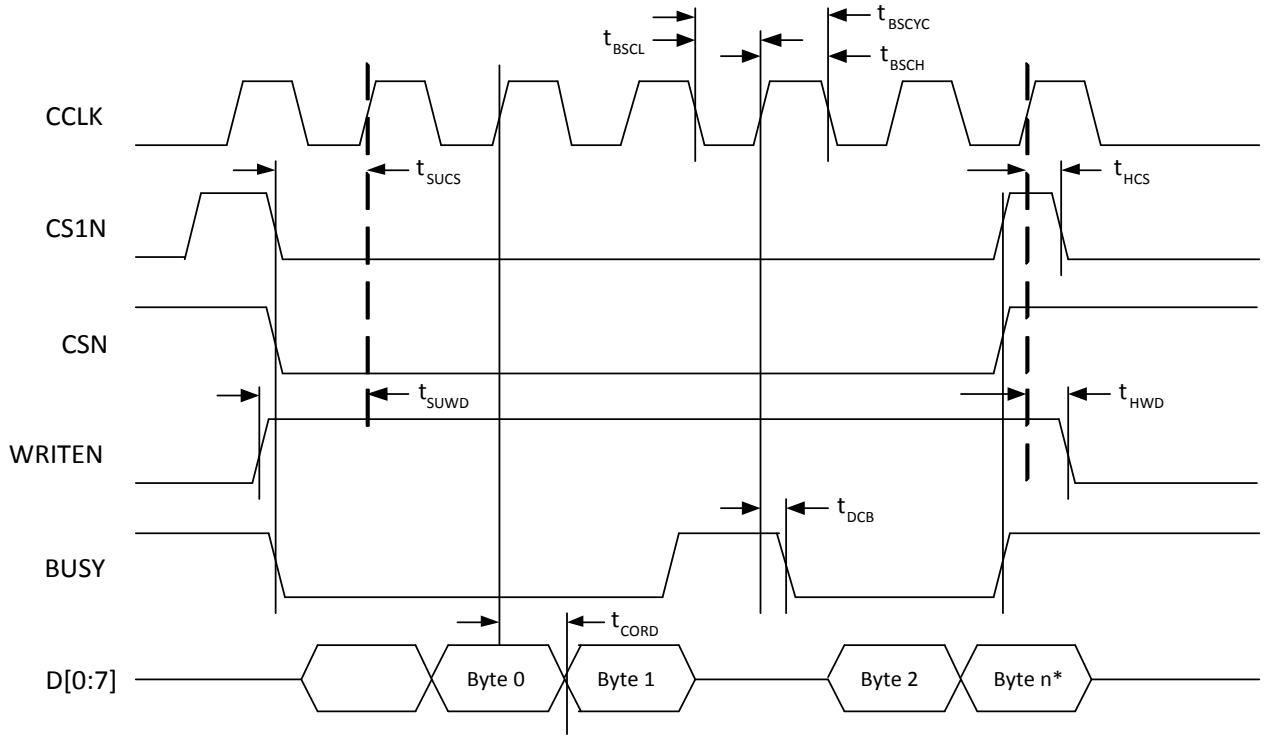


Figure 3.13. Transmitter and Receiver Latency Block Diagram

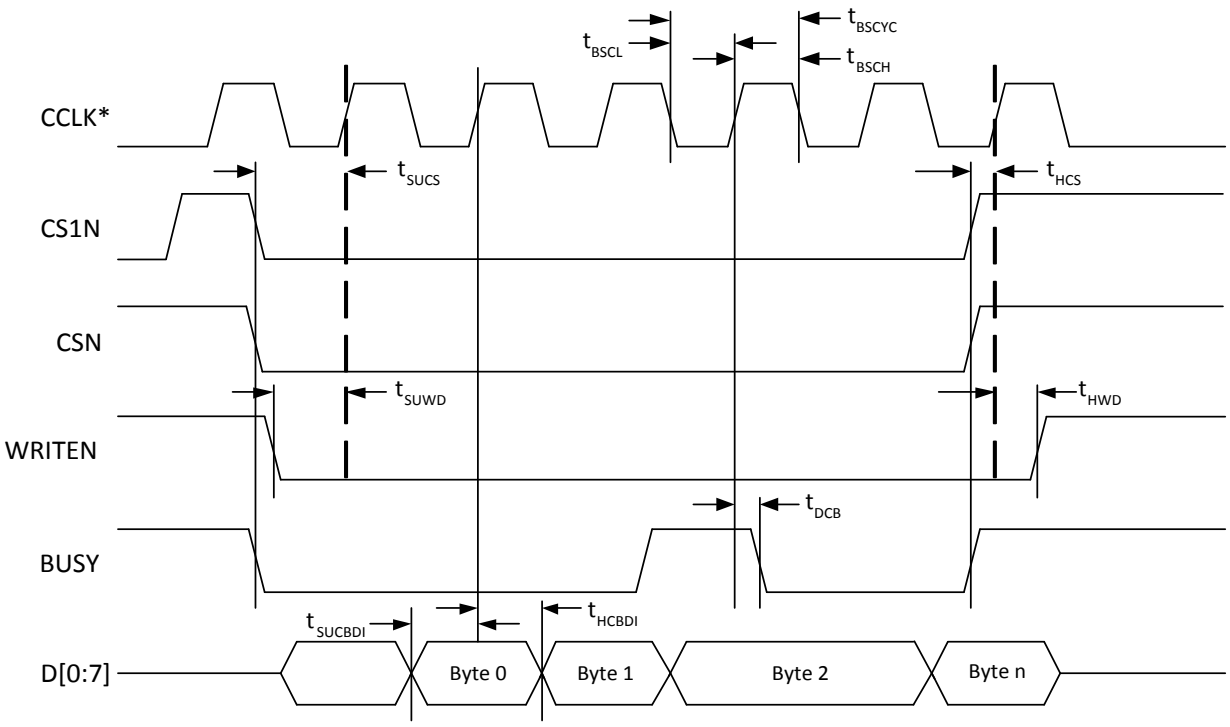
Table 3.39. ECP5 Automotive sysCONFIG Port Timing Specifications *(Continued)*

Symbol	Parameter	Frequency	Min	Max	Unit
Slave Parallel					
t_{HSCDI}	CCLK Hold Time	—	1.5	—	ns
f_{CCLK}	CCLK Input Clock Frequency	—	—	50	MHz
t_{BSCH}	CCLK Input Clock Pulsewidth HIGH	—	6	—	ns
t_{BSCL}	CCLK Input Clock Pulsewidth LOW	—	6	—	ns
t_{CORD}	CCLK to DOUT for Read Data	—	—	12	ns
t_{SUCBDI}	Data Setup Time to CCLK	—	1.5	—	ns
t_{HCBDI}	Data Hold Time to CCLK	—	1.5	—	ns
t_{SUCS}	CSN, CSN1 Setup Time to CCLK	—	2.5	—	ns
t_{HCS}	CSN, CSN1 Hold Time to CCLK	—	1.5	—	ns
t_{SUWD}	WRITEN Setup Time to CCLK	—	45	—	ns
t_{HCWD}	WRITEN Hold Time to CCLK	—	2	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	—	12	ns



*n = last byte of read cycle.

Figure 3.15. sysCONFIG Parallel Port Read Cycle



*In Master Parallel Mode the FPGA provides CCLK (MCLK). In Slave Parallel Mode the external device provides CCLK.

Figure 3.16. sysCONFIG Parallel Port Write Cycle

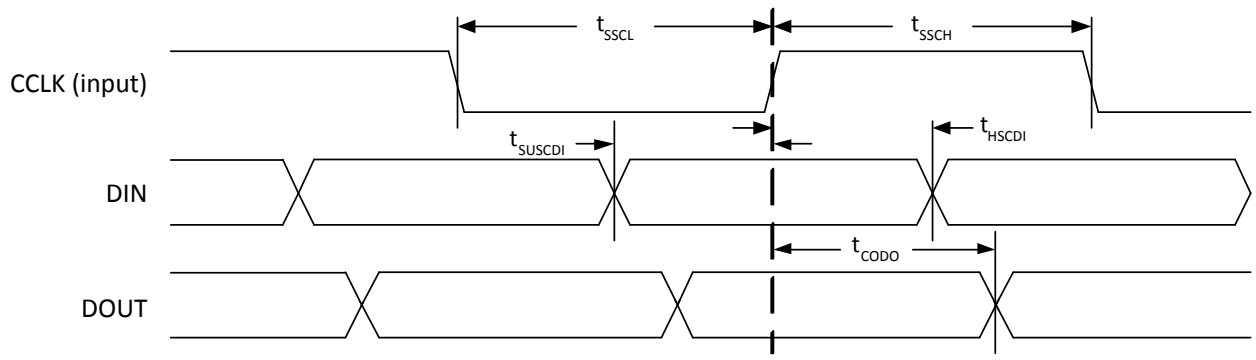


Figure 3.17. sysCONFIG Slave Serial Port Timing

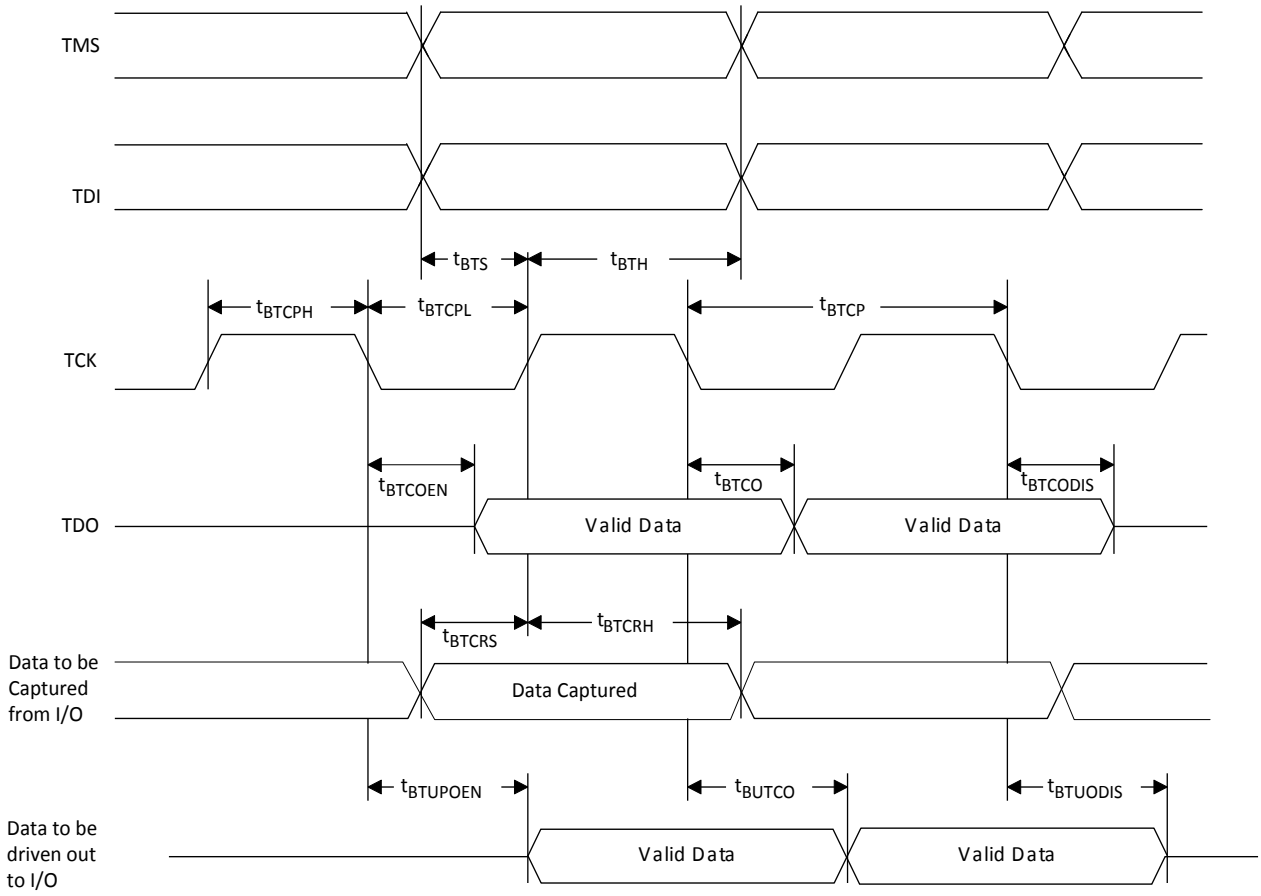
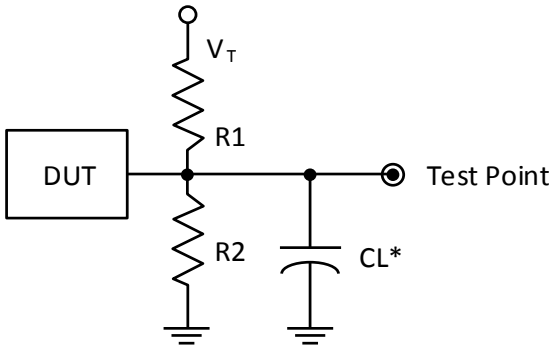


Figure 3.23. JTAG Port Timing Waveforms

3.33. Switching Test Conditions

Figure 3.24 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 3.41.



*Note: CL Includes Test Fixture and Probe Capacitance

Figure 3.24. Output Test Load, LVTTL and LVCMOS Standards

Signal Name	I/O	Description
PLL, DLL and Clock Functions *(Continued)*		
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_ num = ball number associated with DQS[T] pin.
[T/R]]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_ num = ball number associated with DQS[T] pin.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. This is a dedicated input pin.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. Note: once a configuration port is selected, it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.
Configuration Pads (Used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on the rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes – Master SPI or Master Serial. This is a dedicated pin.
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPIm mode data output. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DOUT/CSON	O	Serial data output. Chip select output. SPI/SPIm mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O
D0/MOSI/IO0	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.

Supplemental Information

For Further Information

A variety of technical notes for the ECP5 Automotive family are available.

- TN1184, LatticeECP3, ECP-5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide
- TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide
- TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide
- TN1262, ECP5 and ECP5-5G sysIO Usage Guide
- TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide
- TN1264, ECP5 and ECP5-5G Memory Usage Guide
- TN1265, ECP5 and ECP5-5G High-Speed I/O Interface
- TN1266, Power Consumption and Management for ECP5 and ECP5-5G Devices
- TN1267, ECP5 and ECP5-5G sysDSP Usage Guide

For further information on interface standards, refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL): www.jedec.org
- PCI: www.pcisig.com

Revision History

Date	Version	Section	Change Summary
September 2016	1.0	All	Initial preliminary release.