Lattice Semiconductor Corporation - LAE5UM-25F-7BG381E Datasheet

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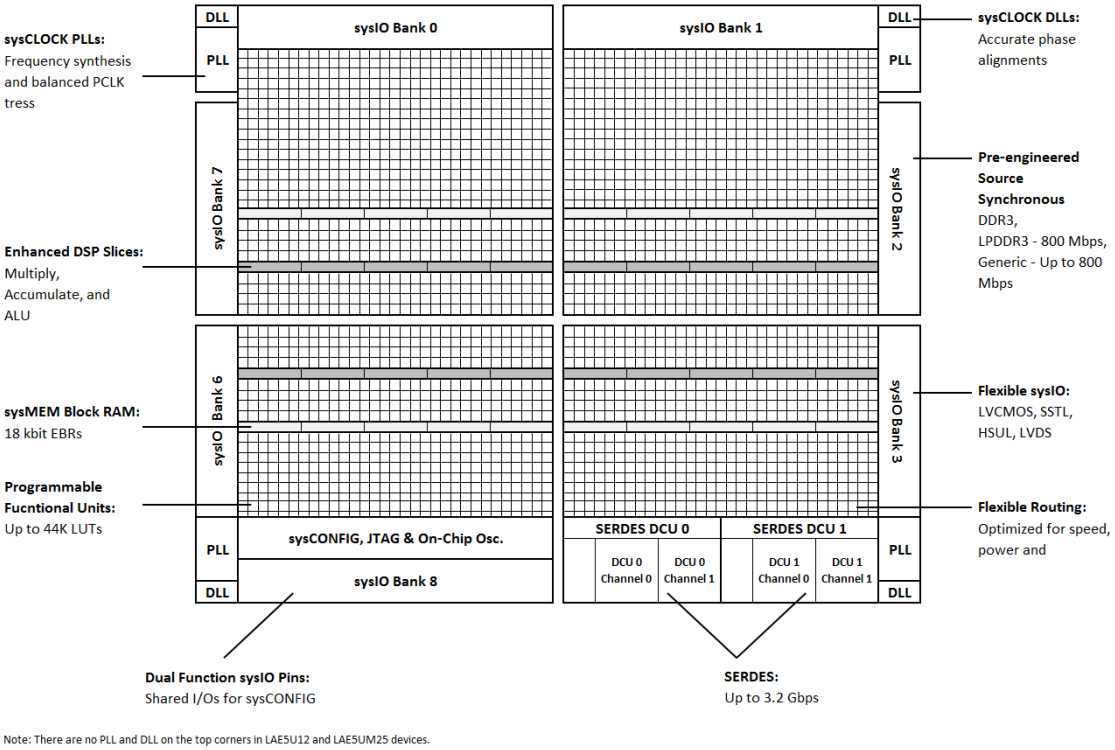
Details	
Product Status	Active
Number of LABs/CLBs	3000
Number of Logic Elements/Cells	24000
Total RAM Bits	1032192
Number of I/O	197
Number of Gates	-
Voltage - Supply	1.04V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae5um-25f-7bg381e

Contents

  - Dedicated DDR2/DDR3 and LPDDR2/LPDDR3 memory support with DQS logic, up to 800 Mb/s data-rate
- Programmable sysI/O™ Buffer Supports Wide Range of Interfaces
  - On-chip termination
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 18/15 I, II
  - HSUL12
  - LVDS, Bus-LVDS, LVPECL, RSDS, MLVDS
  - subLVDS and SLVS, MIPI D-PHY input interfaces
- Flexible Device Configuration
  - Shared bank for configuration I/Os
  - SPI boot flash interface
  - Dual-boot images supported
  - Slave SPI
  - TransFR™ I/O for simple field updates
- Single Event Upset (SEU) Mitigation Support
  - Soft Error Detect – Embedded hard macro
  - Soft Error Correction – Without stopping user operation
  - Soft Error Injection – Emulate SEU event to debug system error handling
- System Level Support
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer
  - On-chip oscillator for initialization and general use
  - 1.1 V core power supply

Table 1.1. ECP5 Automotive Family Selection Guide

Device	LAE5UM-25	LAE5UM-45	LAE5U-12
LUTs (K)	24	44	12
sysMEM Blocks (18 Kb)	56	108	32
Embedded Memory (Kb)	1,008	1944	576
Distributed RAM Bits (Kb)	194	351	97
18 X 18 Multipliers	28	72	28
SERDES (Dual/Channels)	1/2	2/4	0
PLLs/DLLs	2/2	4/4	2/2
Packages and SERDES Channels / I/O Combinations			
381 caBGA (17 x 17 mm^2)	2/197	4/203	0/197



Note: There are no PLL and DLL on the top corners in LAE5U12 and LAE5UM25 devices.

Figure 2.1. Simplified Block Diagram of LAE5UM-45 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5 Automotive device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0 – 3 as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in different modes.

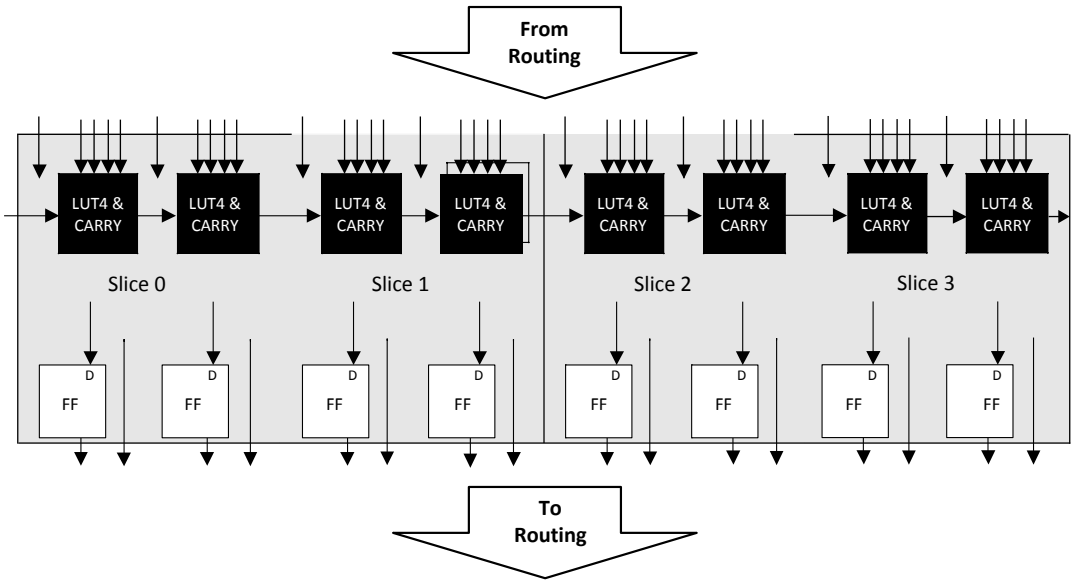
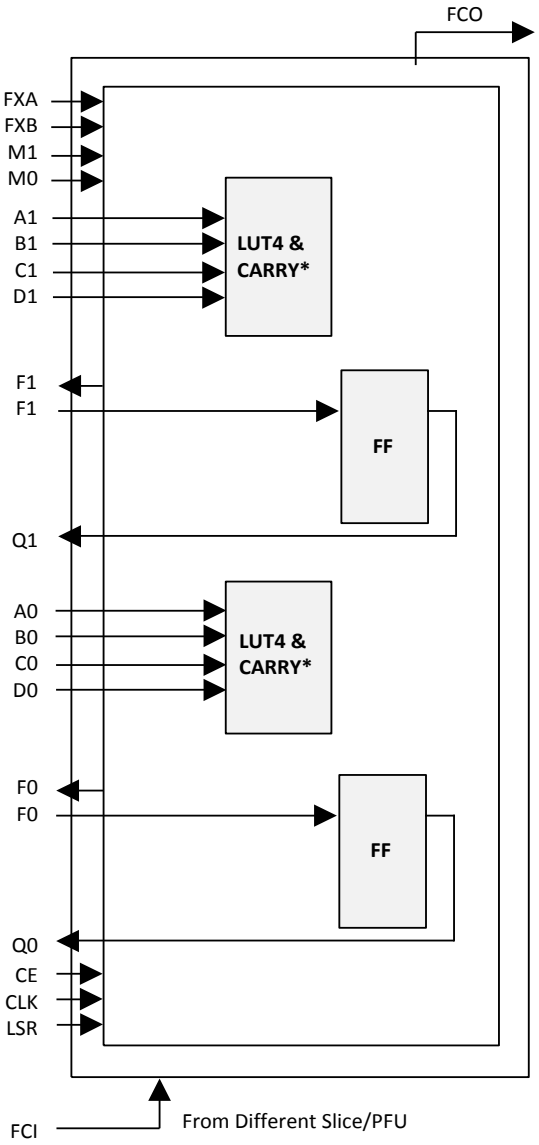


Figure 2.2. PFU Diagram



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.3. Slice Diagram

2.12. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90-degree phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90-degree shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL and DLLDEL, which takes a clock input, and generates a 90-degree shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90-degree clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

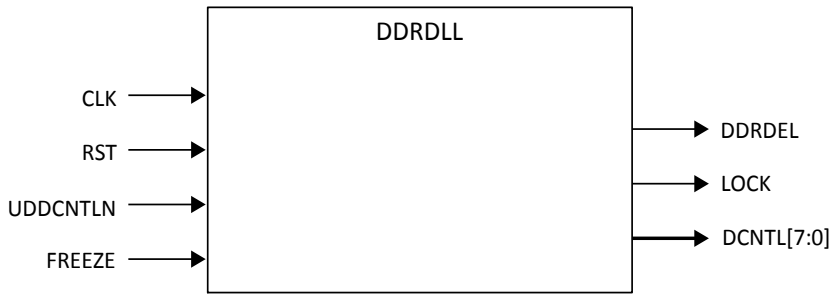


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delayed.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. When UDDCNTLN goes LOW, the delay code out the DDRDLL is updated. Should not be active during a read or a write cycle.
FREEZE	Input	FREEZE goes HIGH and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes LOW, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are identical DDRDLLs, four in each corner in LAE5-45 device and two in upper corners in both LAE5-25 and LAE5-12 devices. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL, DQSBUF, and DLLDEL use the code to delay the signal, to create the phase shifted signal used for either DDR memory, or to create 90-degree shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

2.13.6. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.12.

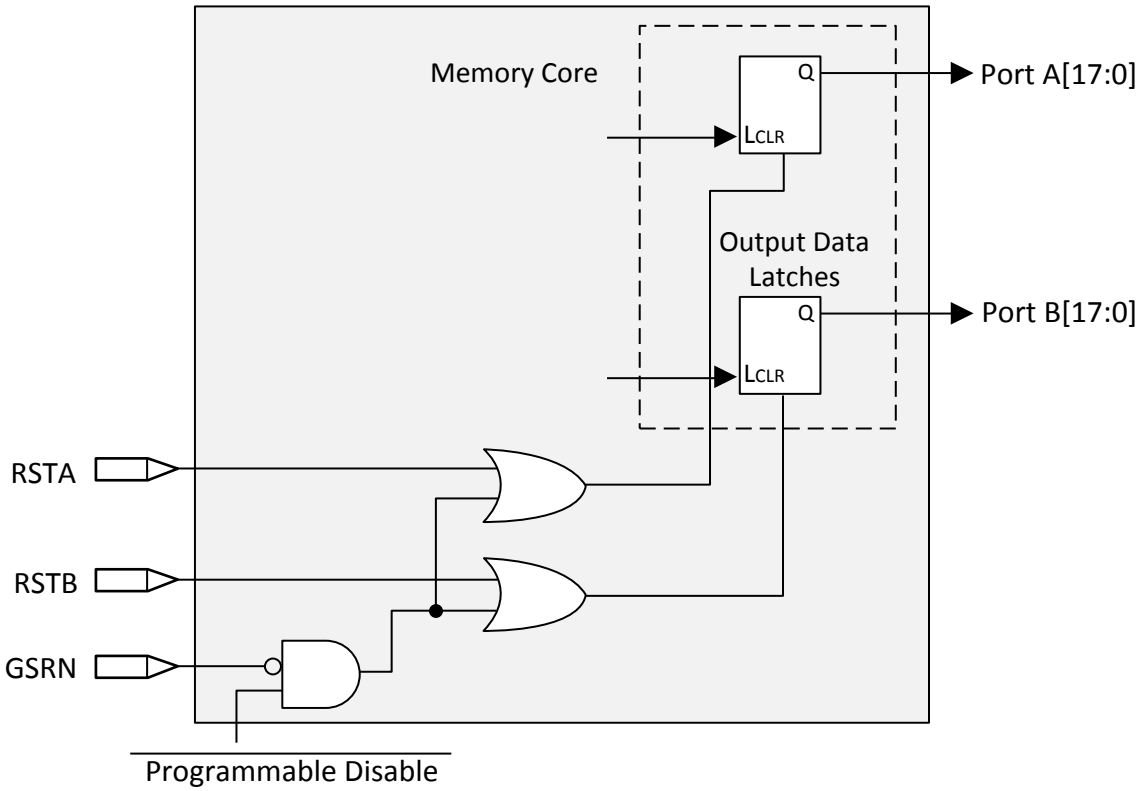


Figure 2.12. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section on page 96.

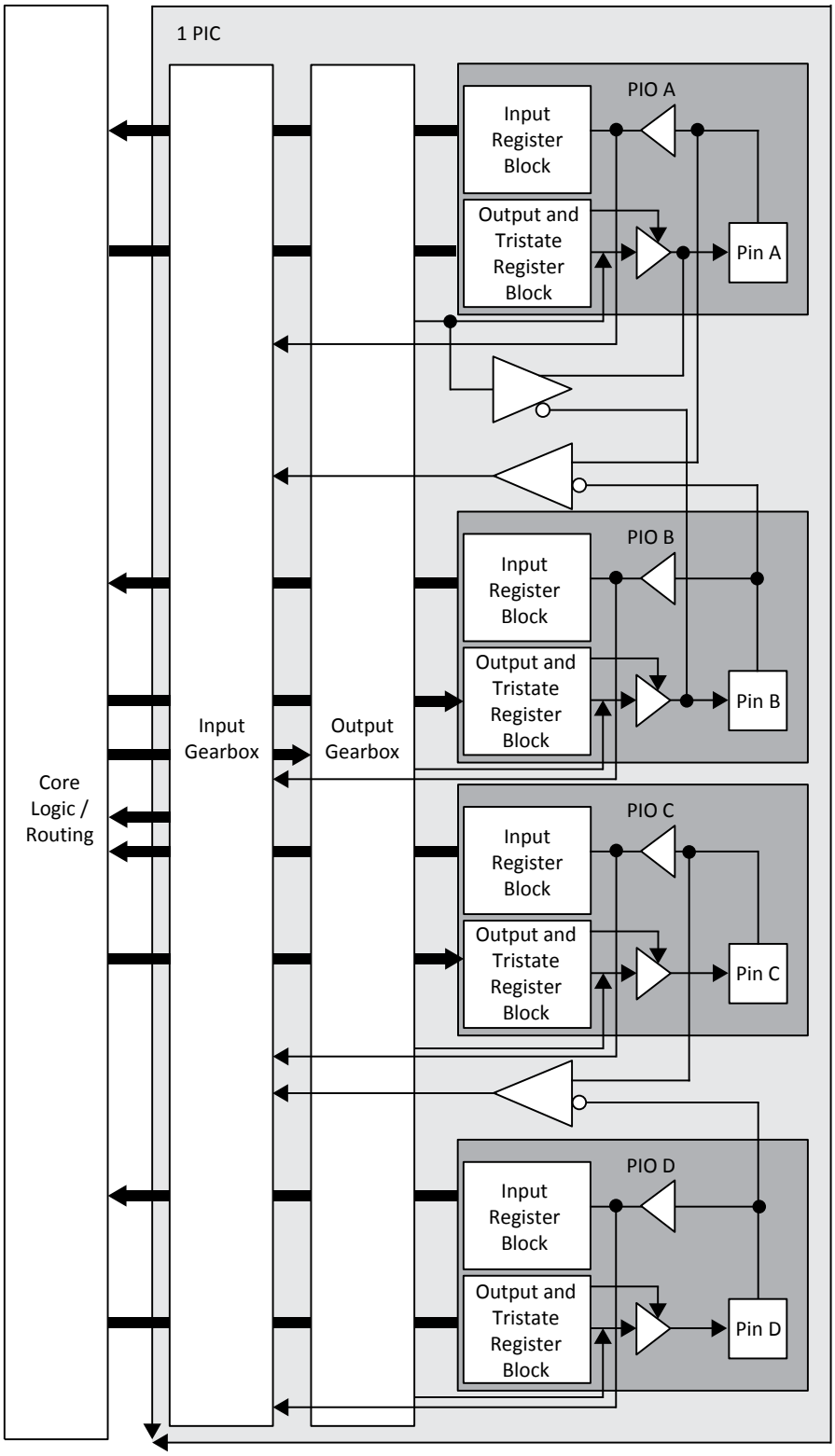


Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Side

2.20. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVDS, HSUL, BLVDS, SSTL Class I and II, LVCMOS, LVTTL, LVPECL, and MIPI.

2.20.1. sysI/O Buffer Banks

ECP5 Automotive devices have seven sysI/O buffer banks, two banks per side at Top, Left and Right, plus one at the bottom left side. The bottom left side bank, Bank 8, is a shared I/O bank. The I/Os in that bank contains both dedicated and shared I/O for sysConfig function. When a shared pin is not used for configuration, it is available as a user I/O.

In ECP5 Automotive devices, the Left and Right sides are tailored to support high performance interfaces, such as DDR2, DDR3, LPDDR2, LPDDR3 and other high speed source synchronous standards. The banks on the Left and Right sides of the devices feature LVDS input and output buffers, data-width gearing, and DQSBUF block to support DDR2/3 and LPDDR2/3 interfaces. The I/Os on the top and bottom banks do not have LVDS input and output buffer, and gearing logic, but can use LVCMOS to emulate most of differential output signaling.

Each sysIO bank has its own I/O supply voltage V_{CCIO}. In addition, the banks on the Left or Right side of the device, have voltage reference input, V_{REF1} per bank, which allow it to be completely independent of each other. This voltage reference input is a shared I/O pin. The V_{REF} voltage is used to set the threshold for the referenced input buffers, such as SSTL. Figure 2.25 shows the seven banks and their associated supplies.

In ECP5 Automotive devices, single-ended output buffers and ratioed input buffers, LVTTL, and LVCMOS, are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25, and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

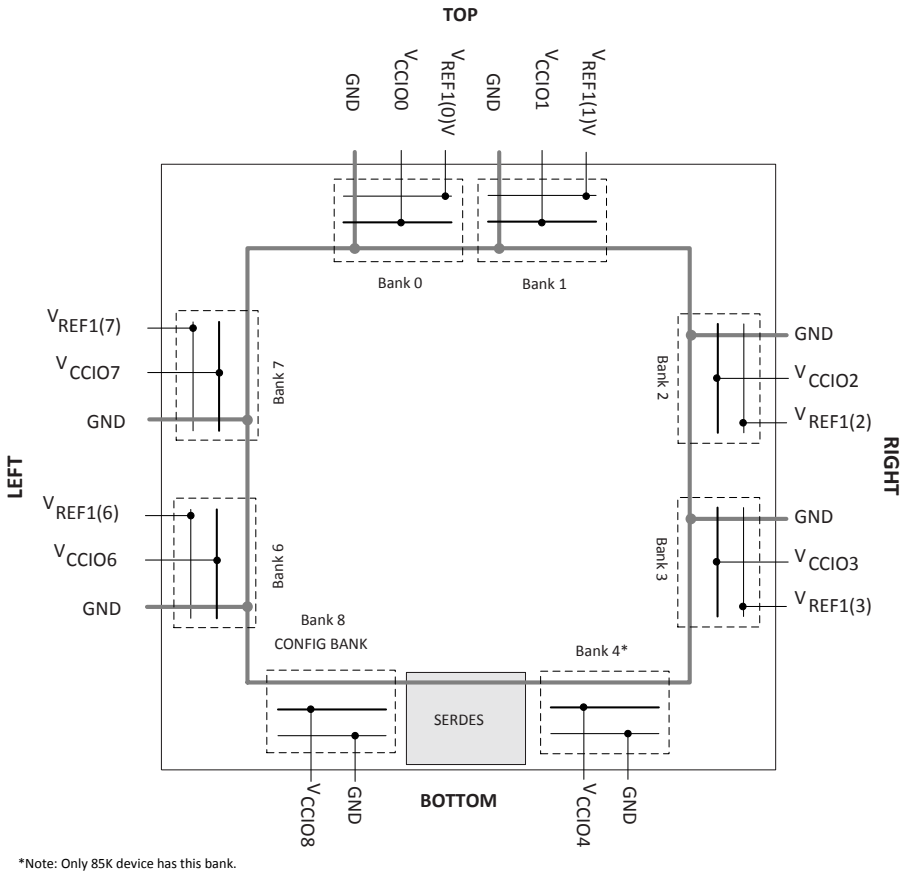


Figure 2.25. ECP5 Automotive Device Family Banks

Table 2.13. LAE5UM SERDES Standard Support

Standard	Data Rate (Mb/s)	Number of General/Link Width	Encoding Style
PCI Express 1.1 and 2.0	2500	x1, x2, x4	8b10b
Gigabit Ethernet	1250	x1	8b10b
SGMII	1250	x1	8b10b
XAUI	3125	x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4	614.4 1228.8 2457.6 3072.0	x1	8b10b
SD-SDI (259M, 344M)*	270	x1	NRZI/Scrambled
HD-SDI (292M)	1483.5 1485	x1	NRZI/Scrambled
3G-SDI (424M)	2967 2970	x1	NRZI/Scrambled
JESD204A/B	3125	x1	8b/10b

***Note**:
For slower rates, the SERDES are bypassed and CML signals are directly connected to the FPGA routing.

Table 2.14. Available SERDES Duals per LAE5UM Device

Package	LAE5UM -25	LAE5UM -45
381 caBGA	1	2

2.21.1. SERDES Block

A SERDES receiver channel may receive serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR), and de-serialize the data stream before passing the 8b/10b data to the PCS logic. The SERDES transmitter channel may receive the parallel 8b/10b data, serialize the data, and transmit the serial bit stream through the differential drivers. Figure 2.28 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply V_{CCA}. The output and input buffers of each channel have their own independent power supplies, V_{CCHTX} and V_{CCHRX}.

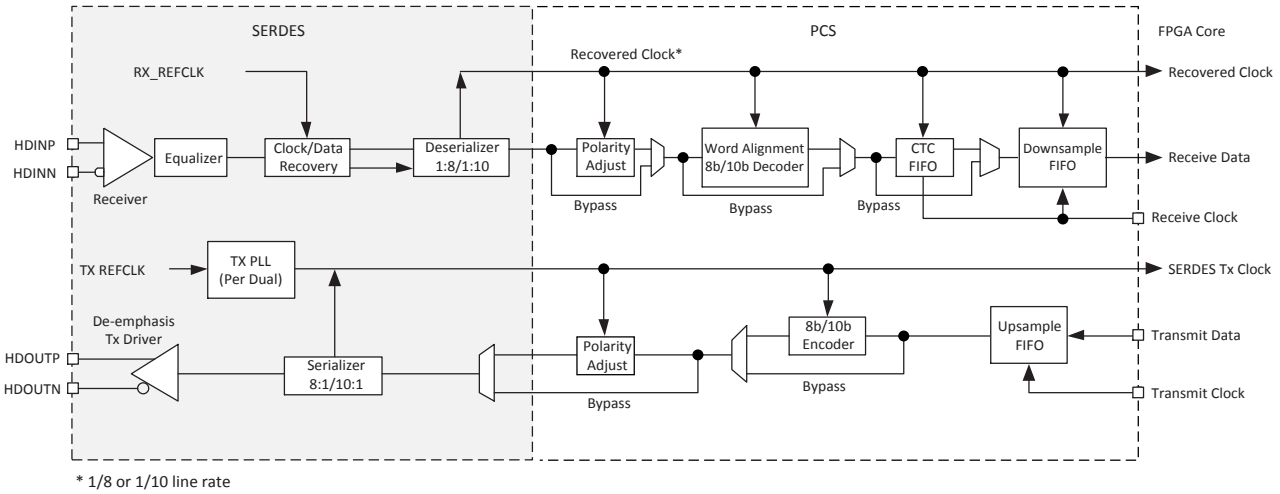


Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

2.21.2. PCS

As shown in Figure 2.28, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes 8b/10b, provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8b/10b data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8b/10b interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

Some of the enhancements in LAE5UM SERDES/PCS include:

- Higher clock/channel granularity: Dual channel architecture provides more clock resource per channel.
- Enhanced TX de-emphasis: Programmable pre- and post-cursors improves TX output signaling.
- Bit-slip function in PCS: Improves logic needed to perform Word Alignment function.

Refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide for more information.

2.21.3. SERDES Client Interface Bus

The SERDES Client Interface (SCI) is an IP interface that allows the user to change the configuration through this interface. This is useful when the user needs to fine-tune some settings, such as input and output buffer that need to be optimized based on the channel characteristics. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

The Diamond design tools support all modes of the PCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow users to define their own operation. With these tools, the user can define the mode for each dual in a design.

Popular standards such as 10 Gb Ethernet, x4 PCI Express, and 4x Serial RapidIO can be implemented using IP that is available through Lattice Semiconductor), with two duals which is four SERDES channels with PCS and some additional logic from the core.

The LAE5UM devices support a wide range of protocols. Within the same dual, the LAE5UM devices support mixed protocols with semi-independent clocking as long as the required clock frequencies are integer x1, x2, or x11 multiples of each other. Table 2.15 lists the allowable combination of primary and secondary protocol combinations.

2.22. Flexible Dual SERDES Architecture

The LAE5UM SERDES architecture is a dual channel-based architecture. For most SERDES settings and standards, the whole dual, consisting of two SERDES channels, is treated as a unit. This helps in silicon area savings, better utilization, higher granularity on clock/SERDES channel and overall lower cost.

However, for some specific standards, the LAE5UM dual-channel architecture provides flexibility. More than one standard can be supported within the same dual.

Table 2.15 lists the standards that can be mixed and matched within the same dual. In general, the SERDES standards whose nominal data rates are either the same or a defined subset of each other, can be supported within the same dual. The two Protocol columns of the table define the different combinations of protocols that can be implemented together within a Dual.

Table 2.15. LAE5UM Mixed Protocol Support

Protocol		Protocol
PCI Express 1.1	with	SGMII
PCI Express 1.1	with	Gigabit Ethernet
CPRI-3	with	CPRI-2 and CPRI-1
3G-SDI	with	HD-SDI and SD-SDI

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	1.21	V
V_{CCA}	Supply Voltage	–0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	2.75	V
V_{CCIO}	Supply Voltage	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	–0.5	1.32	V
—	Voltage Applied on SERDES Pins	–0.5	1.80	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Semiconductor Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter	Device	Min	Max	Unit
V_{CC}[2]	Core Supply Voltage	All	1.045	1.155	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage	All	2.375	2.625	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	All	1.14	3.465	V
V_{REF}[1]	Input Reference Voltage	All	0.5	1.0	V
t_{JAUTO}	Junction Temperature, Industrial Operation	All	–40	125	°C
SERDES External Power Supply[5]					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	All	2.374	2.625	V
V_{CCHRX}[6]	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 .
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the SERDES Power Supply Requirements section of this Data Sheet.

3.12. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min	Typ	Max	Min	Typ	Max
LVCMOS33[1]	3.135	3.3	3.465	—	—	—
LVCMOS33D[3] Output	3.135	3.3	3.465	—	—	—
LVCMOS25[1]	2.375	2.5	2.625	—	—	—
LVCMOS18	1.71	1.8	1.89	—	—	—
LVCMOS15	1.425	1.5	1.575	—	—	—
LVCMOS12[1]	1.14	1.2	1.26	—	—	—
LVTTL33[1]	3.135	3.3	3.465	—	—	—
SSTL15_I, _II[2]	1.43	1.5	1.57	0.68	0.75	0.9
SSTL18_I, _II[2]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL135_I, _II[2]	1.28	1.35	1.42	0.6	0.675	0.75
HSUL12[2]	1.14	1.2	1.26	0.588	0.6	0.612
MIPI D-PHY LP Input[3]	1.425	1.5	1.575	—	—	—
LVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
subLVS[3] (Input only)	—	—	—	—	—	—
SLVS[3] (Input only)	—	—	—	—	—	—
LVDS25E[3] Output	2.375	2.5	2.625	—	—	—
MLVDS[3] Output	2.375	2.5	2.625	—	—	—
LVPECL33[1, 3] Output	3.135	3.3	3.465	—	—	—
BLVDS25[1, 3] Output	2.375	2.5	2.625	—	—	—
HSULD12D[2, 3]	1.14	1.2	1.26	—	—	—
SSTL135D_I, II[2, 3]	1.28	1.35	1.42	—	—	—
SSTL15D_I, II[2, 3]	1.43	1.5	1.57	—	—	—
SSTL18D_I[1, 2, 3], II[1, 2, 3]	1.71	1.8	1.89	—	—	—

Notes:

1. For input voltage compatibility, refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide.
2. V_{REF} is required when using Differential SSTL and HSUL to interface to DDR/LPDDR memories.
3. These differential inputs use LVDS input comparator, which uses V_{CCAUX} power.
4. All differential inputs and LVDS25 output are supported in the Left and Right banks only. Refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide for details.

3.14. sysI/O Differential Electrical Characteristics

3.14.1. LVDS

Over recommended operating conditions.

Table 3.11. LVDS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two	±100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	±10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9 V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA

Note: On the left and right sides of the device, this specification is valid only for V_{CCIO} = 2.5 V or 3.3 V.

3.14.2. SSTLD

All differential SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes, class I and class II, are supported in this mode.

3.14.3. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO}. The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 12 mA or 16 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

Table 3.18. Register-to-Register Performance

Function	–6 Timing	Unit
Basic Functions		
16-Bit Decoder	—	MHz
32-Bit Decoder	—	MHz
64-Bit Decoder	—	MHz
4:1 Mux	—	MHz
8:1 Mux	—	MHz
16:1 Mux	—	MHz
32:1 Mux	—	MHz
8-Bit Adder	—	MHz
16-Bit Adder	—	MHz
64-Bit Adder	—	MHz
16-Bit Counter	—	MHz
32-Bit Counter	—	MHz
64-Bit Counter	—	MHz
64-Bit Accumulator	—	MHz
Embedded Memory Functions		
1024x18 True-Dual Port RAM (Write Through or Normal), with EBR Output Registers	—	MHz
1024x18 True-Dual Port RAM (Read-Before-Write), with EBR Output Registers	—	MHz
Distributed Memory Functions		
16 x 2 Pseudo-Dual Port or 16 x 4 Single Port RAM (One PFU)	—	MHz
16 x 4 Pseudo-Dual Port (Two PFUs)	—	MHz
DSP Functions (DDR/SDR)		
9 x 9 Multiplier (All Registers)	—	MHz
18 x 18 Multiplier (All Registers)	—	MHz
36 x 36 Multiplier (All Registers)	—	MHz
18 x 18 Multiply-Add/Sub (All Registers)	—	MHz
18 x 18 Multiply/Accumulate (Input and Output Registers)	—	MHz

Notes:

1. These functions were generated using Lattice Semiconductor Diamond design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.
2. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from Lattice Semiconductor Diamond design software tool.

3.16. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

Table 3.20. ECP5 Automotive External Switching Characteristics *(Continued)*

Parameter	Description	Device	–6		Unit
			Min	Max	
Generic DDR Output					
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.8					
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9					
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8					
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9					
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12					
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.2	—	ns + (i) UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.2	ns + (i) UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	262.5	MHz
Memory Interface					
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)					
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.374	—	ns + 1/2 UI

Table 3.33. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential Return Loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common Mode Return Loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential Termination Resistance	—	80	100	120	Ω
J_{RX_DJ}[2, 3, 4]	Deterministic Jitter Tolerance Peak-to-peak	—	—	—	0.37	UI
J_{RX_RJ}[2, 3, 4]	Random Jitter Tolerance Peak-to-peak	—	—	—	0.18	UI
J_{RX_SJ}[2, 3, 4]	Sinusoidal Jitter Tolerance Peak-to-peak	—	—	—	0.10	UI
J_{RX_TJ}[1, 2, 3, 4]	Total Jitter Tolerance Peak-to-peak	—	—	—	0.65	UI
T_{RX_EYE}	Receiver Eye Opening	—	0.35	—	—	UI

Notes:
1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity, and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.29. Gigabit Ethernet/SGMII/CPRI LV E.12 Electrical and Timing Characteristics

3.29.1. AC and DC Characteristics

Table 3.34. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
T_{RF}	Differential Rise/Fall Time	20% to 80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential Impedance	—	80	100	120	Ω
J_{TX_DDJ}[2, 3]	Output Data Deterministic Jitter	—	—	—	0.10	UI
J_{TX_TJ}[1, 2, 3]	Total Output Data Jitter	—	—	—	0.24	UI

Notes:
1. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
2. Jitter values are measured with each CML output AC coupled into a 50 Ω impedance (100 Ω differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.

Table 3.35. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX_DIFF}	Differential Return Loss	From 100 MHz to 1.25 GHz	10	—	—	dB
RL_{RX_CM}	Common Mode Return Loss	From 100 MHz to 1.25 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential Termination Resistance	—	80	100	120	Ω
J_{RX_DJ}[1, 2, 3, 4]	Deterministic Jitter Tolerance Peak-to-peak	—	—	—	0.34	UI
J_{RX_RJ}[1, 2, 3, 4]	Random Jitter Tolerance Peak-to-peak	—	—	—	0.26	UI
J_{RX_SJ}[1, 2, 3, 4]	Sinusoidal Jitter Tolerance Peak-to-peak	—	—	—	0.11	UI
J_{RX_TJ}[1, 2, 3, 4]	Total Jitter Tolerance Peak-to-peak	—	—	—	0.71	UI
T_{RX_EYE}	Receiver Eye Opening	—	0.29	—	—	UI

Notes:
1. Total jitter includes deterministic jitter, random jitter, and sinusoidal jitter.
2. Jitter values are measured with each high-speed input AC coupled into a 50 Ω impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.

3.30. SMPTE SD/HD-SDI/3G-SDI (Serial Digital Interface) Electrical and Timing Characteristics

3.30.1. AC and DC Characteristics

Table 3.36. Transmit

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDO}	Serial Data Date	—	270	—	2975	Mb/s
$T_{JALIGNMENT}$[2]	Serial Output Jitter, Alignment	270 Mb/s[3]	—	—	0.2	UI
$T_{JALIGNMENT}$[2]	Serial Output Jitter, Alignment	1485 Mb/s	—	—	0.2	UI
$T_{JALIGNMENT}$[1, 2]	Serial Output Jitter, Alignment	2970 Mb/s	—	—	0.3	UI
$T_{JTIMING}$	Serial Output Jitter, Timing	270 Mb/s[3]	—	—	0.2	UI
$T_{JTIMING}$	Serial Output Jitter, Timing	1485 Mb/s	—	—	1	UI
$T_{JTIMING}$	Serial Output Jitter, Timing	2970 Mb/s	—	—	2	UI

Notes:

1. Timing jitter is measured in accordance with SMPTE serial data transmission standards.
2. Jitter is defined in accordance with SMPTE RP1 184-1996 as: jitter at an equipment output in the absence of input jitter.
3. 270 Mb/s is supported with Rate Divider only.
4. All Tx jitter are measured at the output of an industry standard cable driver, with the Lattice Semiconductor SERDES device configured to 50 Ω output impedance connecting to the external cable driver with differential signaling.
5. The cable driver drives: RL=75 Ω, AC-coupled at 270, 1485, or 2970 Mb/s.
6. All LAE5UM devices are compliant with all SMPTE compliance tests, except 3G-SDI Level-A pathological compliance pattern test.

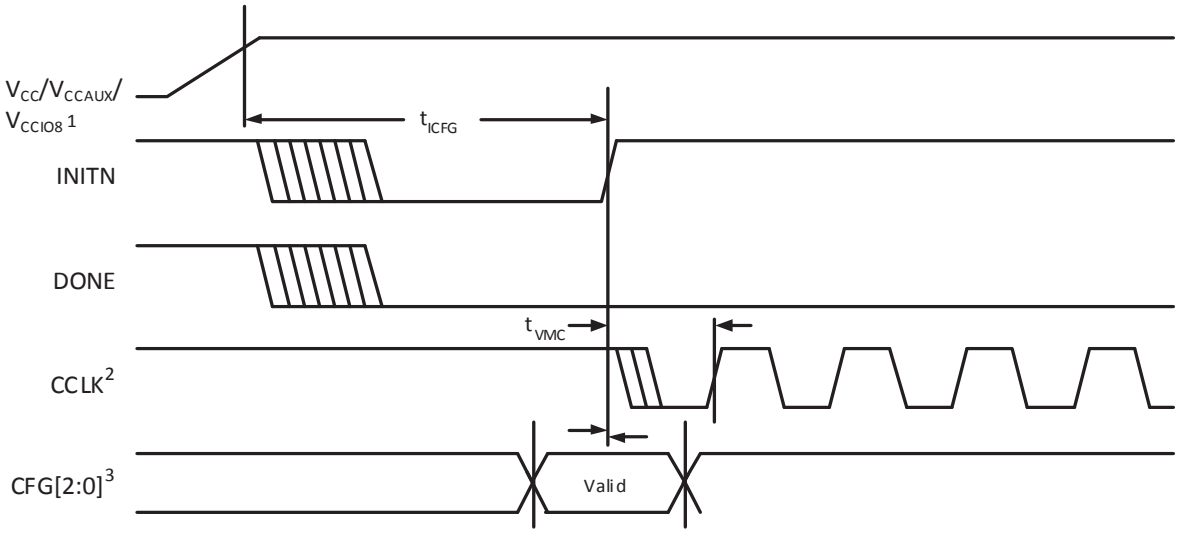
Table 3.37. Receive

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
BR_{SDI}	Serial Input Data Rate	—	270	—	2970	Mb/s

Table 3.38. Reference Clock

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
F_{VCLK}	Video Output Clock Frequency	—	54	—	148.5	MHz
DC_V	Duty Cycle, Video Clock	—	45	50	55	%

Note: 270 Mb/s SD-SDI (is supported with Rate Divider only. For Single Rate: Reference Clock = 54 MHz and Rate Divider = /2. For Tri-Rate: Reference Clock = 148.5 MHz and Rate Divider = /11.



Notes:
1. Time taken from V_{CC}, V_{CCAUX} or V_{CCIO8}, whichever is the last to cross the POR trip point.
2. Device is in a Master Mode (SPI, SPIm).
3. The CFG pins are normally static (hardwired).

Figure 3.18. Power-On-Reset (POR) Timing

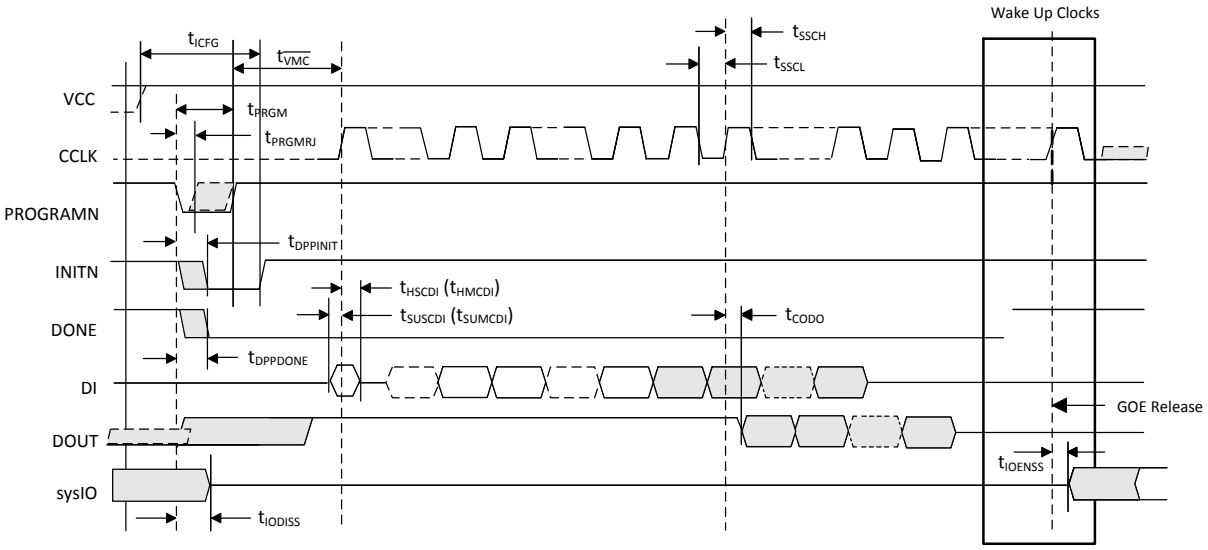


Figure 3.19. sysCONFIG Port Timing

Signal Name	I/O	Description
PLL, DLL and Clock Functions *(Continued)*		
[L/R]DQS[group_num]	I/O	DQS input/output pads: T (top), R (right), group_ num = ball number associated with DQS[T] pin.
[T/R]]DQ[group_num]	I/O	DQ input/output pads: T (top), R (right), group_ num = ball number associated with DQS[T] pin.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. This is a dedicated input pin.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. This is a dedicated input pin.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. Note: once a configuration port is selected, it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. This is a dedicated input pin.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1. This is a dedicated output pin.
Configuration Pads (Used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on the rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI, Serial, and CPU modes. Output Configuration Clock for configuring an FPGA in Master configuration modes – Master SPI or Master Serial. This is a dedicated pin.
HOLDN/DI/BUSY/CSSPIN/CEN	I/O	Parallel configuration mode busy indicator. SPI/SPIm mode data output. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CSN/SN	I/O	Parallel configuration mode active-low chip select. Slave SPI chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
CS1N	I	Parallel configuration mode active-low chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
WRITEN	I	Write enable for parallel configuration modes. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
DOUT/CSON	O	Serial data output. Chip select output. SPI/SPIm mode chip select. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O
D0/MOSI/IO0	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.

4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device Only		
P[L/R] [n−6]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n−3]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n]	A	DQS (P)
	B	DQS (N)
	C	DQ
	D	DQ
P[L/R] [n+3]	A	DQ
	B	DQ
	C	DQ
	D	DQ

Note: “n” is a row PIC number.