Lattice Semiconductor Corporation - LAE5UM-45F-6BG381E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5500
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.04V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae5um-45f-6bg381e

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PIO	Programmable I/O
PLL	Phase Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SCM	Serial Configuration Mode
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPCM	Slave Parallel Configuration Mode
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

1. General Description

The ECP5 Automotive family of FPGA devices is optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. This combination is achieved through advances in device architecture and the use of 40 nm technology making the devices suitable for high-volume, high-speed, and low-cost applications.

The ECP5 Automotive device family covers look-up-table (LUT) capacity to 44K logic elements and supports up to 203 user I/Os. The ECP5 Automotive device family also offers up to 72 18 x 18 multipliers and a wide range of parallel I/O standards.

The ECP5 Automotive FPGA fabric is optimized to reach high performance with low power and low cost in mind. The ECP5 Automotive devices utilize reconfigurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and dual-boot capabilities.

The pre-engineered source synchronous logic implemented in the ECP5 Automotive device family supports a broad range of interface standards, including DDR2/3, LPDDR2/3, XGMII and 7:1 LVDS.

The ECP5 Automotive device family also features high speed SERDES with dedicated Physical Coding Sublayer (PCS) functions. High jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE, XAUI, and SGMII), and CPRI. Transmit De-emphasis with pre- and post-cursors, and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

The ECP5 Automotive devices also provide flexible, reliable and secure configuration options, such as dual-boot capability, bit-stream encryption, and TransFR field upgrade features.

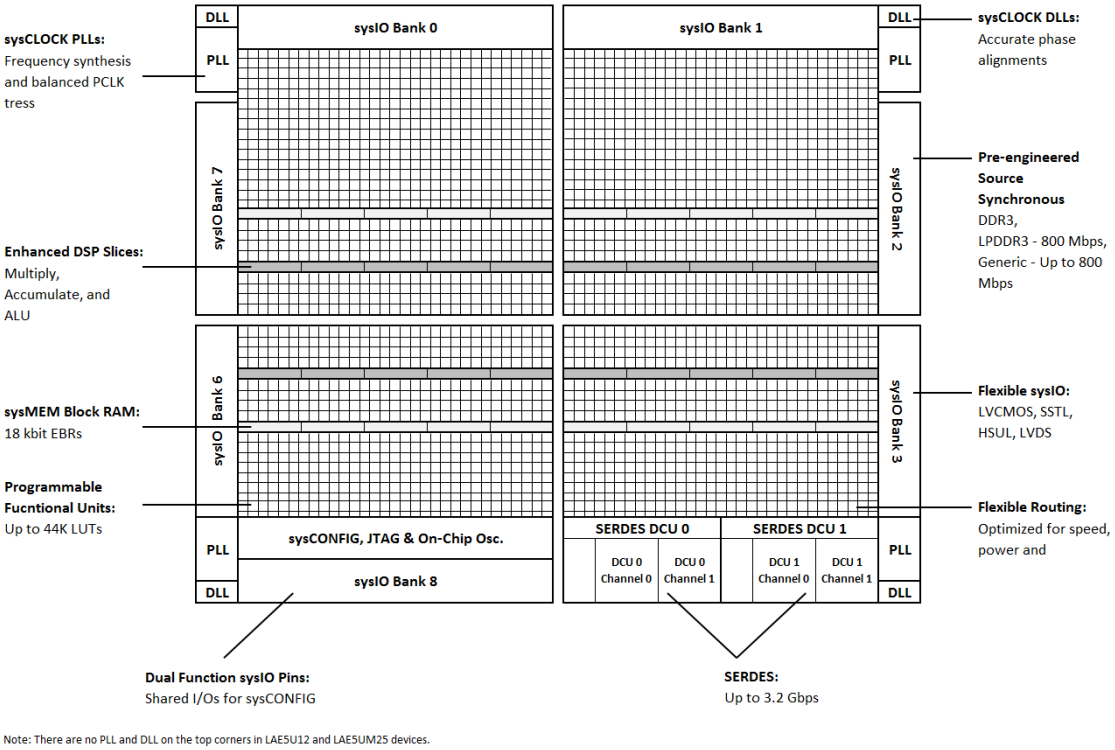
The Lattice Semiconductor Diamond™ design software allows large complex designs to be efficiently implemented using the ECP5 Automotive FPGA family. Synthesis library support for ECP5 Automotive devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the ECP5 Automotive device.

The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for the ECP5 Automotive family. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of the design, increasing their productivity.

1.1. Features

- Higher Logic Density for Increased System Integration
  - 12K to 44K LUTs
  - 197 to 203 user programmable I/Os
- Embedded SERDES
  - 270 Mb/s, up to 3.2 Gb/s, SERDES interface (ECP5)
  - Supports eDP in RDR (1.62 Gb/s) and HDR (2.7 Gb/s)
  - Up to four channels per device: PCI Express, Ethernet (1GbE, XAUI, and SGMII,), and CPRI
- sysDSP™
  - Fully cascadable slice architecture
  - 12 to 160 slices for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - Each slice supports
    - Half 36 x 36, two 18 x 18 or four 9 x 9 multipliers
    - Advanced 18 x 36 MAC and 18 x 18 Multiply-Multiply-Accumulate (MMAC) operations
- Flexible Memory Resources
  - Up to 1.944 Mb sysMEM™ Embedded Block RAM (EBR)
  - 194K to 351K bits distributed RAM
- sysCLOCK Analog PLLs and DLLs
  - Four DLLs and four PLLs in LAE5-45; two DLLs and two PLLs in LAE5-25 and LAE5-12
- Pre-engineered Source Synchronous I/O
  - DDR registers in I/O cells
  - Dedicated read/write levelling functionality
  - Dedicated gearing logic
  - Source synchronous standards support
    - ADC/DAC, 7:1 LVDS, XGMII
    - High Speed ADC/DAC devices



Note: There are no PLL and DLL on the top corners in LAE5U12 and LAE5UM25 devices.

Figure 2.1. Simplified Block Diagram of LAE5UM-45 Device (Top Level)

2.2. PFU Blocks

The core of the ECP5 Automotive device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0 – 3 as shown in Figure 2.2. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic, or ROM functions. Table 2.1 shows the functions each slice can perform in different modes.

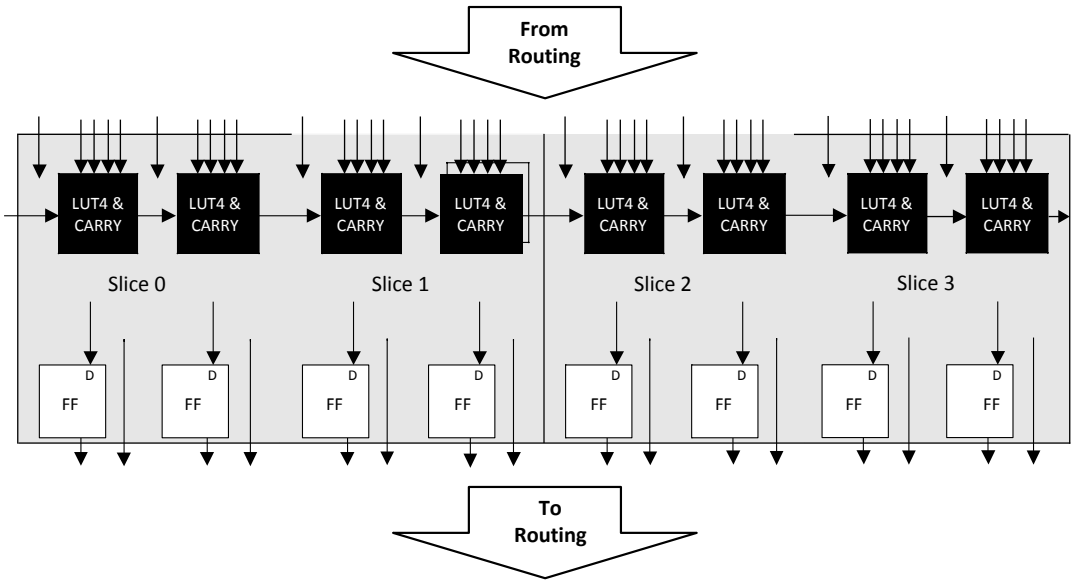


Figure 2.2. PFU Diagram

2.15. ECP5 Automotive sysDSP Slice Architecture Features

The ECP5 Automotive sysDSP Slice has been significantly enhanced to provide functions needed for advanced processing applications. These enhancements provide improved flexibility and resource utilization.

The ECP5 Automotive sysDSP Slice supports many functions that include the following:

- Fully double data rate support. Higher operation frequency (throughput of up to 370 Mb/s) is achieved by double input and output interfaces that enable twice the fabric operation throughput for most of the operation modes.
- Symmetry support. The primary target application is wireless. 1D Symmetry is useful for many applications that use FIR filters when their coefficients have symmetry or asymmetry characteristics. The main motivation for using 1D symmetry is cost/size optimization. The expected size reduction is up to 2x.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
  - Two dimensional (2D) symmetry mode – Supports 2D filters for mainly video applications
- Dual-multiplier architecture. Lower accumulator overhead to half and the latency to half compared to single multiplier architecture.
- Fully cascadable DSP across slices. Support for symmetric, asymmetric, and non-symmetric filters.
- Multiply function supports one 18x36, two 18x18, or four 9x9 multipliers per slice.
- Multiply function with the 36x36 multiplier uses two sysDSP slices.
- Multiply Accumulate supports one 18x36 multiplier result accumulation or two 18x18 multiplier result accumulation
- Two multipliers feeding one Accumulate per cycle for increased processing with lower latency (two 18x18 multipliers feed into an accumulator that can accumulate up to 52 bits)
- Pipeline registers
- 1D Symmetry support. The coefficients of FIR filters have symmetry or negative symmetry characteristics.
  - Odd mode – Filter with Odd number of taps
  - Even mode – Filter with Even number of taps
- 2D Symmetry support. The coefficients of 2D FIR filters have symmetry or negative symmetry characteristics.
  - 3*3 and 3*5 – Internal DSP Slice support
  - 5*5 and larger size 2D blocks – Semi-internal DSP Slice support
- Flexible saturation and rounding options to satisfy a diverse set of applications situations
- Flexible cascading across DSP slices
  - Minimizes fabric use for common DSP and ALU functions
  - Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  - Provides matching pipeline registers
  - Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and Powerful Arithmetic Logic Unit (ALU) supports:
  - Dynamically selectable ALU OPCODE
  - Ternary arithmetic addition/subtraction of three inputs
  - Bit-wise two-input logic operations such as AND, OR, NAND, NOR, XOR, and XNOR
  - Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as overflow, underflow and convergent rounding.
  - Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2.14 on the next page, the ECP5 Automotive sysDSP slice is backwards-compatible with the LatticeECP2™ and LatticeECP3™ sysDSP block, such that, legacy applications can be targeted to the ECP5 Automotive sysDSP slice. Figure 2.14 shows the diagram of sysDSP. Figure 2.15 shows the detailed diagram.

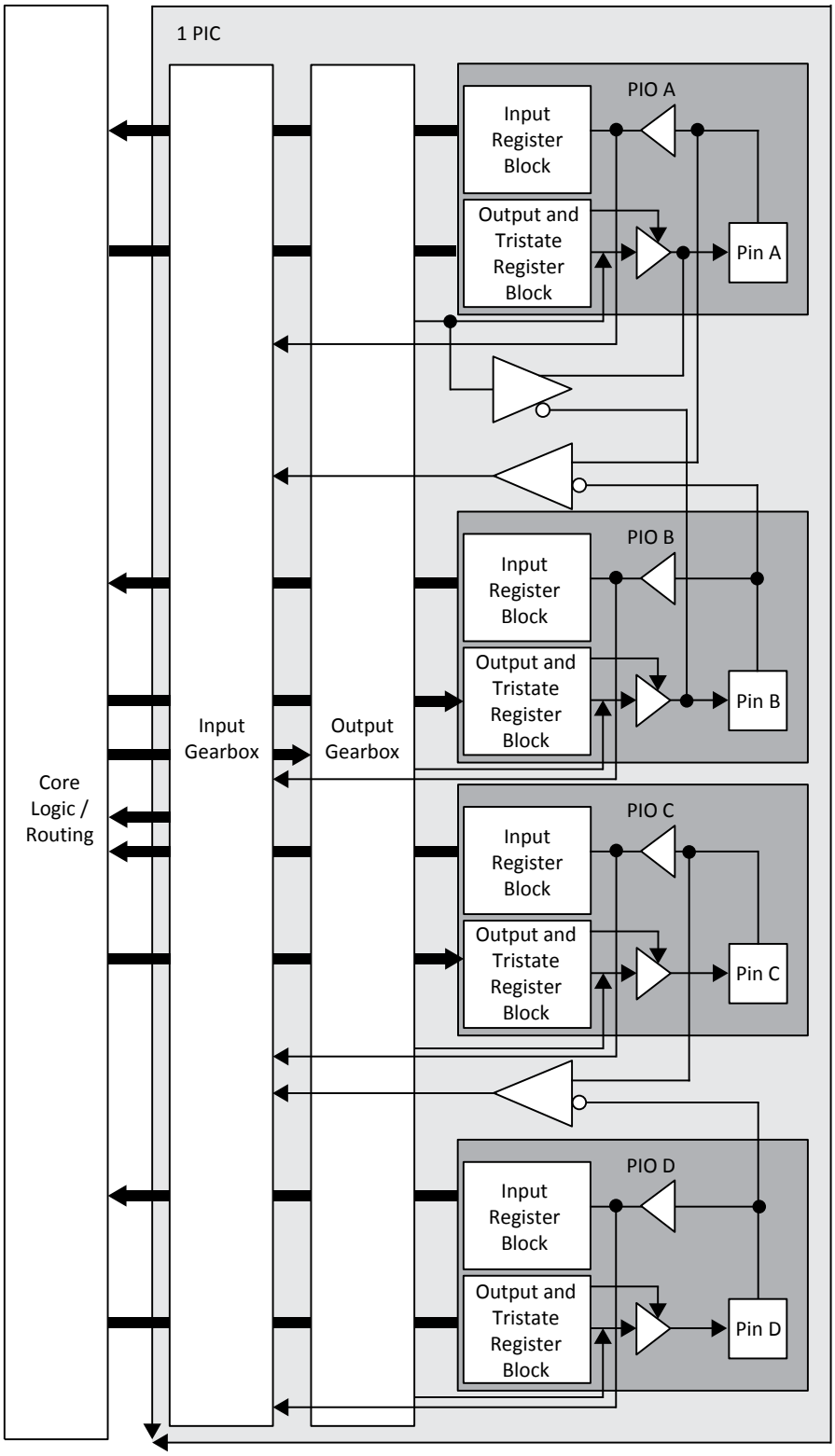


Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Side

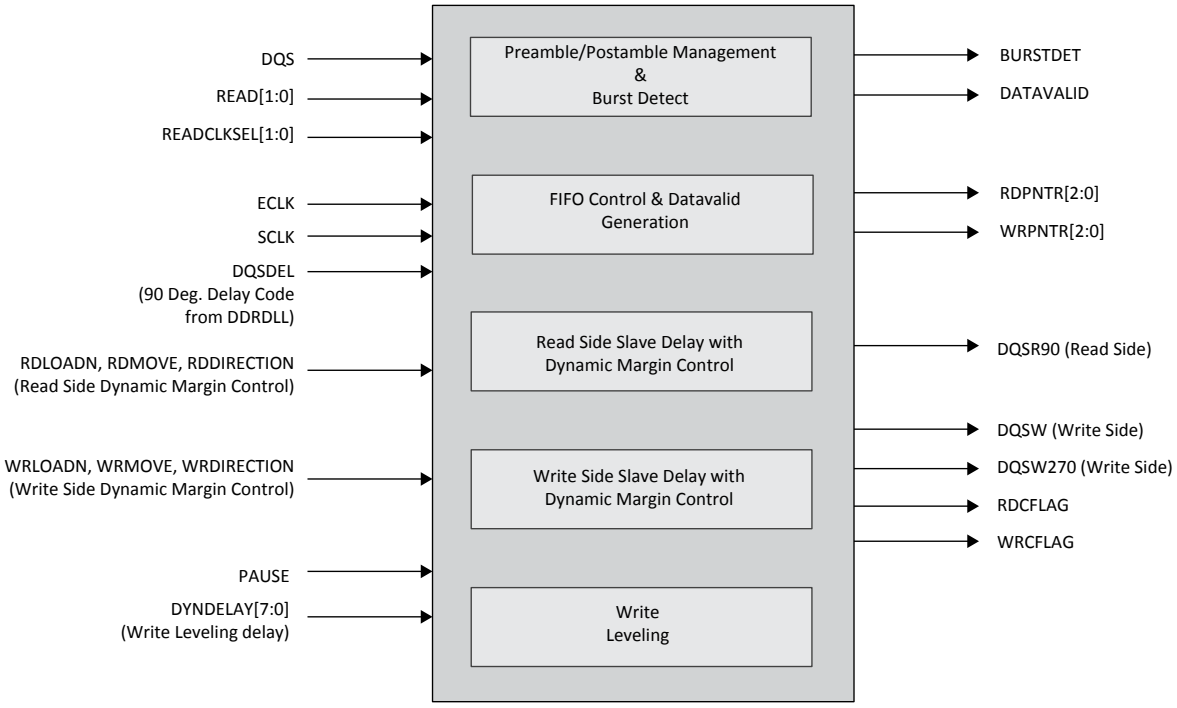


Figure 2.24. DQS Control and Delay Block (DQSBUF)

Table 2.11. DQSBUF Port list description

Name	Type	Description
DQS	Input	DDR memory DQS strobe
READ[1:0]	Input	Read Input from DDR controller
READCLKSEL[1:0]	Input	Read pulse selection
SCLK	Input	Slow system clock
ECLK	Input	High speed edge clock with the same frequency as that of the DDR memory)
DQSDEL	Input	90-degree delay code from DDRDLL
RDLOADN, RDMOVE, RDDIRECTION	Input	Dynamic margin control ports for Read delay
WRLOADN, WRMOVE, WRDIRECTION	Input	Dynamic margin control ports for Write delay
PAUSE	Input	Used by DDR controller to pause write side signals during DDRDLL code update or Write leveling
DYNDELAY[7:0]	Input	Dynamic Write leveling delay control
DQSR90	Output	90-degree delay DQS used for Read
DQSW270	Output	90-degree delay clock used for DQ Write
DQSW	Output	Clock used for DQS Write
RDPNTR[2:0]	Output	Read pointer for IFIFO module
WRPNTR[2:0]	Output	Write pointer for IFIFO module
DATAVALID	Output	Signal indicating start of valid data
BURSTDET	Output	Burst detect indicator
RDFLAG	Output	Read dynamic margin control output to indicate max value
WRFLAG	Output	Write dynamic margin control output to indicate max value

ECP5 Automotive devices contain two types of sysI/O buffer pairs:

- Top, Bank 0 and Bank 1, and Bottom, Bank 8 and Bank 4, single-ended sysIO Buffer Pairs

  The sysI/O buffers in the Banks at top and bottom of the device consist of ratioed single-ended output drivers and single-ended input buffers. The I/Os in these banks are not usually used as a pair, except when used as emulated differential output pair. They are used as individual I/Os and are configured as different I/O modes, as long as they are compatible with the V_{CCIO} voltage in the bank. When used as emulated differential outputs, the pair can be used together.

  The top or bottom side IOs also support hot socketing. They support IO standards from 3.3 V to 1.2 V. They are ideal for general purpose I/Os, or as ADDR/CMD bus for DDR2/DDR3 applications, or for being used as emulated differential signaling.

  Bank 8 is a bottom bank that shares with sysConfig I/Os. During configuration, these I/Os are used for programming the device. Once the configuration is completed, these I/Os can be released and user can use these I/Os for functional signals in his design.

  The top and bottom side pads can be identified by the Lattice Semiconductor Diamond tool.

- Left and right banks have 50% differential sysI/O buffer pairs and 100% single-ended outputs.

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two single-ended input buffers, both ratioed and referenced, and half of the sysI/O buffer pairs, PIOA/B pairs. Also has a high-speed differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

  In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

  LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.20.2. Typical sysI/O I/O Behavior during Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in ECP5 Automotive devices, see the list of technical documentation in Supplemental Information section on page 96.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

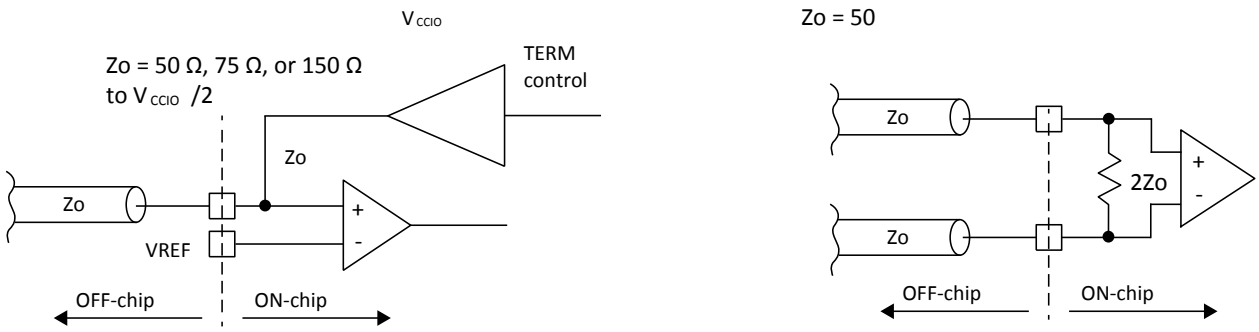
2.20.3. Supported sysI/O Standards

The ECP5 Automotive sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSUL. Differential standards supported include LVDS, differential SSTL and differential HSUL. For further information on utilizing the sysI/O buffer to support a variety of standards, refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide.

2.20.4. On-Chip Programmable Termination

The ECP5 Automotive devices support a variety of programmable on-chip terminations options including:

- Dynamically switchable Single-ended Termination with programmable resistor values of 50 Ω, 75 Ω, or 150 Ω.
- Common mode termination of 100 Ω for differential inputs.



Parallel Single-Ended Input **Differential Input**

Figure 2.26. On-chip Termination

See Table 2.12 for termination options for input modes.

Table 2.12. On-Chip Termination Options for Input Modes

IO_TYPE	Terminate to $V_{CCIO}/2$*	Differential Termination Resistor*
LVDS25	—	100
BLVDS25	—	100
MLVDS	—	100
LVPECL33	—	100
subLVDS	—	100
SLVS	—	100
HSUL12	50, 75, 150	—
HSUL12D	—	100
SSTL135_I / II	50, 75, 150	—
SSTL135D_I / II	—	100
SSTL15_I / II	50, 75, 150	—
SSTL15D_I / II	—	100
SSTL18_I / II	50, 75, 150	—
SSTL18D_I / II	—	100

***Note**:

TERMINATE to single-ended $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only left and right banks have this feature.

Use of TERMINATE to $V_{CCIO}/2$ and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank. On-chip termination tolerance ±20%.

Refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide for on-chip termination usage and value ranges.

2.20.5. Hot Socketing

ECP5 Automotive devices have been carefully designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled within specified limits. See the Hot Socketing Specifications section on page 47.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update, the ECP5 Automotive devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the ECP5 Automotive device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide.

2.24.2. Single Event Upset (SEU) Support

ECP5 Automotive devices support SEU mitigation with three supporting functions:

- SED – Soft Error Detect
- SEC – Soft Error Correction
- SEI – Soft Error Injection

ECP5 Automotive devices have dedicated logic to perform Cycle Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, the ECP5 Automotive device can also be programmed to utilize a Soft Error Detect (SED) mode that checks for soft errors in configuration SRAM. The SED operation can be run in the background during user mode. If a soft error occurs, during user mode, normal operation, the device can be programmed to generate an error signal.

When an error is detected, and the user's error handling software determines the error did not create any risk to the system operation, the SEC tool allows the device to be re-configured in the background to correct the affected bit. This operation allows the user functions to continue to operate without stopping the system function.

Additional SEI tool is also available in the Diamond Software, by creating a frame of data to be programmed into the device in the background with one bit changed, without stopping the user functions on the device. This emulates an SEU situation, allowing the user to test and monitor its error handling software.

For further information on SED support, refer to TN1184, LatticeECP3, ECP5 and ECP5-5G Soft Error Detection (SED)/Correction (SEC) Usage Guide.

2.24.3. On-Chip Oscillator

Every ECP5 Automotive device has an internal CMOS oscillator which is used to derive a Master Clock (MCLK) for configuration. The oscillator and the MCLK run continuously and are available to user logic after configuration is completed. The software default value of the MCLK is nominally 2.4 MHz. Table 2.16 lists all the available MCLK frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal Master Clock frequency of 2.4 MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.4 MHz.

This internal oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, refer to TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide.

Table 2.16. Selectable Master Clock (MCLK) Frequencies during Configuration (Nominal)

MCLK Frequency (MHz)
2.4
4.8
9.7
19.4
38.8
62

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	1.21	V
V_{CCA}	Supply Voltage	–0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	2.75	V
V_{CCIO}	Supply Voltage	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	–0.5	1.32	V
—	Voltage Applied on SERDES Pins	–0.5	1.80	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Semiconductor Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter	Device	Min	Max	Unit
V_{CC}[2]	Core Supply Voltage	All	1.045	1.155	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage	All	2.375	2.625	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	All	1.14	3.465	V
V_{REF}[1]	Input Reference Voltage	All	0.5	1.0	V
t_{JAUTO}	Junction Temperature, Industrial Operation	All	–40	125	°C
SERDES External Power Supply[5]					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	All	2.374	2.625	V
V_{CCHRX}[6]	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 .
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the SERDES Power Supply Requirements section of this Data Sheet.

3.10. Standby ECP5 Automotive Supply Current

Over recommended operating conditions.

Table 3.8. Standby ECP5 Automotive Supply Current

Symbol	Parameter	Device	Typical	Unit
I_{CC}	Core Power Supply Current	LAE5U-12FLAE5UM-25F	77	mA
		LAE5UM-45F	116	mA
I_{CCAUX}	Auxiliary Power Supply Current	LAE5U-12F/ LAE5UM-25F	16	mA
		LAE5UM-45F	17	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	LAE5U-12F/ LAE5UM-25F	0.5	mA
		LAE5UM-45F	0.5	mA
I_{CCA}	SERDES Power Supply Current (Per Dual)	LAE5UM-25F	11	mA
		LAE5UM-45F	9.5	mA

Notes:

- For further information on supply current, see the list of technical documentation in the Supplemental Information section on page 96.
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 Hz.
- Pattern represents a “blank” configuration data file.
- T_J = 85 °C, power supplies at nominal voltage.
- To determine the ECP5 Automotive peak start-up current, use the Power Calculator tool in the Lattice Semiconductor Diamond Design Software.

Table 3.20. ECP5 Automotive External Switching Characteristics *(Continued)*

Parameter	Description	Device	–6		Unit
			Min	Max	
Generic DDR Output					
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.8					
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9					
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8					
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9					
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12					
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.2	—	ns + (i) UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.2	ns + (i) UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	262.5	MHz
Memory Interface					
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)					
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.374	—	ns + 1/2 UI

3.22. SERDES High-Speed Data Receiver

Table 3.25. Serial Input Data Specifications

Symbol	Description	Min	Typ	Max	Unit
$V_{RX-DIFF-S}$	Differential input sensitivity	150	—	1760	mV, p-p
V_{RX-IN}	Input levels	0	—	V_{CCA} +0.5[2]	V
$V_{RX-CM-DCCM}$	Input common mode range (internal DC coupled mode)	0.6	—	V_{CCA}	V
$V_{RX-CM-ACCM}$	Input common mode range (internal AC coupled mode)[2]	0.1	—	V_{CCA} +0.2	V
$T_{RX-RELOCK}$	SCDR re-lock time[1]	—	1000	—	Bits
$Z_{RX-TERM}$	Input termination 50/75 Ω /High Z	–20%	50/75/5 K	+20%	Ω
RL_{RX-RL}	Return loss without package	—	—	–10	dB

Notes:

1. This is the typical number of bit times to re-lock to a new phase or frequency within ±300 ppm, assuming 8b10b encoded data.
2. Up to 1.655 for ECP5.

3.23. Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3.26. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min	Typ	Max	Unit
Deterministic	3.125 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gb/s	400 mV differential eye	—	—	0.37	UI, p-p
Random		400 mV differential eye	—	—	0.18	UI, p-p
Total		400 mV differential eye	—	—	0.65	UI, p-p

Note:

Jitter tolerance measurements are done with protocol compliance tests: 3.125 Gb/s - XAUI Standard, 2.5 Gb/s - PCIe Standard, 1.25 Gb/s - SGMII Standard.

3.24. SERDES External Reference Clock

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3.27 specifies reference clock requirements over the full range of operating conditions.

Table 3.27. External Reference Clock Specification (refclkp/refclkn)[5]

Symbol	Description	Min	Typ	Max	Unit
F_{REF}	Frequency range	50	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	–1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2, 4]	200	—	V_{CCAUXA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCAUXA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCAUXA} + 0.4	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	–30%	100/HiZ	+30%	Ω
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

Notes:

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide.
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. With single-ended clock, a reference voltage needs to be externally connected to CLKREFN pin, and the input voltage needs to be swung around this reference voltage.
3. Measured at 50% amplitude.
4. Single-ended clocking is achieved by applying a reference voltage V_{REF} on REFCLKN input, with the clock applied to REFCLKP input pin. V_{REF} should be set to mid-point of the REFCLKP voltage swing.
5. refclkp and refclkn are standard external reference clock inputs.

Signal Name	I/O	Description
Configuration Pads (Used during sysCONFIG) *(Continued)*		
D1/MISO/IO1	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an input in Master mode, and output in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D2/IO2	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D3/IO3	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D4/IO4	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D5/IO5	I/O	Parallel configuration I/O. Open drain during configuration. This is a shared I/ O pin. When not in configuration, it can be used as general purpose I/O pin.
D6/IO6	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin.
D7/IO7	I/O	Parallel configuration I/O. Open drain during configuration. When in SPI modes, it is an output in Master mode, and input in Slave mode. This is a shared I/O pin. When not in configuration, it can be used as general purpose I/O pin
SERDES Function		
V_{CCAx}	—	SERDES, transmit, receive, PLL and reference clock buffer power supply for SERDES Dual x. All V_{CCA} supply pins must always be powered to the recommended operating voltage range. If no SERDES channels are used, connect V_{CCA} to V_{CC}. V_{CCAx} = 1.1 V for ECP5
$V_{CCAUXAx}$	—	SERDES Aux Power Supply pin for SERDES Dual x. $V_{CCAUXAx}$ = 2.5 V.
HDRX[P/N]_D[dual_num]CH[chan_num]	I	High-speed SERDES inputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES input pins.
HDTX[P/N]_D[dual_num]CH[chan_num]	O	High-speed SERDES outputs, P = Positive, N = Negative, dual_num = [0, 1], chan_num = [0, 1]. These are dedicated SERDES output pins.
REFCLK[P/N]_D[dual_num]	I	SERDES Reference Clock inputs, P = Positive, N = Negative, dual_num = [0, 1]. These are dedicated SERDES input pins.
VCCHRX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Inputs Termination Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5.
VCCHTX_D[dual_num]CH[chan_num]	—	SERDES High-Speed Outputs Buffer Voltage Supplies, dual_num = [0, 1], chan_num = [0, 1]. These pins should be powered to 1.1 V on ECP5.

Notes:

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. num defines the associated channel in the quad.

4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device Only		
P[L/R] [n−6]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n−3]	A	DQ
	B	DQ
	C	DQ
	D	DQ
P[L/R] [n]	A	DQS (P)
	B	DQS (N)
	C	DQ
	D	DQ
P[L/R] [n+3]	A	DQ
	B	DQ
	C	DQ
	D	DQ

Note: “n” is a row PIC number.