Lattice Semiconductor Corporation - LAE5UM-45F-7BG381E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5500
Number of Logic Elements/Cells	44000
Total RAM Bits	1990656
Number of I/O	203
Number of Gates	-
Voltage - Supply	1.04V ~ 1.155V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	381-FBGA
Supplier Device Package	381-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae5um-45f-7bg381e

Figures

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ALU	Arithmetic Logic Unit
BGA	Ball Grid Array
CDR	Clock and Data Recovery
CRC	Cycle Redundancy Code
DCC	Dynamic Clock Control
DCS	Dynamic Clock Select
DDR	Double Data Rate
DLL	Delay Locked Loops
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECLK	Edge Clock
FFT	Fast Fourier Transforms
FIFO	First In First Out
FIR	Finite Impulse Response
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
LUT	Look Up Table
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PIO	Programmable I/O
PLL	Phase Locked Loops
POR	Power On Reset
SCI	SERDES Client Interface
SCM	Serial Configuration Mode
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPCM	Slave Parallel Configuration Mode
SPI	Serial Peripheral Interface
SPR	Single Port RAM
SRAM	Static Random-Access Memory
TAP	Test Access Port
TDM	Time Division Multiplexing

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to TN1264, ECP5 and ECP5-5G Memory Usage Guide.

2.3. Routing

There are many resources provided in the ECP5 Automotive devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect segments.

The ECP5 Automotive family has an enhanced routing architecture that produces a compact design. The Diamond design software tool suites take the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

ECP5 Automotive clocking structure consists of:

- Clock synthesis blocks and sysCLOCK PLL;
- Balanced clock tress networks, PCLK, and ECLK trees;
- Efficient clock logic modules, CLOCK DIVIDER and Dynamic Clock Select (DCS), Dynamic Clock Control (DCC), and DLL.

Each of these functions is described as follows.

2.5. sysCLOCK PLL

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The devices in the ECP5 Automotive family support two to four full-featured General Purpose PLLs. The sysCLOCK PLLs provide the ability to synthesize clock frequencies.

The architecture of the PLL is shown in Figure 2.5. Following is the description of the PLL functionality.

- CLKI is the reference frequency input to the PLL and its source can come from two different external CLK inputs or from internal routing. A non-glitchless 2-to-1 input multiplexor is provided to dynamically select between two different external reference clock sources. The CLKI input feeds into the input Clock Divider block.
- CLKFB is the feedback signal to the PLL that can come from internal feedback path, routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.
- The PLL has four clock outputs CLKOP, CLKOS, CLKOS2, and CLKOS3. Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network.
- The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. This phase shift can be either programmed during configuration or can be adjusted dynamically using the PHASESEL, PHASEDIR, PHASESTEP, and PHASELOADREG ports.
- The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected.

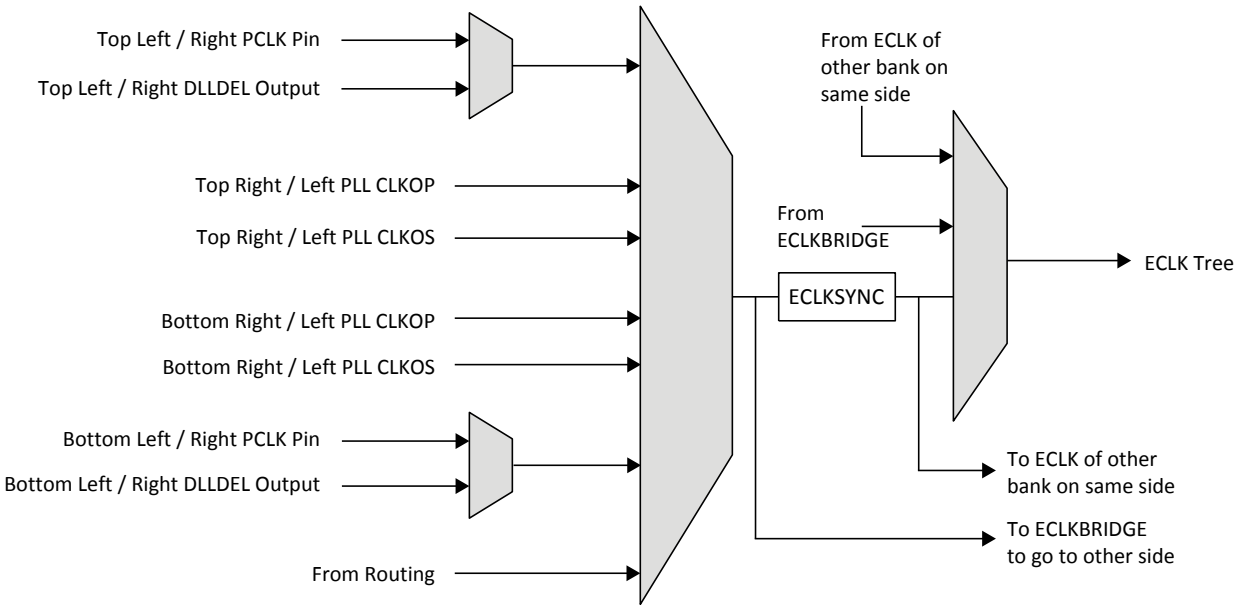


Figure 2.8. Edge Clock Sources per Bank

The edge clocks have low injection delay and low skew. They are used for DDR Memory or Generic DDR interfaces. For detailed information on Edge Clock connections, refer to TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide.

2.11. Clock Dividers

ECP5 Automotive devices have two clock dividers, one on the left side and the other on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷3.5 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal.

The clock dividers can be fed from selected PLL outputs, external primary clock pins multiplexed with the DDRDEL Slave Delay or from routing. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The SLIP signal slips the outputs one cycle relative to the input clock. For further information on clock dividers, refer to TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide. Figure 2.9 shows the clock divider connections.

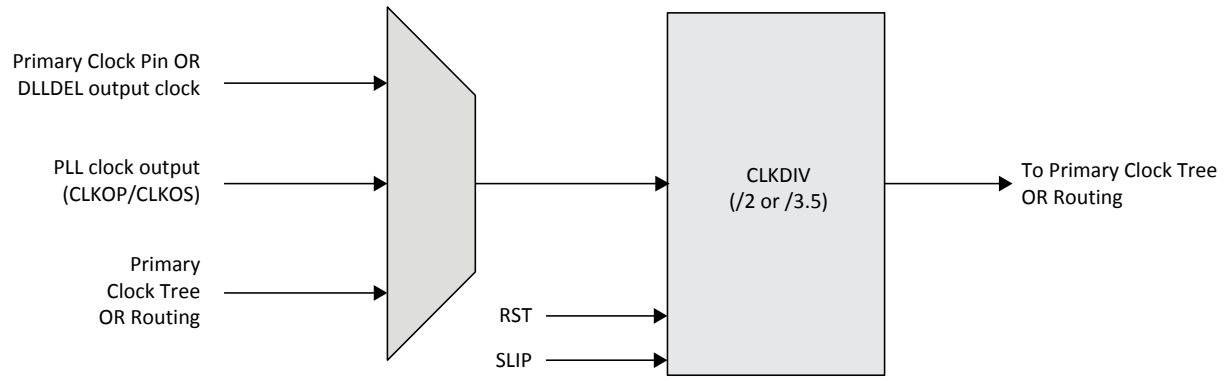


Figure 2.9. ECP5 Automotive Clock Divider Sources

2.12. DDRDLL

Every DDRDLL (master DLL block) can generate phase shift code representing the amount of delay in a delay block that corresponding to 90-degree phase of the reference clock input. The reference clock can be either from PLL, or input pin. This code is used in the DQSBUF block that controls a set of DQS pin groups to interface with DDR memory (slave DLL). There are two DDRDLLs that supply two sets of codes (for two different reference clock frequencies) to each side of the I/Os (at each of the corners). The DQSBUF uses this code to controls the DQS input of the DDR memory to 90-degree shift to clock DQs at the center of the data eye for DDR memory interface.

The code is also sent to another slave DLL and DLLDEL, which takes a clock input, and generates a 90-degree shift clock output to drive the clocking structure. This is useful to interface edge-aligned Generic DDR, where 90-degree clocking needs to be created. Figure 2.10 shows DDRDLL functional diagram.

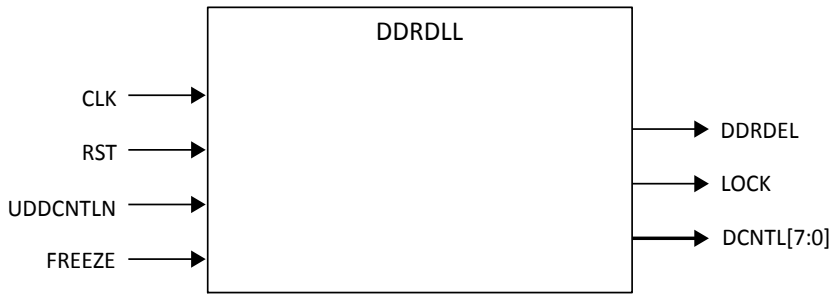


Figure 2.10. DDRDLL Functional Diagram

Table 2.5. DDRDLL Ports List

Port Name	Type	Description
CLK	Input	Reference clock input to the DDRDLL. Should run at the same frequency as the clock to the delayed.
RST	Input	Reset Input to the DDRDLL.
UDDCNTLN	Input	Update Control to update the delay code. When UDDCNTLN goes LOW, the delay code out the DDRDLL is updated. Should not be active during a read or a write cycle.
FREEZE	Input	FREEZE goes HIGH and, without a glitch, turns off the DLL internal clock and the ring oscillator output clock. When FREEZE goes LOW, it turns them back on.
DDRDEL	Output	The delay codes from the DDRDLL to be used in DQSBUF or DLLDEL.
LOCK	Output	Lock output to indicate the DDRDLL has valid delay output.
DCNTL [7:0]	Output	The delay codes from the DDRDLL available for the user IP.

There are identical DDRDLLs, four in each corner in LAE5-45 device and two in upper corners in both LAE5-25 and LAE5-12 devices. Each DDRDLL can generate delay code based on the reference frequency. The slave DLL, DQSBUF, and DLLDEL use the code to delay the signal, to create the phase shifted signal used for either DDR memory, or to create 90-degree shift clock. Figure 2.11 shows the DDRDLL and the slave DLLs on the top level view.

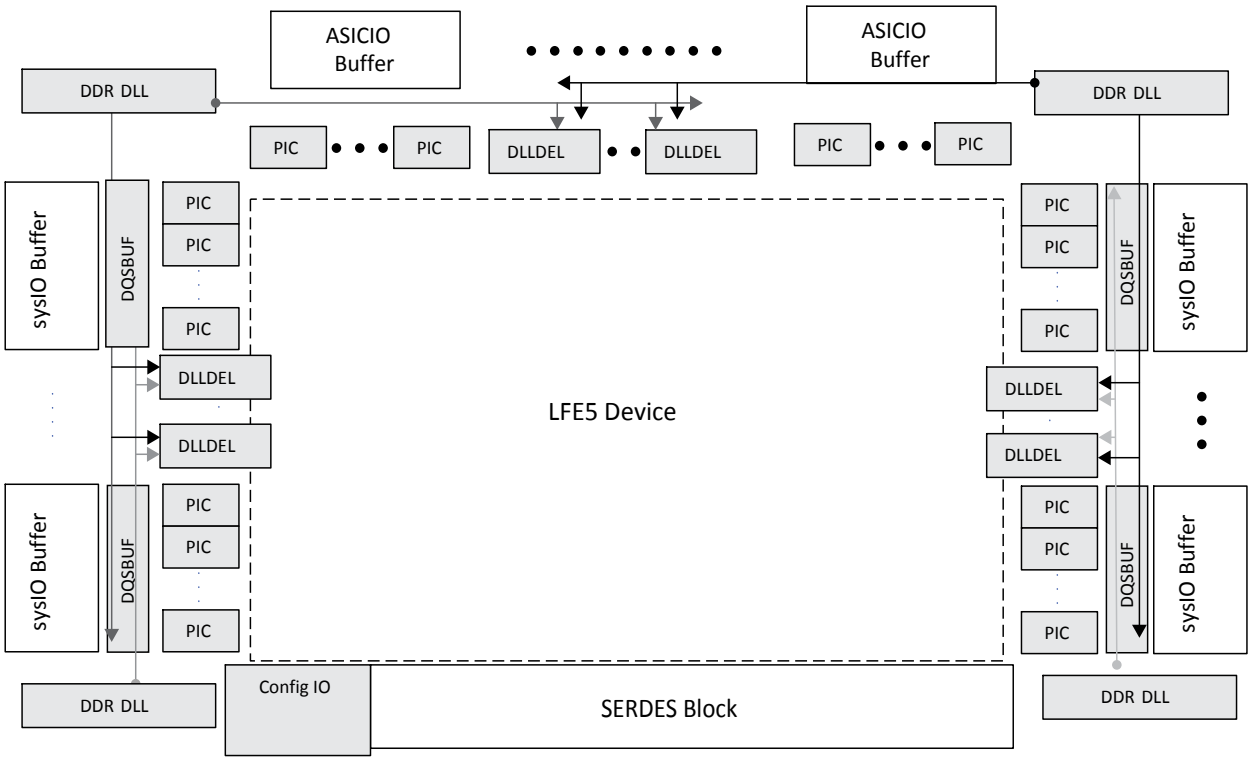


Figure 2.11. ECP5 Automotive DLL Top Level View for LFE-45

2.13. sysMEM Memory

ECP5 Automotive devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18 Kb RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM, and FIFO buffers via external PFUs.

2.13.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.6 on page 23. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths. For more information, refer to TN1264, ECP5 and ECP5-5G Memory Usage Guide.

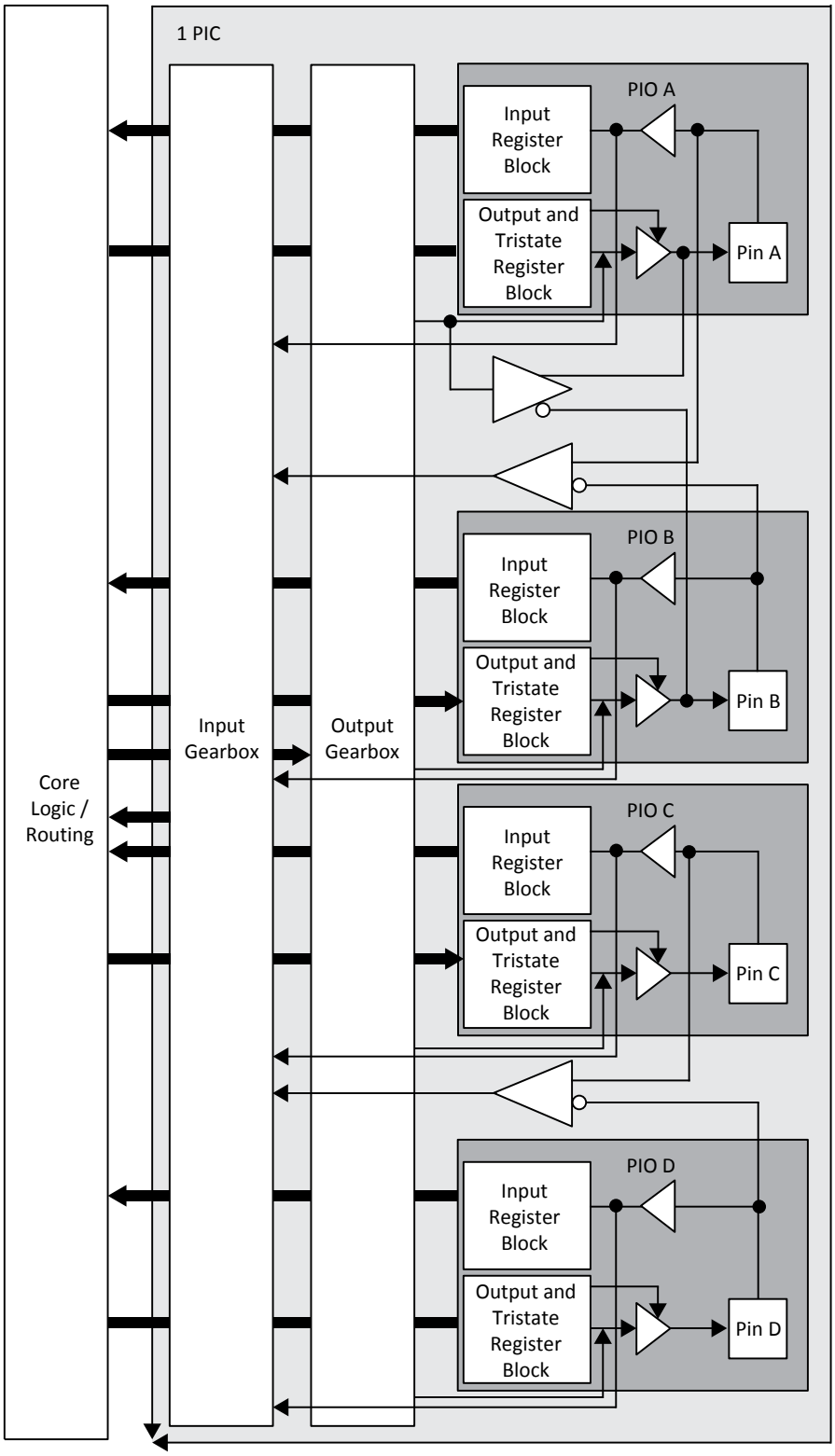


Figure 2.16. Group of Four Programmable I/O Cells on Left/Right Side

2.17. PIO

The PIO contains three blocks: an input register block, an output register block, and a tristate register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

2.17.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIOs on the left and right edges include built-in FIFO logic to interface to DDR and LPDDR memory.

The Input register block on the right and left sides includes gearing logic and registers to implement IDDRX1 and IDDRX2 functions. With two PICs sharing the DDR register path, it can also implement IDDRX71 function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. The Top side of the device will support IDDRX1 gearing function. For more information on gearing function, refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

Figure 2.17 shows the input register block for the PIOs on the top edge.

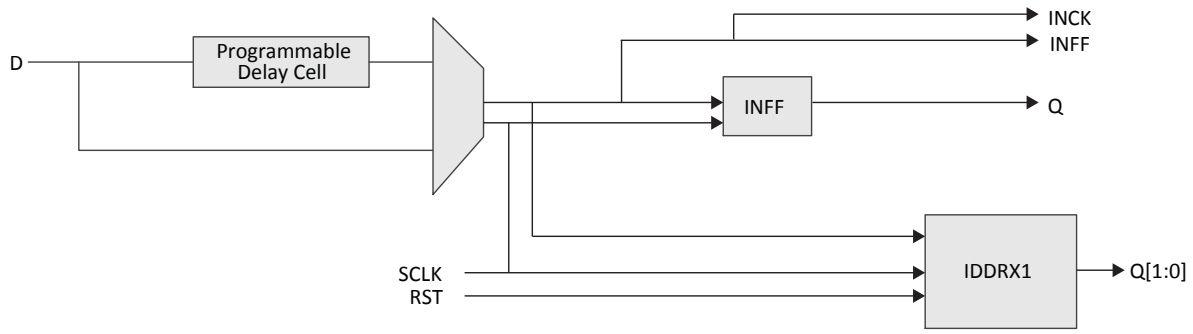
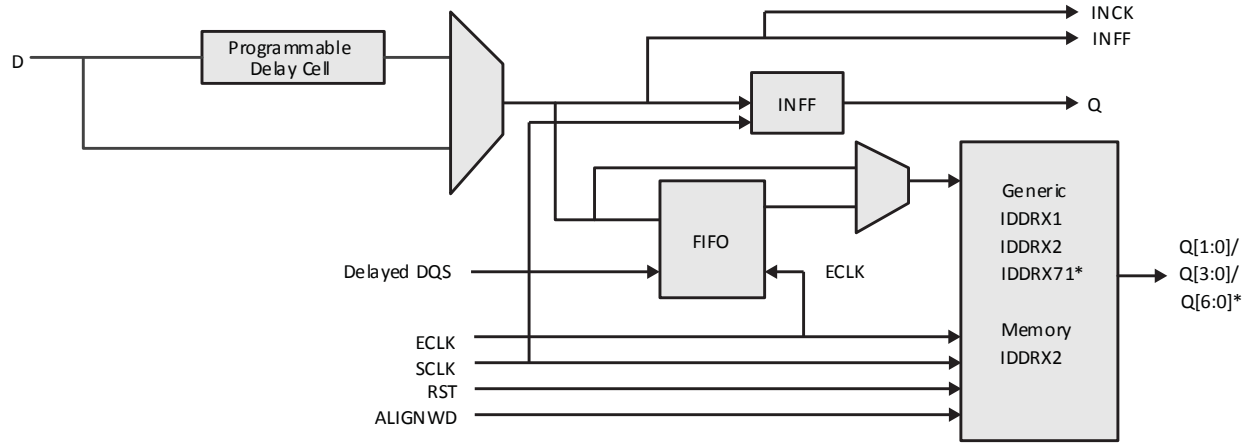


Figure 2.17. Input Register Block for PIO on Top Side of the Device

Figure 2.18 shows the input register block for the PIOs located on the left and right edges.



*Note: For 7:1 LVDS interface only. It is required to use PIO pair pins (PIOA/B or PIOC/D).

Figure 2.18. Input Register Block for PIO on Left or Right Side of the Device

2.17.1.1. Input FIFO

The ECP5 Automotive PIO has dedicated input FIFO per single-ended pin for input data register for DDR Memory interfaces. The FIFO resides before the gearing logic. It transfers data from DQS domain to continuous ECLK domain. On the Write side of the FIFO, it is clocked by DQS clock which is the delayed version of the DQS Strobe signal from DDR memory. On the Read side of FIFO, it is clocked by ECLK. ECLK may be any high speed clock with identical frequency as DQS (the frequency of the memory chip). Each DQS group has one FIFO control block. It distributes FIFO read/write pointer to every PIC in same DQS group. DQS Grouping and DQS Control Block is described in DDR Memory Support section on page 34.

Table 2.8. Input Block Port

Name	Type	Description
D	Input	High speed data input
Q[1:0]/Q[3:0]/Q[6:0]	Output	Low speed data to the device core
RST	Input	Reset to the output block
SCLK	Input	Slow speed system clock
ECLK	Input	High speed edge clock
DQS	Input	Clock from DQS control block used to clock DDR memory data
ALIGNWD	Input	Data alignment signal from device core

2.17.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers.

ECP5 Automotive output data path has output programmable flip flops and output gearing logic. On the left and right sides the output register block can support 1x, 2x and 7:1 gearing enabling high speed DDR interfaces and DDR memory interfaces. On the top side, the banks will support 1x gearing. ECP5 Automotive output data path diagram is shown in Figure 2.19. The programmable delay cells are also available in the output data path.

For detailed description of the output register block modes and usage, refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

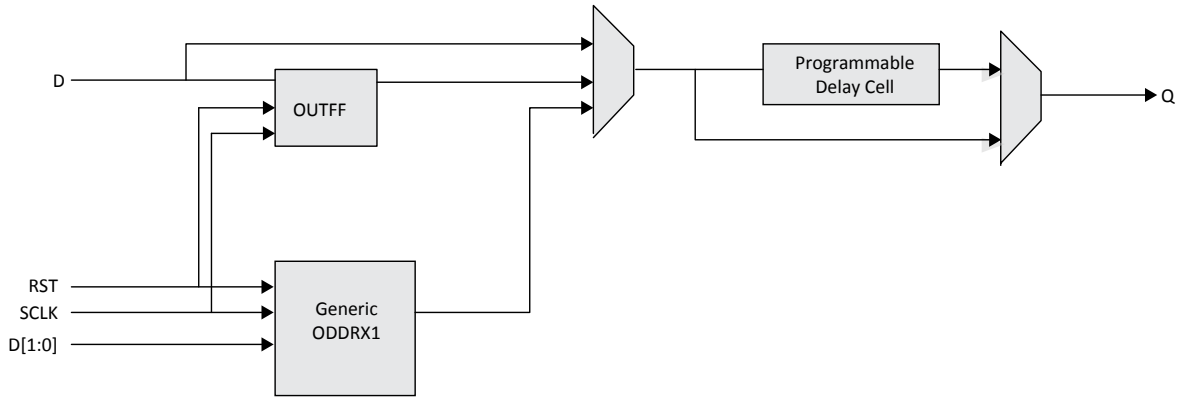
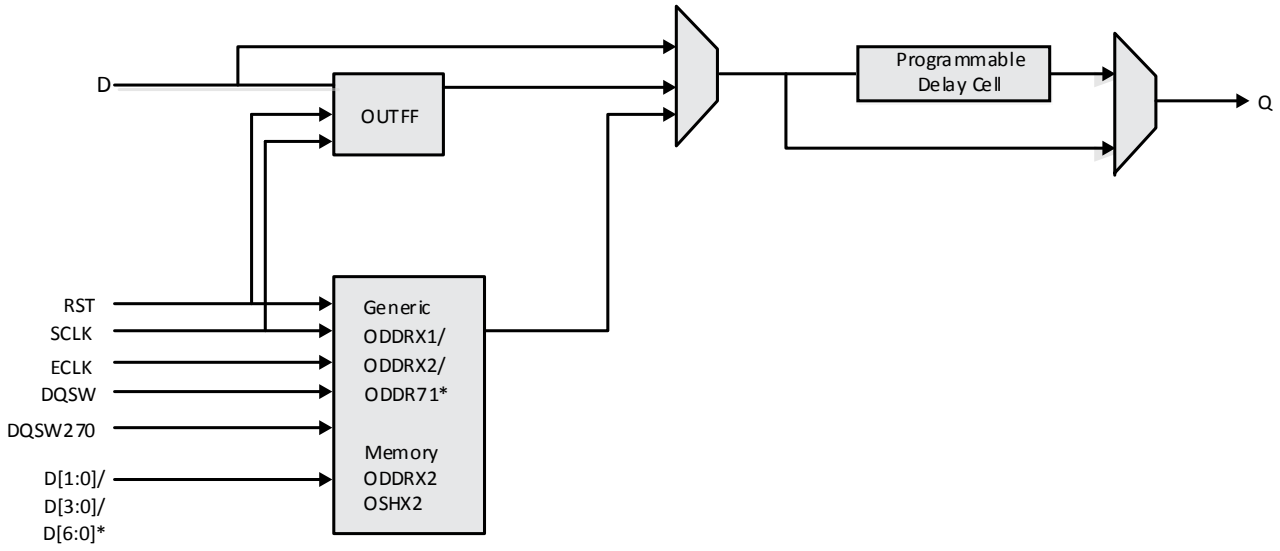


Figure 2.19. Output Register Block on Top Side



*Note: For 7:1 LVDS interface only. It is required to use PIO pair pins PIOA/B.

Figure 2.20. Output Register Block on Left or Right Side

Table 2.9. Output Block Port Description

Name	Type	Description
Q	Output	High Speed Data Output
D	Input	Data from core to output SDR register
D[1:0]/D[3:0]/ D[6:0]	Input	Low Speed Data from device core to output DDR register
RST	Input	Reset to the Output Block
SCLK	Input	Slow Speed System Clock
ECLK	Input	High Speed Edge Clock
DQSW	Input	Clock from DQS control Block used to generate DDR memory DQS output
DQSW270	Input	Clock from DQS control Block used to generate DDR memory DQ output

2.18. Tristate Register Block

The tristate register block registers tristate control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops, which feeds the output. DDR memory interface can be implemented on the left and right sides of the device. Here two inputs feed the tristate registers clocked by both ECLK and SCLK.

Figure 2.21 and Figure 2.22 show the Tristate Register Block functions on the device. For detailed description of the tristate register block modes and usage, refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

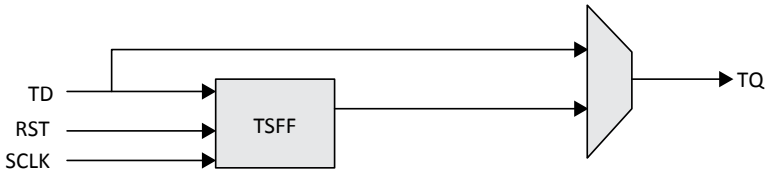


Figure 2.21. Tristate Register Block on Top Side

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.5	1.21	V
V_{CCA}	Supply Voltage	–0.5	1.32	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	2.75	V
V_{CCIO}	Supply Voltage	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCHRX}, V_{CCHTX}	SERDES RX/TX Buffer Supply Voltages	–0.5	1.32	V
—	Voltage Applied on SERDES Pins	–0.5	1.80	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Semiconductor Thermal Management document is required.
3. All voltages referenced to GND.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

Symbol	Parameter	Device	Min	Max	Unit
V_{CC}[2]	Core Supply Voltage	All	1.045	1.155	V
V_{CCAUX}[2, 4]	Auxiliary Supply Voltage	All	2.375	2.625	V
V_{CCIO}[2, 3]	I/O Driver Supply Voltage	All	1.14	3.465	V
V_{REF}[1]	Input Reference Voltage	All	0.5	1.0	V
t_{JAUTO}	Junction Temperature, Industrial Operation	All	–40	125	°C
SERDES External Power Supply[5]					
V_{CCA}	SERDES Analog Power Supply	ECP5UM	1.045	1.155	V
V_{CCAUXA}	SERDES Auxiliary Supply Voltage	All	2.374	2.625	V
V_{CCHRX}[6]	SERDES Input Buffer Power Supply	ECP5UM	0.30	1.155	V
V_{CCHTX}	SERDES Output Buffer Power Supply	ECP5UM	1.045	1.155	V

Notes:

1. For correct operation, all supplies except V_{REF} must be held in their valid operation range. This is true independent of feature usage.
2. All supplies with same voltage, except SERDES Power Supplies, should be connected together.
3. See recommended voltages by I/O standard in Table 3.4 .
4. V_{CCAUX} ramp rate must not exceed 30 mV/µs during power-up when transitioning between 0 V and 3 V.
5. Refer to TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide for information on board considerations for SERDES power supplies.
6. V_{CCHRX} is used for Rx termination. It can be biased to Vcm if external AC coupling is used. This voltage needs to meet all the HDin input voltage level requirements specified in the SERDES Power Supply Requirements section of this Data Sheet.

3.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33	–0.3	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	16, 12, 8, 4	–16, –12, –8, –4
LVCMOS25	–0.3	0.7	1.7	3.465	0.4	V_{CCIO} – 0.4	12, 8, 4	–12, –8, –4
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	12, 8, 4	–12, –8, –4
LVCMOS15	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	8, 4	–8, –4
LVCMOS12	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	8, 4	–8, –4
LVTTL33	–0.3	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	16, 12, 8, 4	–16, –12, –8, –4
SSTL18_I (DDR2 Memory)	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	3.465	0.4	V_{CCIO} – 0.4	6.7	–6.7
SSTL18_II	–0.3	V_{REF} –	V_{REF} + 0.125	3.465	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL15 _I (DDR3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.31	V_{CCIO} – 0.31	7.5	–7.5
SSTL15_II (DDR3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.31	V_{CCIO} – 0.31	8.8	–8.8
SSTL135_I (DDR3L Memory)	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	3.465	0.27	V_{CCIO} – 0.27	7	–7
SSTL135_II (DDR3L Memory)	–0.3	V_{REF} – 0.09	V_{REF} + 0.09	3.465	0.27	V_{CCIO} – 0.27	8	–8
MIPI D-PHY (LP)	–0.3	0.55	0.88	3.465	—	—	—	—
HSUL12 (LPDDR2/3 Memory)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	3.465	0.3	V_{CCIO} – 0.3	4	–4

Notes:

1. For electromigration, the average DC current drawn by the I/O pads within a bank of I/Os shall not exceed 10 mA per I/O. All I/Os are used in the same V_{CCIO}.
2. Not all IO types are supported in all banks. Refer to TN1262, ECP5 and ECP5-5G sysIO Usage Guide for details.

3.17. ECP5 Automotive Maximum I/O Buffer Speed

Over recommended operating conditions.

Table 3.19. ECP5 Automotive Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	400	MHz
MIPI D-PHY (HS Mode)	MIPI Video	400	MHz
SLVS	SLVS similar to MIPI	400	MHz
Mini LVDS	Mini LVDS	400	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	400	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL_12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	200	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	200	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	200	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	200	MHz
LVCMOS15	LVCMOS 1.5, V_{CCIO} = 1.5 V	200	MHz
LVCMOS12	LVCMOS 1.2, V_{CCIO} = 1.2 V	200	MHz
Maximum Output Frequency			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	300	MHz
LVDS25	LVDS, V_{CCIO} = 2.5 V	400	MHz
MLVDS25	MLVDS, Emulated, V_{CCIO} = 2.5 V	300	MHz
BLVDS25	BLVDS, Emulated, V_{CCIO} = 2.5 V	300	MHz
LVPECL33	LVPECL, Emulated, V_{CCIO} = 3.3 V	300	MHz
SSTL18 (all supported classes)	SSTL_18 class I, II, V_{CCIO} = 1.8 V	400	MHz
SSTL15 (all supported classes)	SSTL_15 class I, II, V_{CCIO} = 1.5 V	400	MHz
SSTL135 (all supported classes)	SSTL_135 class I, II, V_{CCIO} = 1.35 V	400	MHz
HSUL12 (all supported classes)	HSUL12 class I, II, V_{CCIO} = 1.2 V	400	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	150	MHz
LVCMOS33 (For all drives)	LVCMOS, 3.3 V	150	MHz
LVCMOS25 (For all drives)	LVCMOS, 2.5 V	150	MHz
LVCMOS18 (For all drives)	LVCMOS, 1.8 V	150	MHz
LVCMOS15 (For all drives)	LVCMOS, 1.5 V	150	MHz
LVCMOS12 (For all drives)	LVCMOS, 1.2 V	150	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Switching Test Conditions, Table 3.41 on page 87.
4. All speeds are measured at fast slew.
5. Actual system operation may vary depending on user logic implementation.
6. Maximum data rate equals 2 times the clock rate when utilizing DDR.

Table 3.20. ECP5 Automotive External Switching Characteristics *(Continued)*

Parameter	Description	Device	–6		Unit
			Min	Max	
Generic DDR Output					
Generic DDRX1 Outputs With Clock and Data Centered at Pin (GDDRX1_TX.SCLK.Centered) Using PCLK Clock Input - Figure 3.8					
$t_{DVB\_GDDRX1\_centered}$	Data Output Valid before CLK Output	All Devices	–0.67	—	ns + 1/2 UI
$t_{DVA\_GDDRX1\_centered}$	Data Output Valid after CLK Output	All Devices	–0.67	—	ns + 1/2 UI
$f_{DATA\_GDDRX1\_centered}$	GDDRX1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX\_GDDRX1\_centered}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX1 Outputs With Clock and Data Aligned at Pin (GDDRX1_TX.SCLK.Aligned) Using PCLK Clock Input - Figure 3.9					
$t_{DIB\_GDDRX1\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.3	—	ns
$t_{DIA\_GDDRX1\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.3	ns
$f_{DATA\_GDDRX1\_aligned}$	GDDRX1 Data Rate	All Devices	—	500	Mb/s
$f_{MAX\_GDDRX1\_aligned}$	GDDRX1 CLK Frequency (SCLK)	All Devices	—	250	MHz
Generic DDRX2 Outputs With Clock and Data Centered at Pin (GDDRX2_TX.ECLK.Centered) Using PCLK Clock Input, Left and Right sides Only - Figure 3.8					
$t_{DVB\_GDDRX2\_centered}$	Data Output Valid Before CLK Output	All Devices	–0.676	—	ns + 1/2 UI
$t_{DVA\_GDDRX2\_centered}$	Data Output Valid After CLK Output	All Devices	—	0.676	ns + 1/2 UI
$f_{DATA\_GDDRX2\_centered}$	GDDRX2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX\_GDDRX2\_centered}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Generic DDRX2 Outputs With Clock and Data Aligned at Pin (GDDRX2_TX.ECLK.Aligned) Using PCLK Clock Input, Left and Right sides Only - Figure 3.9					
$t_{DIB\_GDDRX2\_aligned}$	Data Output Invalid before CLK Output	All Devices	–0.2	—	ns
$t_{DIA\_GDDRX2\_aligned}$	Data Output Invalid after CLK Output	All Devices	—	0.2	ns
$f_{DATA\_GDDRX2\_aligned}$	GDDRX2 Data Rate	All Devices	—	624	Mb/s
$f_{MAX\_GDDRX2\_aligned}$	GDDRX2 CLK Frequency (ECLK)	All Devices	—	312	MHz
Video DDRX71 Outputs With Clock and Data Aligned at Pin (GDDRX71_TX.ECLK) Using PLL Clock Input, Left and Right sides Only - Figure 3.12					
$t_{DIB\_LVDS71\_i}$	Data Output Invalid before CLK Output	All Devices	–0.2	—	ns + (i) UI
$t_{DIA\_LVDS71\_i}$	Data Output Invalid after CLK Output	All Devices	—	0.2	ns + (i) UI
f_{DATA_LVDS71}	DDR71 Data Rate	All Devices	—	525	Mb/s
f_{MAX_LVDS71}	DDR71 CLK Frequency (ECLK)	All Devices	—	262.5	MHz
Memory Interface					
DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 READ (DQ Input Data are Aligned to DQS)					
t_{DVBDQ_DDR2} t_{DVBDQ_DDR3} t_{DVBDQ_DDR3L} t_{DVBDQ_LPDDR2} t_{DVBDQ_LPDDR3}	Data Output Valid before DQS Input	All Devices	—	–0.374	ns + 1/2 UI
t_{DVADQ_DDR2} t_{DVADQ_DDR3} t_{DVADQ_DDR3L} t_{DVADQ_LPDDR2} t_{DVADQ_LPDDR3}	Data Output Valid after DQS Input	All Devices	0.374	—	ns + 1/2 UI

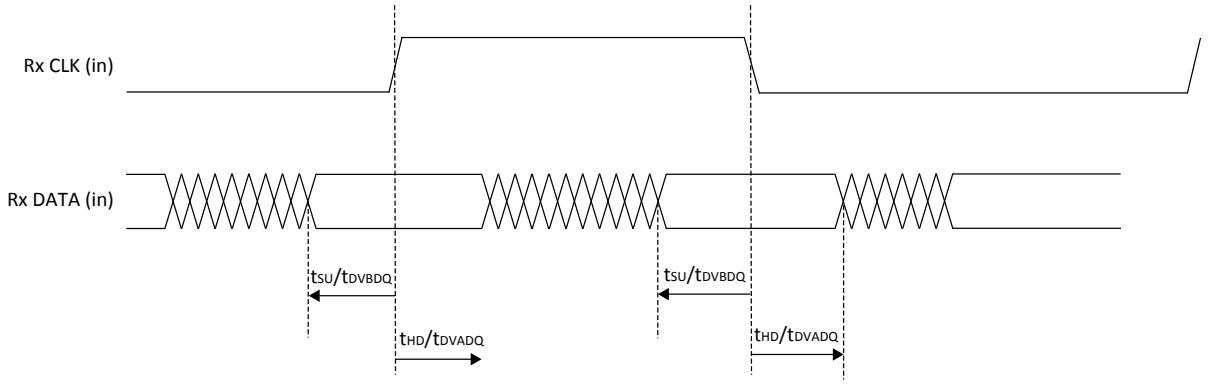


Figure 3.6. Receiver RX.CLK. Centered Waveforms

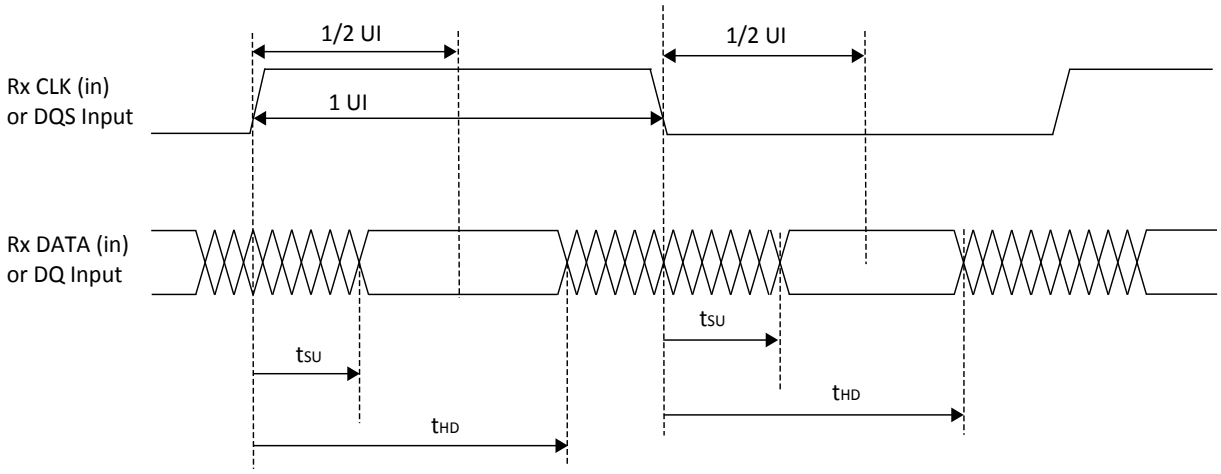


Figure 3.7. Receiver RX.CLK. Aligned and DDR Memory Input Waveforms

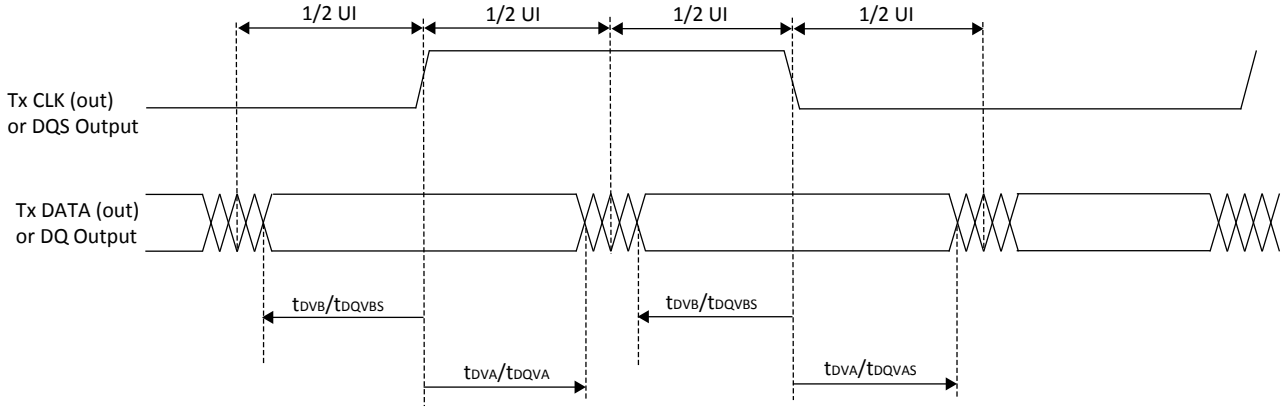


Figure 3.8. Transmit TX.CLK. Centered and DDR Memory Output Waveforms

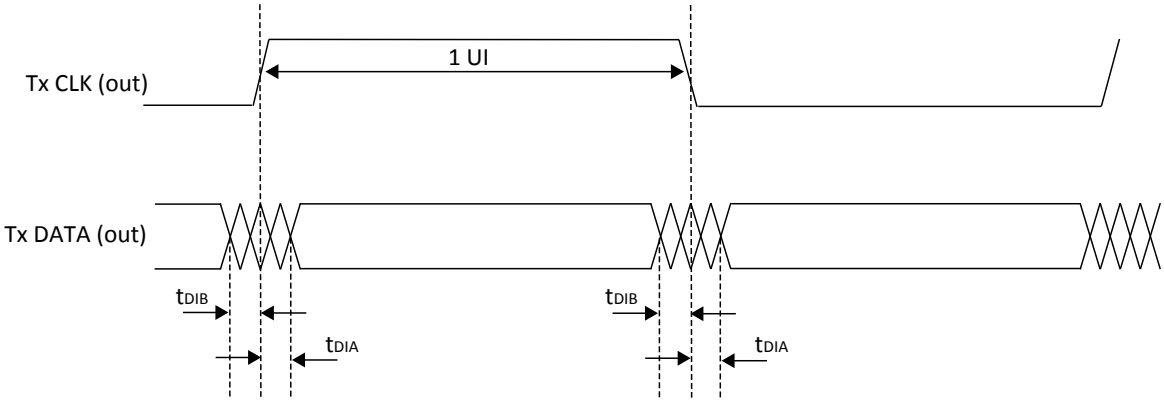
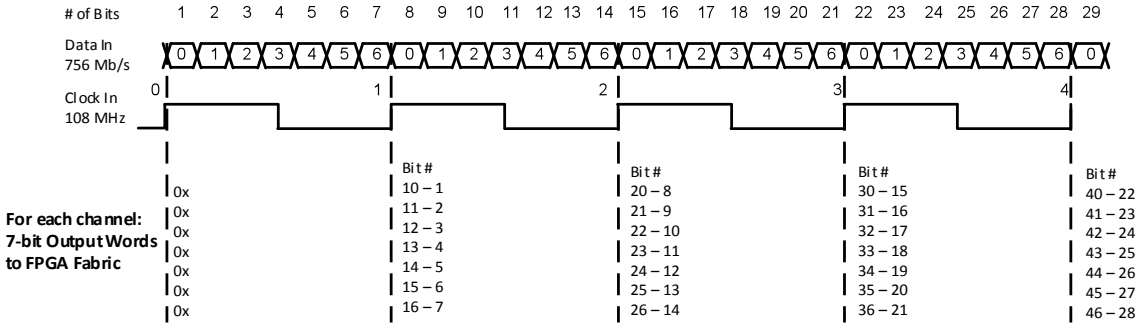


Figure 3.9. Transmit TX.CLK. Aligned Waveforms

Receiver – Shown for one LVDS channel



Transmitter – Shown for one LVDS channel

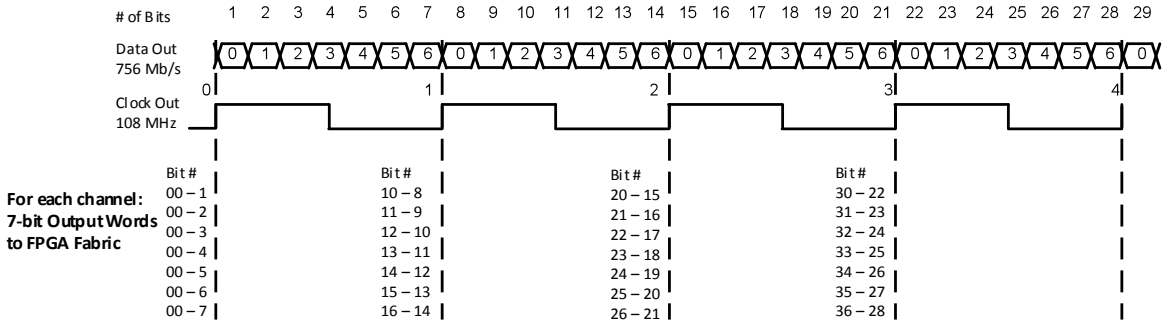


Figure 3.10. DDRX71 Video Timing Waveforms

3.21. SERDES/PCS Block Latency

Table 3.24 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3.13 shows the location of each block.

Table 3.24. SERDES/PCS Latency Breakdown

Item	Description	Min	Avg	Max	Fixed	Bypass	Unit[3]
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with same clocks	3	—	4	—	1	byte clk
	FPGA Bridge - Gearing enabled	5	—	7	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	byte clk
T3	SERDES Bridge transmit	—	—	—	2	1	byte clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	byte clk
R4	Word alignment	3.1	—	4	—	1	byte clk
R5	8b10b decoder	—	—	—	1	0	byte clk
R6	Clock Tolerance Compensation	7	15	23	—	1	byte clk
R7	FPGA Bridge - Gearing disabled with same clocks	4	—	5	—	1	byte clk
	FPGA Bridge - Gearing enabled	7	—	9	—	—	word clk

Notes:

1. Δ1 = –245 ps, Δ2 = +88 ps, Δ3 = +112 ps.
2. Δ1 = +118 ps, Δ2 = +132 ps, Δ3 = +700 ps.
3. byte clk = 8UIs (8-bit mode), or 10 UIs (10-bit mode); word clk = 16UIs (8-bit mode), or 20 UIs (10-bit mode).

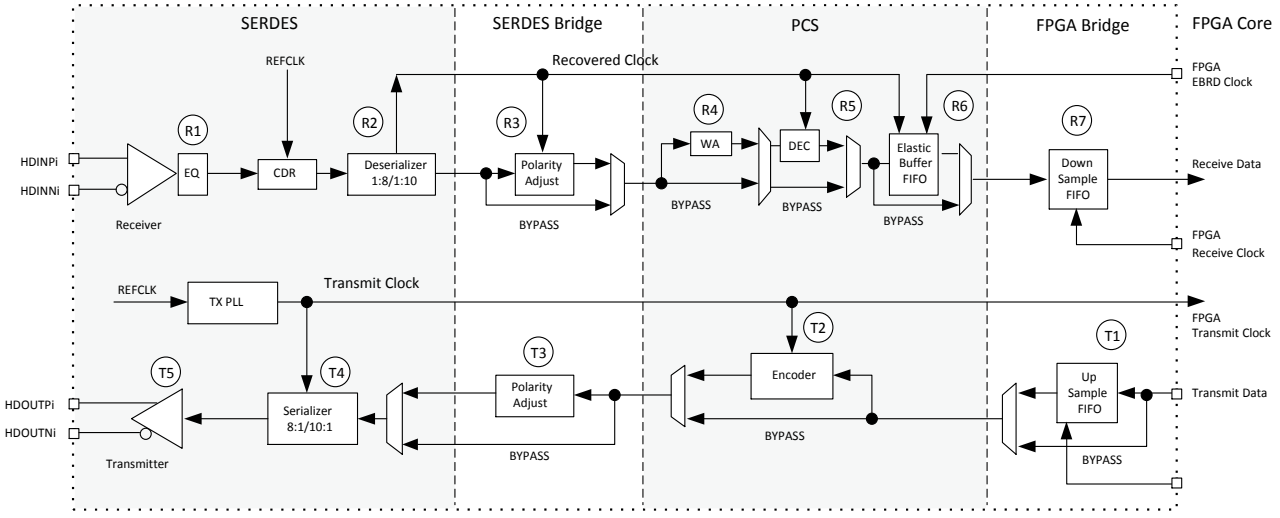


Figure 3.13. Transmitter and Receiver Latency Block Diagram

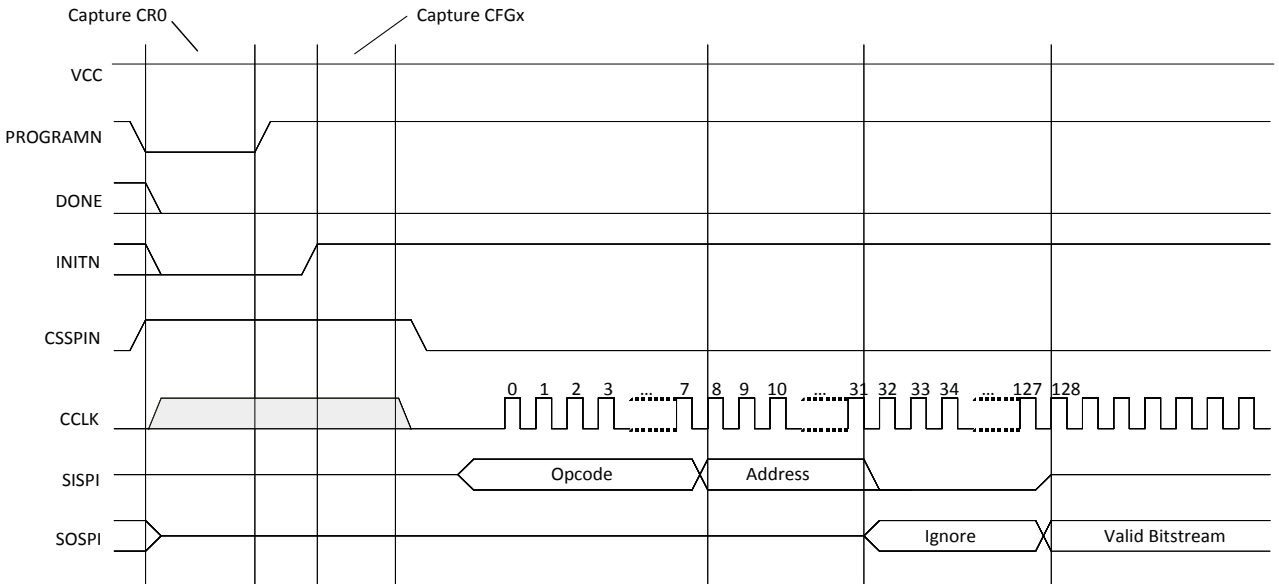


Figure 3.22. Master SPI Configuration Waveforms

3.32. JTAG Port Timing Specifications

Over recommended operating conditions.

Table 3.40. JTAG Port Timing Specifications

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK Clock Frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	10	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	8	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	25	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Table 3.41. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = V_{CCIO}/2	—
				LVCMOS 1.8 = V_{CCIO}/2	—
				LVCMOS 1.5 = V_{CCIO}/2	—
				LVCMOS 1.2 = V_{CCIO}/2	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	V_{CCIO}/2	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	V_{CCIO}/2	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V_{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.