Welcome to E-XFL.COM

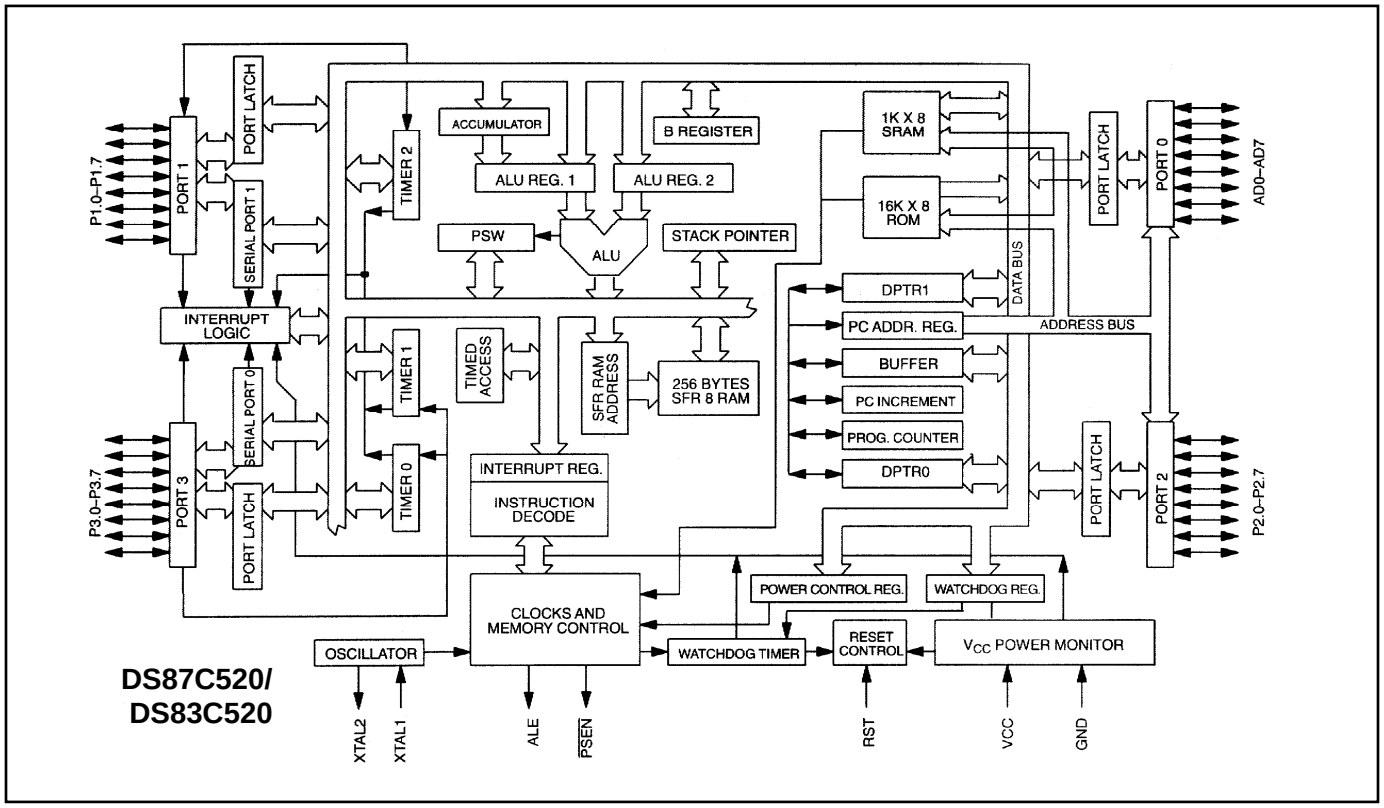
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	External
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds83c520-c01

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**Positive Supply Voltage.** +5V
20	1, 22, 23	16, 17, 39	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is not required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output.** This active-low signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse and is driven high when external ROM is not being accessed.

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
21	24	18	P2.0 (A8)	**Port 2 (A8–15), I/O**. Port 2 is a bidirectional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
22	25	19	P2.1 (A9)	
23	26	20	P2.2 (A10)	
24	27	21	P2.3 (A11)	
25	28	22	P2.4 (A12)	
26	29	23	P2.5 (A13)	
27	30	24	P2.6 (A14)	
28	31	25	P2.7 (A15)	
10	11	5	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below. **Port — Alternate — Mode** P3.0 — RXD0 — Serial Port 0 Input P3.1 — TXD0 — Serial Port 0 Output P3.2 — $\overline{INT0}$ — External Interrupt 0 P3.3 — $\overline{INT1}$ — External Interrupt 1 P3.4 — T0 — Timer 0 External Input P3.5 — T1 — Timer 1 External Input P3.6 — $\overline{WR}$ — External Data Memory Write Strobe P3.7 — $\overline{RD}$ — External Data Memory Read Strobe
11	13	7	P3.1	
12	14	8	P3.2	
13	15	9	P3.3	
14	16	10	P3.4	
15	17	11	P3.5	
16	18	12	P3.6	
17	19	13	P3.7	
31	35	29	$\overline{EA}$	**External Access Input, Active Low.** Connect to ground to force the DS87C520/DS83C520 to use an external ROM. The internal RAM is still accessible as determined by register settings. Connect $\overline{EA}$ to V_{CC} to use internal ROM.
—	12, 34	6, 28	N.C.	**Not Connected.** These pins should not be connected. They are reserved for use with future devices in this family.

COMPATIBILITY

The DS87C520/DS83C520 are fully static CMOS 8051-compatible microcontrollers designed for high performance. In most cases, the DS87C520/DS83C520 can drop into an existing socket for the 8xc51 family to improve the operation significantly. While remaining familiar to 8051 family users, the devices have many new features. In general, software written for existing 8051-based systems works without modification on the DS87C520/DS83C520. The exception is critical timing since the high-speed microcontrollers performs instructions much faster than the original for any given crystal selection. The DS87C520/DS83C520 run the standard 8051 family instruction set and are pin compatible with DIP, PLCC, or TQFP packages.

The DS87C520/DS83C520 provide three 16-bit timer/counters, full-duplex serial port (2), 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12-clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new four clocks per cycle if desired. The PCA is not supported.

The DS87C520/DS83C520 provide several new hardware features implemented by new special function registers. A summary of these SFRs is provided below.

PERFORMANCE OVERVIEW

The DS87C520/DS83C520 feature a high-speed 8051-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C520/DS83C520, the same machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C520/DS83C520 will see the full 3-to-1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements produce a peak instruction cycle in 121ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the *High-Speed Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C520/DS83C520, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C520/DS83C520 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C520/DS83C520. This allows the DS87C520/DS83C520 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C520/DS83C520 duplicate the SFRs contained in the standard 80C52. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 1. Special Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	C0h
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	C/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

Note: *New functions are in bold.*

MEMORY RESOURCES

Like the 8051, the DS87C520/DS83C520 use three memory areas. The total memory configuration of the DS87C520/DS83C520 is 16kB of ROM, 1kB of data SRAM and 256 bytes of scratchpad or direct RAM. The 1kB of data space SRAM is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1kB as they use different addressing modes and separate instructions.

OPERATIONAL CONSIDERATION

The erasure window of the windowed CERDIP should be covered without regard to the programmed/unprogrammed state of the EPROM. Otherwise, the device may not meet the AC and DC parameters listed in the data sheet.

PROGRAM MEMORY ACCESS

On-chip ROM begins at address 0000h and is contiguous through 3FFFh (16kB). Exceeding the maximum address of on-chip ROM will cause the device to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS87C520/DS83C520 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory, such as Flash, is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory, and then restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 and 2. A depiction of the ROM memory map is shown in Figure 2.

The ROMSIZE register is used to select the maximum on-chip decoded address for ROM. Bits RMS2, RMS1, RMS0 have the following effect.

RMS2	RMS1	RMS0	MAXIMUM ON-CHIP ROM ADDRESS
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB (default)/3FFFh
1	1	0	Invalid—reserved
1	1	1	Invalid—reserved

The reset default condition is a maximum on-chip ROM address of 16kB. Thus no action is required if this feature is not used. When accessing external program memory, the first 16kB would be inaccessible. To select a smaller effective ROM size, software must alter bits RMS2–RMS0. Altering these bits requires a Timed-Access procedure as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that the DS87C520/DS83C520 are executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C520/DS83C520 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using 2 bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

Table 2. Data Memory Access Control

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h–FFFFh	External data memory (*default condition)*
0	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFFh	External data memory
1	0	Reserved	Reserved
1	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFBh	Reserved—no external access
		FFFCh	Read access to the status of lock bits
		FFFDh–FFFFh	Reserved—no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2–0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

Note: After internal MOVX SRAM has been initialized, changing the DME0/1 bits has no effect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C520/DS83C520 allow software to adjust the speed of off-chip data memory access. The microcontrollers can perform the MOVX in as few as two instruction cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch

setting. When desiring maximum speed, software should select a Stretch value of 0. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. Also, setup and hold times are increased by 1 clock when using any Stretch greater than 0. This results in a wider read/write strobe and relaxed interface timing, allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is in the *Electrical Specifications* section. Table 3 shows the resulting strobe widths for each Stretch value. The memory Stretch uses the Clock Control Special Function Register at SFR location 8Eh. The Stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first Stretch (default) allows the use of common 120ns RAMs without dramatically lengthening the memory access.

Table 3. Data Memory Cycle Stretch Values

CKCON.2-0			MEMORY CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME at 33MHz (ns)
M2	M1	M0			
0	0	0	2 (forced internal)	2	60
0	0	1	3 (default external)	4	121
0	1	0	4	8	242
0	1	1	5	12	364
1	0	0	6	16	485
1	0	1	7	20	606
1	1	0	8	24	727
1	1	1	9	28	848

DUAL DATA POINTER

The timing of block moves of data memory is faster using the Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS87C520/DS83C520, this data pointer is called DPTR0, located at SFR addresses 82h and 83h. These are the original locations. Using DPTR requires no modification of standard code. The new DPTR at SFR 84h and 85h is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer. Its location is the lsb of the SFR location 86h. No other bits in register 86h have any effect and are 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore it takes only one instruction to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. The software simply switches between DPTR0 and 1 once software loads them. The relevant register locations are as follows:

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

Crystal/Ring Operation

The DS87C520/DS83C520 allow software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one-instruction cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to 0. At this time, the crystal oscillation will begin. The DS87C520/DS83C520 then provide a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to 1 before XTUP=1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

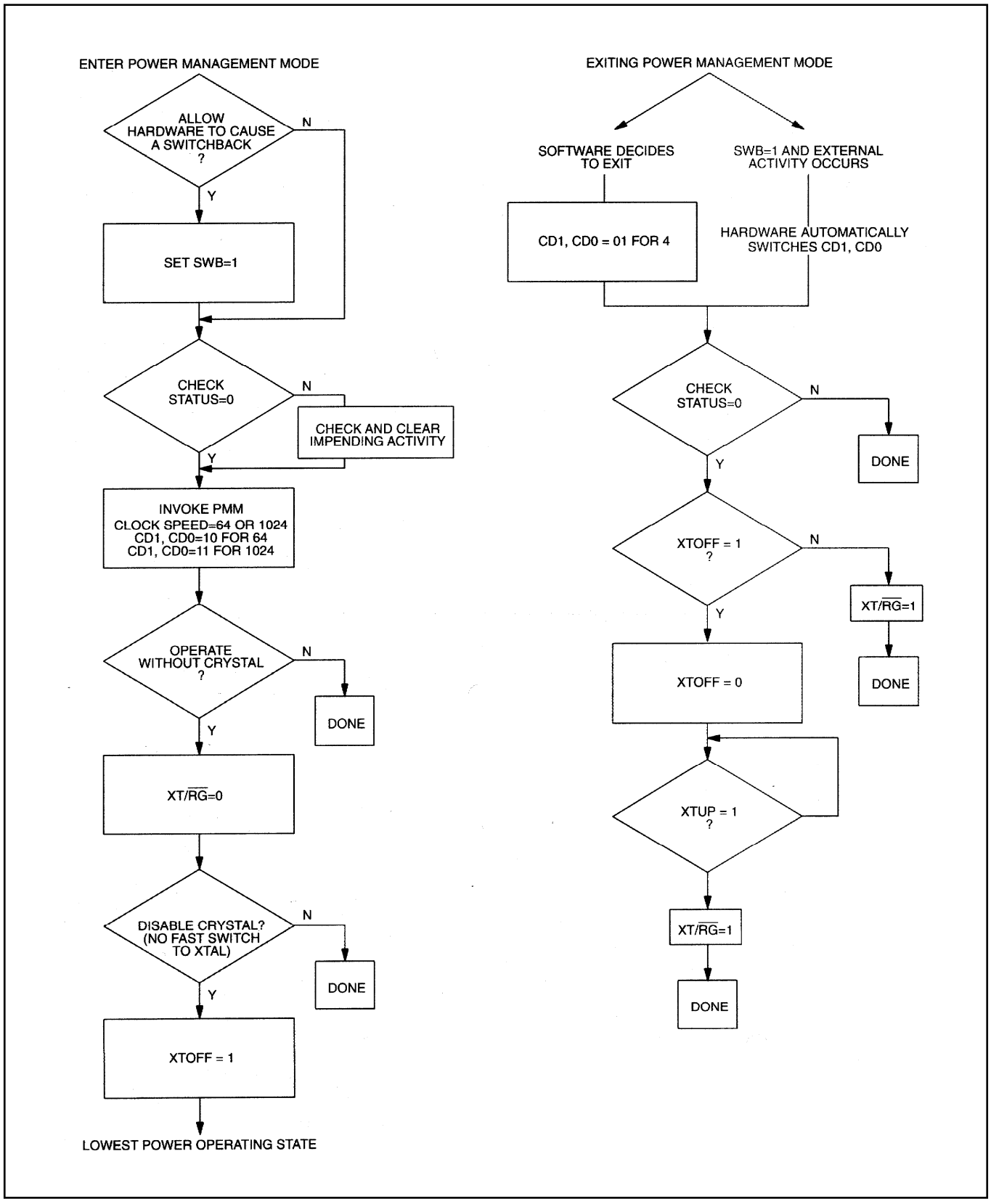
Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystal-less PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

Figure 3 illustrates a typical decision set associated with PMM. Table 6 is a summary of the bits relating to PMM and its operation.

Table 6. PMM Control and Status Bit Summary

BIT	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{RG}$	EXIF.3	Control. XT/$\overline{RG}$ = 1, runs from crystal or external clock; XT/$\overline{RG}$ = 0, runs from internal ring oscillator.	X	0 to 1 only when XTUP = 1 and XTOFF = 0
RGMD	EXIF.2	Status. RGMD = 1, CPU clock = ring; RGMD = 0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1, 0 = 01, 4 clocks; CS1, 0 = 10, PMM1; CD1, 0 = 11, PMM2.	0, 1	Write CD1, 0 = 10 or 11 only from CD1, 0 = 01
SWB	PMR.5	Control. SWB = 1, hardware invokes switchback to 4 clocks, SWB = 0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{RG}$ = 0
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

Figure 3. Invoking and Clearing PMM



POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning Power-Fail Interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to a logic 1 will enable the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

To prevent software from losing control, the DS87C520/DS83C520 include a programmable Watchdog Timer. The Watchdog is a free-running timer that sets a flag if allowed to reach a preselected timeout. It can be (re)started by software.

A typical application is to select the flag as a reset source. When the Watchdog times out, it sets its flag, which generates reset. Software must restart the timer before it reaches its timeout or the processor is reset.

Software can select one of four timeout values. Then, it restarts the timer and enables the reset function. After enabling the reset function, software must then restart the timer before its expiration or hardware will reset the CPU. Both the Watchdog Reset Enable and the Watchdog Restart control bits are protected by a "Timed Access" circuit. This prevents errant software from accidentally clearing the Watchdog. Timeout values are precise since they are a function of the crystal frequency as shown in Table 7. For reference, the time periods at 33MHz also are shown.

The Watchdog also provides a useful option for systems that do not require a reset circuit. It will set an interrupt flag 512 clocks before setting the reset flag. Software can optionally enable this interrupt source. The interrupt is independent of the reset. A common use of the interrupt is during debug, to show developers where the Watchdog times out. This indicates where the Watchdog must be restarted by software. The interrupt also can serve as a convenient time-base generator or can wake-up the processor from power saving modes.

The Watchdog function is controlled by the Clock Control (CKCON-8Eh), Watchdog Control (WDCON-D8h), and Extended Interrupt Enable (EIE-E8h) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively and they select the Watchdog timeout period as shown in Table 7.

Table 7. Watchdog Timeout Values

WD1	WD2	INTERRUPT TIMEOUT	TIME (33 MHz)	RESET TIMEOUT	TIME (33 MHz)
0	0	2^{17} clocks	3.9718 ms	2^{17} + 512 clocks	3.9874 ms
0	1	2^{20} clocks	31.77 ms	2^{20} + 512 clocks	31.79 ms
1	0	2^{23} clocks	254.20 ms	2^{23} + 512 clocks	254.21 ms
1	1	2^{26} clocks	2033.60 ms	2^{26} + 512 clocks	2033.62 ms

As shown in Table 7, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; and 2^{26} = 67,108,864 clocks. The times shown in Table 7 are with a 33MHz crystal frequency. Once the counter chain has completed a full interrupt count, hardware

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 9. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

OTHER EPROM OPTIONS

The DS87C520 has user selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

Program the EPROM selectable options as shown in Table 9. The Option Register sets or reads these selections. The bits in the Option Control Register have the following function:

Bits 7 to 4	Reserved, program to a 1.
Bit 3	Watchdog POR default. Set = 1; watchdog reset function is disabled on power-up. Set = 0; watchdog reset function is enabled automatically.
Bits 2 to 0	Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	20h	Model
60h	01h	Extension

DS83C520 ROM VERIFICATION

The DS83C520 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 5, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C520 SIGNATURE

The Signature bytes identify the DS83C520 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	21h	Model
60h	01h	Extension

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	2
Power-Fail Warning	DS87C520	V_{PFW}	4.25	4.38	4.5	V	2
	DS83C520		4.25	4.38	4.55		
Minimum Operating Voltage	DS87C520	V_{RST}	4.0	4.13	4.25	V	2
	DS83C520		4.0	4.13	4.275		
Supply Current Active Mode at 33MHz		I_{CC}		30	45	mA	3
Supply Current Idle Mode at 33MHz		I_{IDLE}		15	25	mA	4
Supply Current Stop Mode, Bandgap Disabled (0°C to +70°C)		I_{STOP}		1	100	µA	5
Supply Current Stop Mode, Bandgap Disabled (-40°C to +85°C)				1	150	µA	5
Supply Current Stop Mode, Bandgap Enabled (0°C to +70°C)		I_{SPBG}		50	170	µA	5
Supply Current Stop Mode, Bandgap Enabled (-40°C to +85°C)				50	195	µA	5
Input Low Level		V_{IL}	-0.3		+0.8	V	2
Input High Level (except XTAL1 and RST)		V_{IH}	2.0		V_{CC} + 0.3	V	2
Input High Level XTAL1 and RST		V_{IH2}	3.5		V_{CC} + 0.3	V	2
Output Low Voltage, Ports 1 and 3 at I_{OL} = 1.6mA		V_{OL1}		0.15	0.45	V	2
Output Low Voltage Ports 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA		V_{OL2}		0.15	0.45	V	2
Output High Voltage Ports 1, 2, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA		V_{OH1}	2.4			V	2, 7
Output High Voltage Ports 1, 2, 3 at I_{OH} = -1.5mA		V_{OH2}	2.4			V	2, 8
Output High Voltage Port 0, 2, ALE, $\overline{PSEN}$ in Bus Mode at I_{OH} = -8mA		V_{OH3}	2.4			V	2, 6
Input Low Current Ports 1, 2, 3 at 0.45V		I_{IL}			-70	µA	12

MOVX CHARACTERISTICS (continued)

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

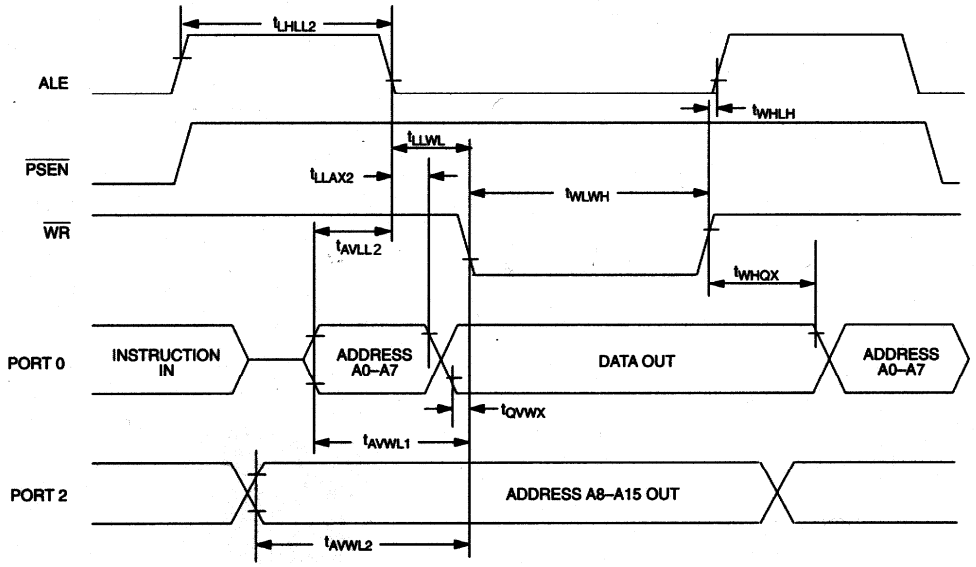
EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCL}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

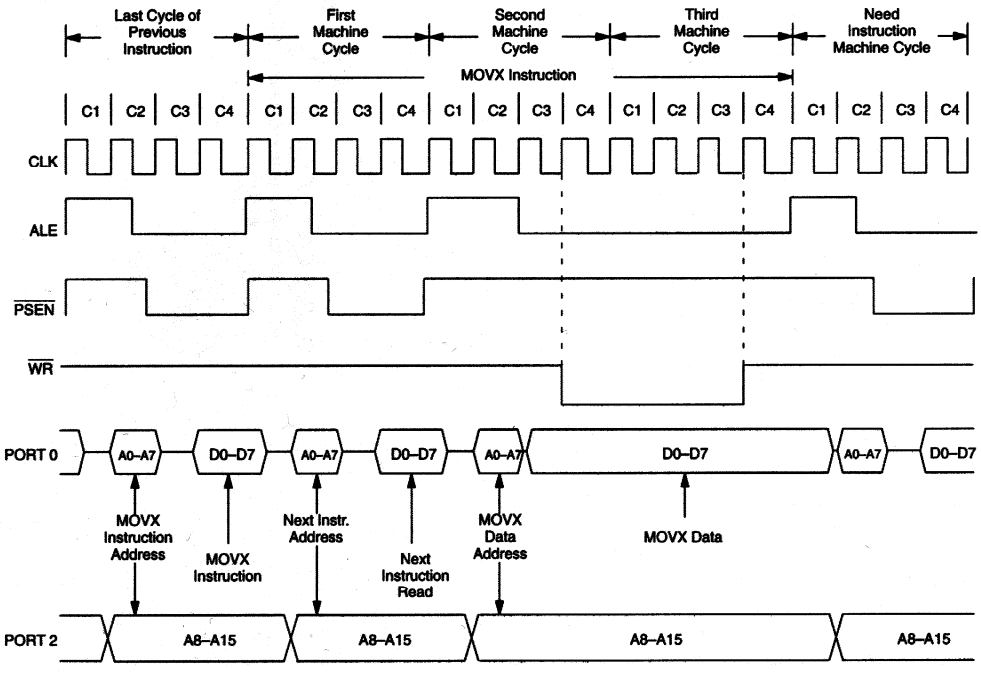
SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0, 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0, 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0, 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0, 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0, 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		

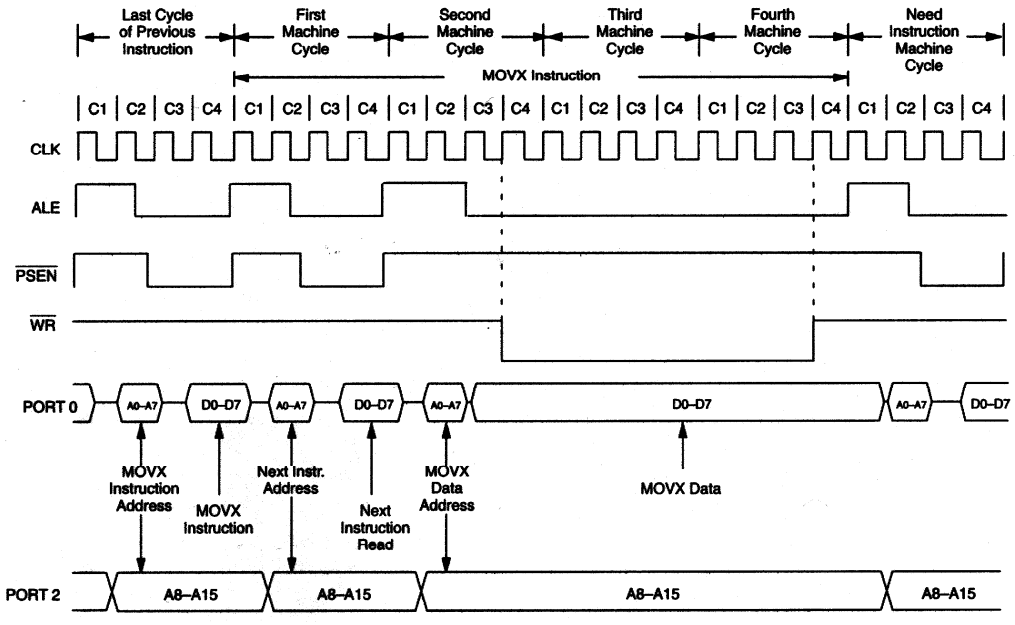
EXTERNAL DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

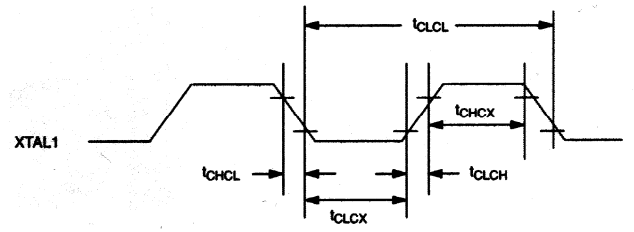


DATA MEMORY WRITE WITH STRETCH = 2

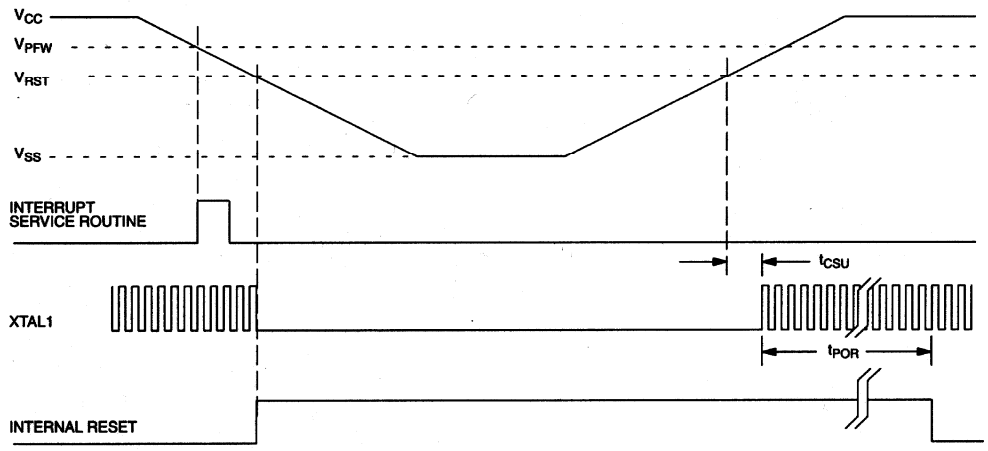


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

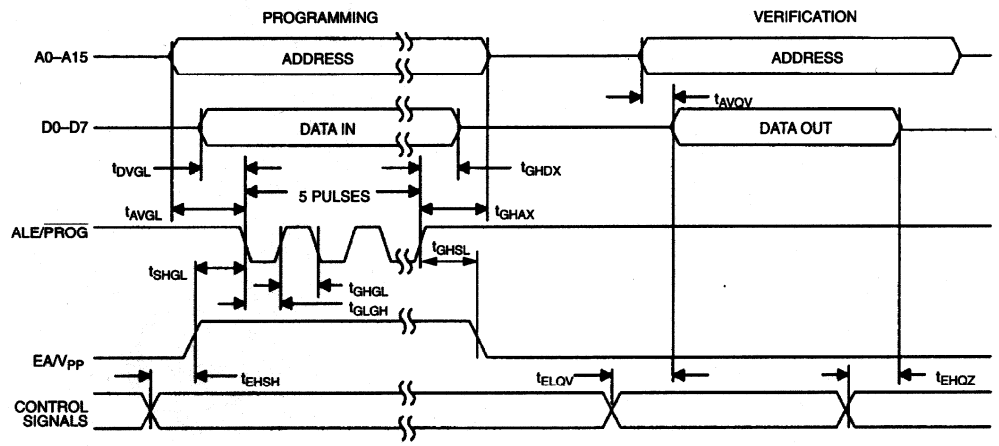
EXTERNAL CLOCK DRIVE



POWER-CYCLE TIMING



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



PACKAGE INFORMATION

For the latest package outline information, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+3	**21-0293**
40 CDIP	J40-5	**21-0384**
40 PDIP	P40+4	**21-0044**
44 PLCC	Q44+9	**21-0049**