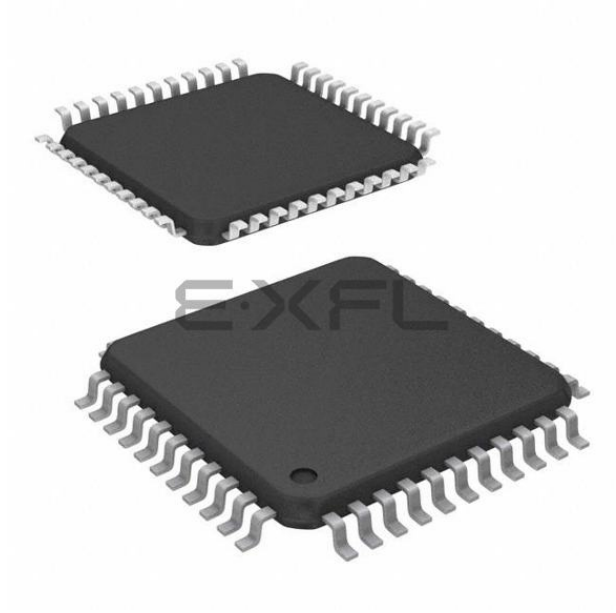
Analog Devices Inc./Maxim Integrated - DS87C520-ENL+ Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c520-enl

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>30</td><td>33</td><td>27</td><td>ALE</td><td>Address Latch Enable Output. The ALE functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the DS87C520/DS83C520 are in a reset condition. ALE can also be disabled and forced high by writing ALEOFF = 1 (PMR.2). ALE operates independently of ALEOFF during external memory accesses.</td></tr>
<tr><td>39</td><td>43</td><td>37</td><td>P0.0 (AD0)</td><td rowspan="8">Port 0 (AD0–7), I/O. Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pullup resistors are required when using Port 0 as an I/O port.</td></tr>
<tr><td>38</td><td>42</td><td>36</td><td>P0.1 (AD1)</td></tr>
<tr><td>37</td><td>41</td><td>35</td><td>P0.2 (AD2)</td></tr>
<tr><td>36</td><td>40</td><td>34</td><td>P0.3 (AD3)</td></tr>
<tr><td>35</td><td>39</td><td>33</td><td>P0.4 (AD4)</td></tr>
<tr><td>34</td><td>38</td><td>32</td><td>P0.5 (AD5)</td></tr>
<tr><td>33</td><td>37</td><td>31</td><td>P0.6 (AD6)</td></tr>
<tr><td>32</td><td>36</td><td>30</td><td>P0.7 (AD7)</td></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td rowspan="8">Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state; a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are out-lines as follows.

Port Alternate Function
P1.0 T2 External I/O for Timer/Counter 2
P1.1 T2EX EX Timer/Counter 2 Capture/Reload Trigger
P1.2 RXD1 Serial Port 1 Input
P1.3 TXD1 Serial Port 1 Output
P1.4 INT2 External Interrupt 2 (Positive Edge Detect)
P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Negative Edge Detect)
P1.6 INT4 External Interrupt 4 (Positive Edge Detect)
P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Negative Edge Detect)</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td></tr>
</table>

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C520/DS83C520, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C520/DS83C520 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C520/DS83C520. This allows the DS87C520/DS83C520 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C520/DS83C520 duplicate the SFRs contained in the standard 80C52. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 1. Special Function Register Locations

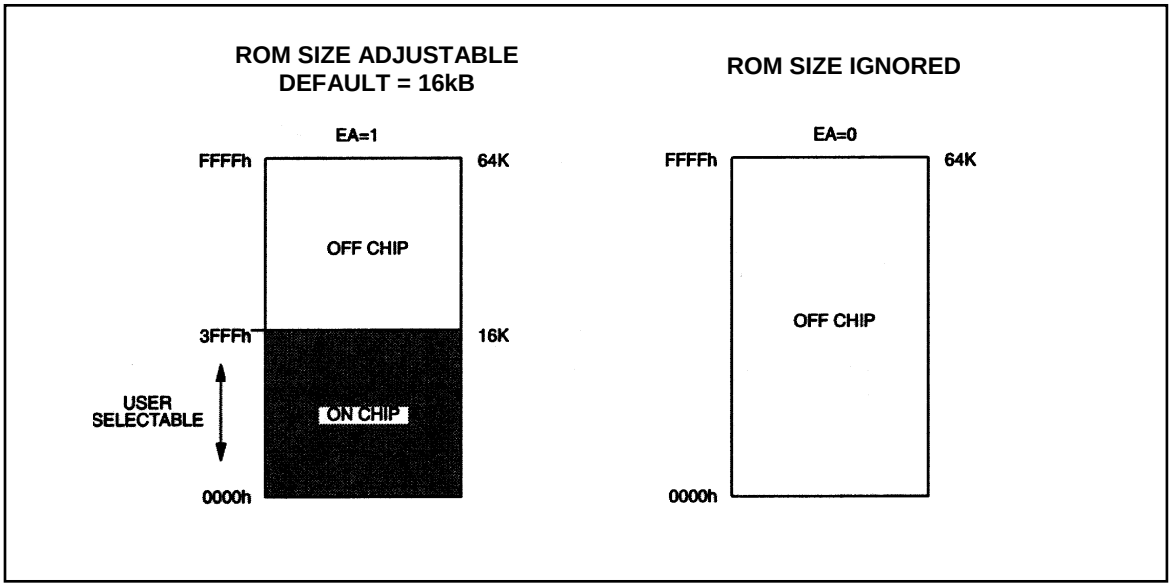
REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	C0h
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	C/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

Note: *New functions are in bold.*

16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device will immediately jump to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4kB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

Figure 2. ROM Memory Map



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C520/DS83C520 contain on-chip data memory. They also contain the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

POWER MANAGEMENT

Along with the standard Idle and power down (Stop) modes of the standard 80C52, the DS87C520/DS83C520 provide a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C520/DS83C520 also feature several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C520/DS83C520 use four clocks per machine cycle. Thus the instruction cycle rate is Clock/4. At 33MHz crystal speed, the instruction cycle speed is 8.25MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources - discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 4 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slow and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 5.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle mode, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from Idle, and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)
11.0592	2.765	172.8	10.8
16	4.00	250.0	15.6
25	6.25	390.6	24.4
33	8.25	515.6	32.2

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)
11.0592	13.1	5.3	4.8
16	17.2	6.4	5.6
25	25.7	8.1	7.0
33	32.8	9.8	8.2

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C520/DS83C520 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal and ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h).

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Switchback

To return to a 4-clock rate from PMM, software can simply select the CD1 and CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C520/DS83C520 provide several hardware alternatives for automatic Switchback. If Switchback is enabled, then the device will automatically return to a 4-clock per cycle speed when an interrupt occurs from an enabled, valid external interrupt source. A Switchback will also occur when a UART detects the beginning of a serial start bit if the serial receiver is enabled (REN = 1). Note the beginning of a start bit does not generate an interrupt; this occurs on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception. A switchback will also occur when a byte is written to SBUF0 or SBUF1 for transmission.

Switchback is enabled by setting the SWB bit (PMR.5) to a 1 in software. For an external interrupt, Switchback will occur only if the interrupt source could really generate the interrupt. For example, if $\overline{\text{INT0}}$ is enabled but has a low priority setting, then Switchback will not occur on $\overline{\text{INT0}}$ if the CPU is servicing a high priority interrupt.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C520/DS83C520 support three levels of interrupt priority. These levels are Power-fail, High, and Low. Bits STATUS.7-5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS. 7) is a 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

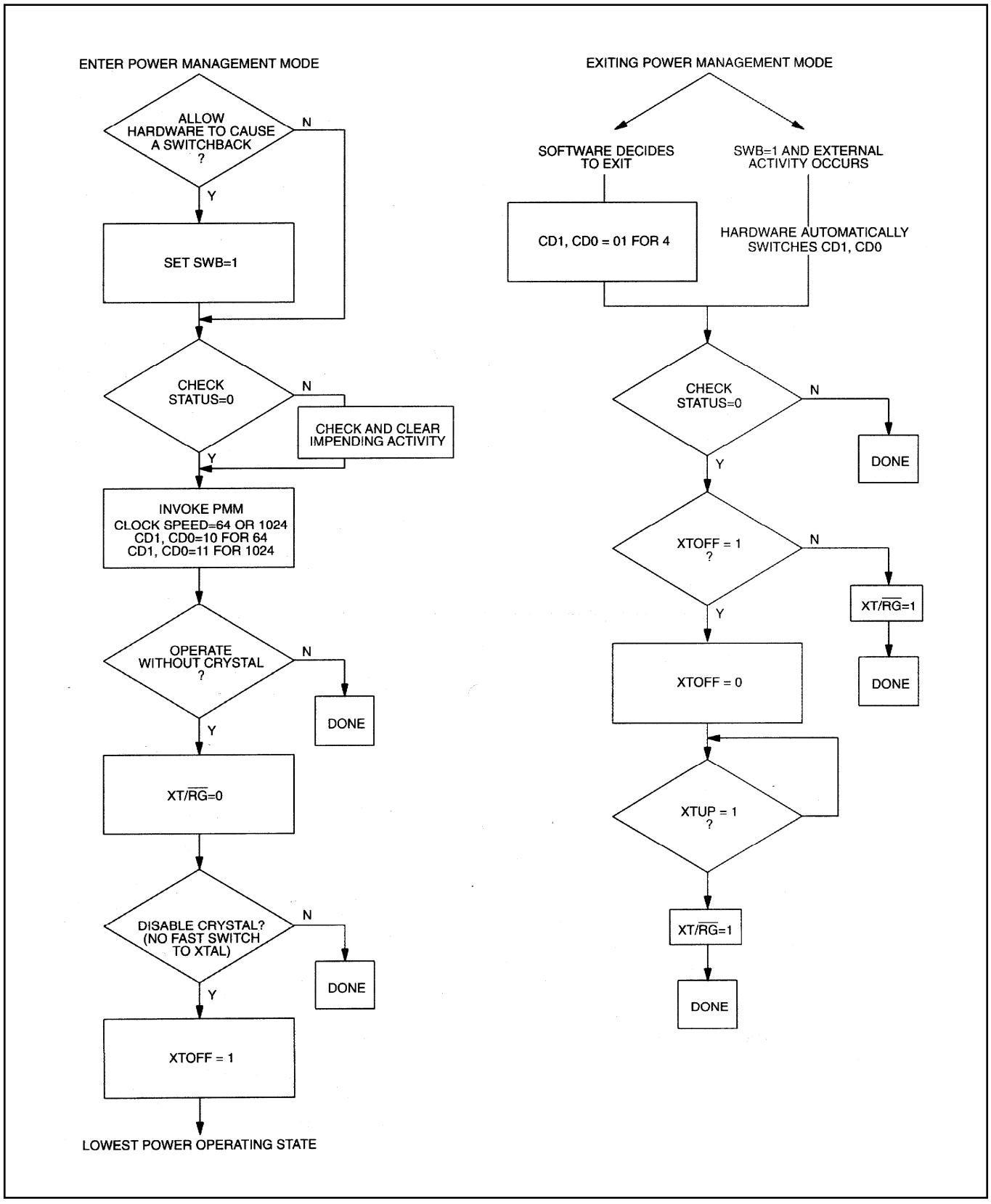
Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port 0 Receive Activity (SPRA0;STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port 0 Transmit Activity (SPTA0; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 and STATUS.3 provide the same information for Serial Port 1, respectively. These bits should be interrogated before entering PMM1 or PMM2 to ensure that no serial port operations are in progress. Changing the clock divisor rate during a serial transmission or reception will corrupt the operation.

Table 6. PMM Control and Status Bit Summary

BIT	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{RG}$	EXIF.3	Control. XT/$\overline{RG}$ = 1, runs from crystal or external clock; XT/$\overline{RG}$ = 0, runs from internal ring oscillator.	X	0 to 1 only when XTUP = 1 and XTOFF = 0
RGMD	EXIF.2	Status. RGMD = 1, CPU clock = ring; RGMD = 0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1, 0 = 01, 4 clocks; CS1, 0 = 10, PMM1; CD1, 0 = 11, PMM2.	0, 1	Write CD1, 0 = 10 or 11 only from CD1, 0 = 01
SWB	PMR.5	Control. SWB = 1, hardware invokes switchback to 4 clocks, SWB = 0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{RG}$ = 0
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

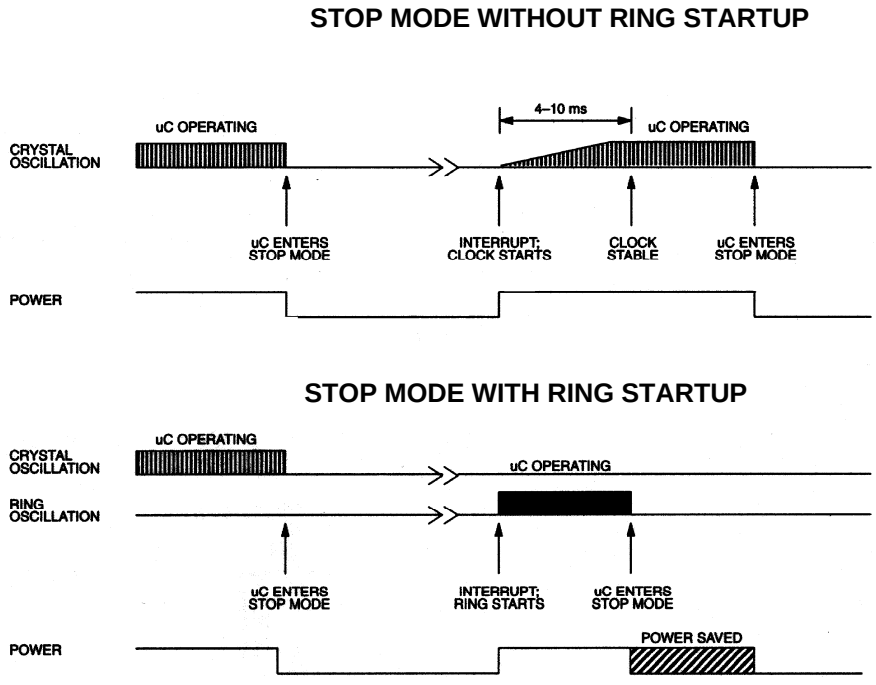
Figure 3. Invoking and Clearing PMM



how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL - Ring Select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD-Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

Figure 4. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The microcontroller allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static mode when performing on-chip memory access. The default state of ALEOFF = 0 so ALE toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C520/DS83C520 provide several of the most commonly needed peripheral functions in micro-computer-based systems. These new functions include a second serial port, power-fail reset, power-fail interrupt, and a programmable watchdog timer. These are described in the following paragraphs. More details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C520/DS83C520 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C520/DS83C520 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C520/DS83C520 architecture normally uses four clocks per machine cycle. However, in the area of timers and serial ports, the DS87C520/DS83C520 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON;8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS87C520/DS83C520 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C520/DS83C520 use 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C520/DS83C520 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning Power-Fail Interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to a logic 1 will enable the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

To prevent software from losing control, the DS87C520/DS83C520 include a programmable Watchdog Timer. The Watchdog is a free-running timer that sets a flag if allowed to reach a preselected timeout. It can be (re)started by software.

A typical application is to select the flag as a reset source. When the Watchdog times out, it sets its flag, which generates reset. Software must restart the timer before it reaches its timeout or the processor is reset.

Software can select one of four timeout values. Then, it restarts the timer and enables the reset function. After enabling the reset function, software must then restart the timer before its expiration or hardware will reset the CPU. Both the Watchdog Reset Enable and the Watchdog Restart control bits are protected by a "Timed Access" circuit. This prevents errant software from accidentally clearing the Watchdog. Timeout values are precise since they are a function of the crystal frequency as shown in Table 7. For reference, the time periods at 33MHz also are shown.

The Watchdog also provides a useful option for systems that do not require a reset circuit. It will set an interrupt flag 512 clocks before setting the reset flag. Software can optionally enable this interrupt source. The interrupt is independent of the reset. A common use of the interrupt is during debug, to show developers where the Watchdog times out. This indicates where the Watchdog must be restarted by software. The interrupt also can serve as a convenient time-base generator or can wake-up the processor from power saving modes.

The Watchdog function is controlled by the Clock Control (CKCON-8Eh), Watchdog Control (WDCON-D8h), and Extended Interrupt Enable (EIE-E8h) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively and they select the Watchdog timeout period as shown in Table 7.

Table 7. Watchdog Timeout Values

WD1	WD2	INTERRUPT TIMEOUT	TIME (33 MHz)	RESET TIMEOUT	TIME (33 MHz)
0	0	2^{17} clocks	3.9718 ms	2^{17} + 512 clocks	3.9874 ms
0	1	2^{20} clocks	31.77 ms	2^{20} + 512 clocks	31.79 ms
1	0	2^{23} clocks	254.20 ms	2^{23} + 512 clocks	254.21 ms
1	1	2^{26} clocks	2033.60 ms	2^{26} + 512 clocks	2033.62 ms

As shown in Table 7, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; and 2^{26} = 67,108,864 clocks. The times shown in Table 7 are with a 33MHz crystal frequency. Once the counter chain has completed a full interrupt count, hardware

Table 9. EPROM Programming Modes

MODE		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	PL	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0-3Fh		H	L	PL	12.75V	L	H	H	L	H
Program Lock Bits	LB1	H	L	PL	12.75V	H	H	H	H	H
	LB2	H	L	PL	12.75V	H	H	H	L	L
	LB3	H	L	PL	12.75V	H	L	H	H	L
Program Option Register Address FCh		H	L	PL	12.75V	L	H	H	L	L
Read Signature or Option Registers 30, 31, 60 FCh		H	L	H	H	L	L	L	L	L

Table 10. DS87C520 EPROM Lock Bits

LEVEL	LOCK BITS			PROTECTION
	LB1	LB2	LB3	
1	U	U	U	No program lock. Encrypted verify if encryption table was programmed.
2	P	U	U	Prevent MOVC instructions in external memory from reading program bytes in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further programming of EPROM.
3	P	P	U	Level 2 plus no verify operation. Also, prevent MOVX instructions in external memory from reading SRAM (MOVX) in internal memory.
4	P	P	P	Level 3 plus no external execution.

SECURITY OPTIONS

The DS87C520 employs a standard three-level lock that restricts viewing of the EPROM contents. A 64-byte Encryption Array allows the authorized user to verify memory by presenting the data in encrypted form.

Lock Bits

The security lock consists of three lock bits. These bits select a total of four levels of security. Higher levels provide increasing security but also limit application flexibility. Table 10 shows the security settings. Note that the programmer cannot directly read the state of the security lock. User software has access to this information as described in the *Memory* section.

DS83C520 ROM VERIFICATION

The DS83C520 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 5, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C520 SIGNATURE

The Signature bytes identify the DS83C520 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	21h	Model
60h	01h	Extension

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature……-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V, T_A = -40°C to +85°C.) (Note 1)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	2
Power-Fail Warning	DS87C520	V_{PFW}	4.25	4.38	4.5	V	2
	DS83C520		4.25	4.38	4.55		
Minimum Operating Voltage	DS87C520	V_{RST}	4.0	4.13	4.25	V	2
	DS83C520		4.0	4.13	4.275		
Supply Current Active Mode at 33MHz		I_{CC}		30	45	mA	3
Supply Current Idle Mode at 33MHz		I_{IDLE}		15	25	mA	4
Supply Current Stop Mode, Bandgap Disabled (0°C to +70°C)		I_{STOP}		1	100	µA	5
Supply Current Stop Mode, Bandgap Disabled (-40°C to +85°C)				1	150	µA	5
Supply Current Stop Mode, Bandgap Enabled (0°C to +70°C)		I_{SPBG}		50	170	µA	5
Supply Current Stop Mode, Bandgap Enabled (-40°C to +85°C)				50	195	µA	5
Input Low Level		V_{IL}	-0.3		+0.8	V	2
Input High Level (except XTAL1 and RST)		V_{IH}	2.0		V_{CC} + 0.3	V	2
Input High Level XTAL1 and RST		V_{IH2}	3.5		V_{CC} + 0.3	V	2
Output Low Voltage, Ports 1 and 3 at I_{OL} = 1.6mA		V_{OL1}		0.15	0.45	V	2
Output Low Voltage Ports 0 and 2, ALE, $\overline{PSEN}$ at I_{OL} = 3.2mA		V_{OL2}		0.15	0.45	V	2
Output High Voltage Ports 1, 2, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA		V_{OH1}	2.4			V	2, 7
Output High Voltage Ports 1, 2, 3 at I_{OH} = -1.5mA		V_{OH2}	2.4			V	2, 8
Output High Voltage Port 0, 2, ALE, $\overline{PSEN}$ in Bus Mode at I_{OH} = -8mA		V_{OH3}	2.4			V	2, 6
Input Low Current Ports 1, 2, 3 at 0.45V		I_{IL}			-70	µA	12

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}$-5		ns	t_{MCS}=0
		$2t_{CLCL}$-5			t_{MCS}>0
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL}$-5		ns	t_{MCS}=0
		t_{CLCL}-5			t_{MCS}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$-10		ns	t_{MCS}=0
		t_{CLCL}-7			t_{MCS}>0
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-22	ns	t_{MCS}=0
			t_{MCS}-24		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	—
Data Float after Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-31	ns	t_{MCS}=0
			$t_{MCS}+t_{CLCL}$-26		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-29	ns	t_{MCS}=0
			$t_{MCS}+2t_{CLCL}$-29		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-37	ns	t_{MCS}=0
			$t_{MCS}+2.5t_{CLCL}$-37		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-10	$0.5t_{CLCL}$+5	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-9		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-17		ns	t_{MCS}=0
		$2.5t_{CLCL}$-16			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-6		ns	—
Data Hold after Write	t_{WHQX}	t_{CLCL}-5		ns	t_{MCS}=0
		$2t_{CLCL}$-6			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 2)	ns	—
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-4	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0

Note 1: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, the DS87C520 and DS83C520 specify the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time	I	Instruction	W	$\overline{WR}$ signal
A	Address	P	$\overline{PSEN}$	X	No longer a valid logic level
C	Clock	Q	Output data		
D	Input data	R	$\overline{RD}$ signal	Z	Tri-State
H	Logic level high	V	Valid		
L	Logic level low				

POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Startup Time	t_{CSU}		1.8		ms	1
Power-On Reset Delay	t_{POR}			65,536	t_{CLCL}	2

Note 1: Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox.

Note 2: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

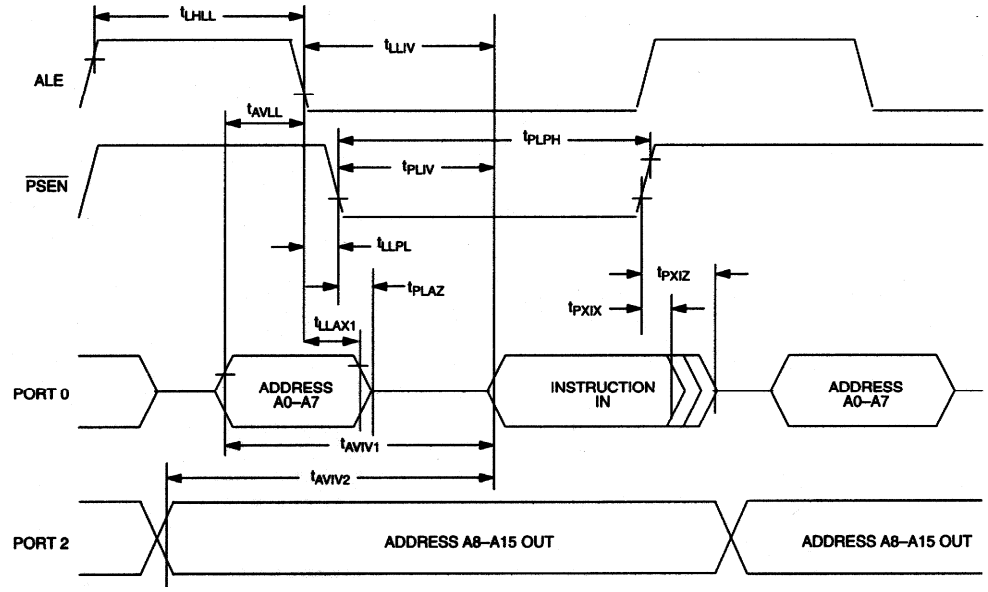
EPROM PROGRAMMING AND VERIFICATION

(V_{CC} = 4.5V to 5.5V, T_A = +21°C to +27°C.)

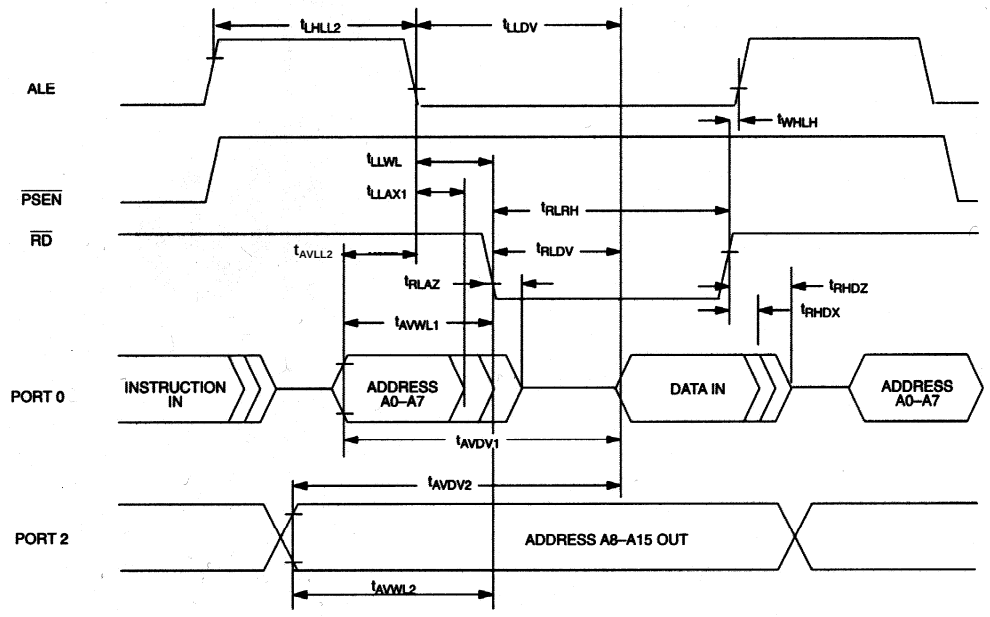
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			50	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
Address Setup to $\overline{PROG}$ Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after $\overline{PROG}$	t_{GHAX}	48 t_{CLCL}				
Data Setup to $\overline{PROG}$ Low	t_{DVGL}	48 t_{CLCL}				
Data Hold after $\overline{PROG}$	t_{GHDX}	48 t_{CLCL}				
Enable High to V_{PP}	t_{EHSH}	48 t_{CLCL}				
V_{PP} Setup to $\overline{PROG}$ Low	t_{SHGL}	10			µs	
V_{PP} Hold after $\overline{PROG}$	t_{SHGL}	10			µs	
$\overline{PROG}$ Width	t_{GLGH}	90		110	µs	
Address to Data Valid	t_{AVQV}			48 t_{CLCL}		
Enable Low to Data Valid	t_{ELQV}			48 t_{CLCL}		
Data Float after Enable	t_{EHQZ}	0		48 t_{CLCL}		
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}	10			µs	

Note 1: All voltages are referenced to ground.

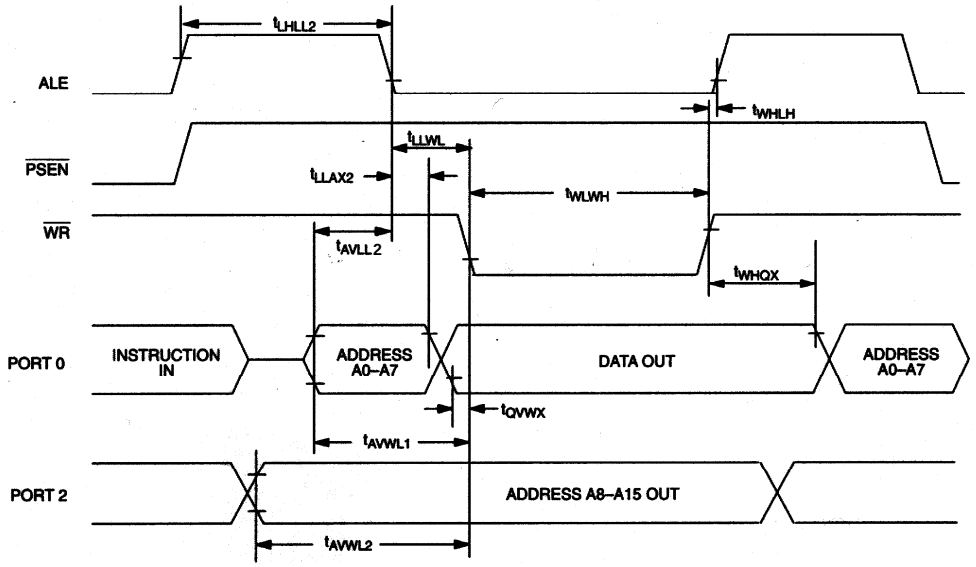
EXTERNAL PROGRAM MEMORY READ CYCLE



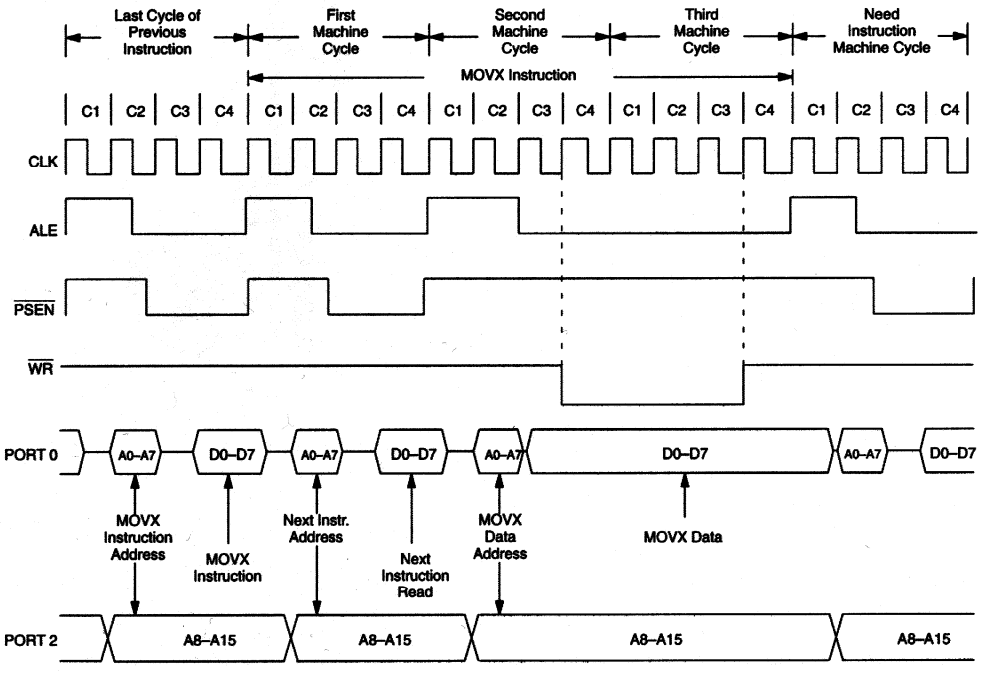
EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1



DATA SHEET REVISION SUMMARY

REVISION	DESCRIPTION
110195	Preliminary release.
022097	1) Update ALE pin description. 2) Add note pertaining to erasure window. 3) Add note pertaining to internal MOVX SRAM. 4) Change Note 10 from RST = 5.5V to RST = V_{CC}. 5) Change serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}.
070698	1) Update PMM operating current estimates 2) Added note to clarify I_{IL} specification. 3) Added note to prevent accidental corruption of Watchdog Timer count while changing counter length. 4) Changed minimum oscillator frequency to 1MHz when using external crystal. 5) Changed RST pulldown resistance from 170kΩ to 200kΩ maximum. 6) Corrected "Data memory write with stretch" diagrams to show falling edge of ALE coincident with rising edge of C3 clock.
070300	1) Corrected P0 pinout description for TQFP package. 2) Clarified point at which reset delay begins.
040104	1) Removed "Preliminary" status. 2) Soldering temperature parameter now references JEDEC specification. 3) Added note to absolute maximums clarifying voltages referenced to ground. 4) Updated I_{CC}, I_{IDLE}, I_{STOP}, I_{SPBG}, I_{IL}, and I_{TL} to incorporate errata conditions. 5) Added note clarifying DC electrical test conditions. 6) Added note clarifying V_{OH3} specification applies to first clock cycle following the transition. 7) Updated AC and MOVX electrical characteristics with final characterization values. Added t_{AVLL2} specification and corrected MOVX timing diagrams to show t_{AVLL2} instead of t_{AVLL}.
070505	1) Added Pb-free/RoHS-compliant part numbers to Ordering Information table. 2) Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.
091605	1) In DC Electrical Characteristics table, added separate specification for DS83C520 V_{PFW}. 2) Changed V_{RST} max to from 4.25V to 4.275V for DS83C520 value.
022207	1) (Page 30) In the Absolute Maximum Ratings table, changed the operating range from 0°C to +70°C to -40°C to +85°C (correction for typographical error; this does not reflect a change in the device or device testing). 2) (Page 33) In the MOVX Characteristics table, added Note 2 and changed t_{RLAZ} max from Note 1 to Note 2.

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