Analog Devices Inc./Maxim Integrated - DS87C520-MNL+ Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c520-mnl

DESCRIPTION

The DS87C520/DS83C520 EPROM/ROM high-speed microcontrollers are fast 8051-compatible microcontrollers. They feature a redesigned processor core without wasted clock and memory cycles. As a result, the devices execute every 8051 instruction between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS87C520/DS83C520 offer a maximum crystal speed of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS87C520/DS83C520 are pin compatible with all three packages of the standard 8051, and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. They feature 16kB of EPROM or mask ROM with an extra 1kB of data RAM. Both OTP and windowed packages are available.

Besides greater speed, the microcontroller includes a second full hardware serial port, seven additional interrupts, programmable Watchdog Timer, Brownout Monitor, and Power-Fail Reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It also can adjust the speed of MOVX data memory access from two to nine machine cycles for flexibility in selecting external memory and peripherals.

A new Power Management Mode (PMM) is useful for portable applications. This feature allows software to select a lower speed clock as the main time base. While normal operation has a machine cycle rate of 4 clocks per cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. For example, at 12MHz, standard operation has a machine cycle rate of 3MHz. In Power Management Mode, software can select either 187.5kHz or 11.7kHz machine cycle rate. There is a corresponding reduction in power consumption when the processor runs slower.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

The DS83C520 is a factory mask ROM version of the DS87C520 designed for high-volume, cost-sensitive applications. It is identical in all respects to the DS87C520, except that the 16kB of EPROM is replaced by a user-supplied application program. All references to features of the DS87C520 will apply to the DS83C520, with the exception of EPROM-specific features where noted. Please contact your local Dallas Semiconductor sales representative for ordering information.

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>30</td><td>33</td><td>27</td><td>ALE</td><td>Address Latch Enable Output. The ALE functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the DS87C520/DS83C520 are in a reset condition. ALE can also be disabled and forced high by writing ALEOFF = 1 (PMR.2). ALE operates independently of ALEOFF during external memory accesses.</td></tr>
<tr><td>39</td><td>43</td><td>37</td><td>P0.0 (AD0)</td><td rowspan="8">Port 0 (AD0–7), I/O. Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pullup resistors are required when using Port 0 as an I/O port.</td></tr>
<tr><td>38</td><td>42</td><td>36</td><td>P0.1 (AD1)</td></tr>
<tr><td>37</td><td>41</td><td>35</td><td>P0.2 (AD2)</td></tr>
<tr><td>36</td><td>40</td><td>34</td><td>P0.3 (AD3)</td></tr>
<tr><td>35</td><td>39</td><td>33</td><td>P0.4 (AD4)</td></tr>
<tr><td>34</td><td>38</td><td>32</td><td>P0.5 (AD5)</td></tr>
<tr><td>33</td><td>37</td><td>31</td><td>P0.6 (AD6)</td></tr>
<tr><td>32</td><td>36</td><td>30</td><td>P0.7 (AD7)</td></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td rowspan="8">Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state; a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are out-lines as follows.

Port Alternate Function
P1.0 T2 External I/O for Timer/Counter 2
P1.1 T2EX EX Timer/Counter 2 Capture/Reload Trigger
P1.2 RXD1 Serial Port 1 Input
P1.3 TXD1 Serial Port 1 Output
P1.4 INT2 External Interrupt 2 (Positive Edge Detect)
P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Negative Edge Detect)
P1.6 INT4 External Interrupt 4 (Positive Edge Detect)
P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Negative Edge Detect)</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td></tr>
</table>

COMPATIBILITY

The DS87C520/DS83C520 are fully static CMOS 8051-compatible microcontrollers designed for high performance. In most cases, the DS87C520/DS83C520 can drop into an existing socket for the 8xc51 family to improve the operation significantly. While remaining familiar to 8051 family users, the devices have many new features. In general, software written for existing 8051-based systems works without modification on the DS87C520/DS83C520. The exception is critical timing since the high-speed microcontrollers performs instructions much faster than the original for any given crystal selection. The DS87C520/DS83C520 run the standard 8051 family instruction set and are pin compatible with DIP, PLCC, or TQFP packages.

The DS87C520/DS83C520 provide three 16-bit timer/counters, full-duplex serial port (2), 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12-clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new four clocks per cycle if desired. The PCA is not supported.

The DS87C520/DS83C520 provide several new hardware features implemented by new special function registers. A summary of these SFRs is provided below.

PERFORMANCE OVERVIEW

The DS87C520/DS83C520 feature a high-speed 8051-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C520/DS83C520, the same machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C520/DS83C520 will see the full 3-to-1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements produce a peak instruction cycle in 121ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the *High-Speed Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C520/DS83C520, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C520/DS83C520 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C520/DS83C520. This allows the DS87C520/DS83C520 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C520/DS83C520 duplicate the SFRs contained in the standard 80C52. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 1. Special Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	C0h
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	C/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

Note: *New functions are in bold.*

MEMORY RESOURCES

Like the 8051, the DS87C520/DS83C520 use three memory areas. The total memory configuration of the DS87C520/DS83C520 is 16kB of ROM, 1kB of data SRAM and 256 bytes of scratchpad or direct RAM. The 1kB of data space SRAM is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1kB as they use different addressing modes and separate instructions.

OPERATIONAL CONSIDERATION

The erasure window of the windowed CERDIP should be covered without regard to the programmed/unprogrammed state of the EPROM. Otherwise, the device may not meet the AC and DC parameters listed in the data sheet.

PROGRAM MEMORY ACCESS

On-chip ROM begins at address 0000h and is contiguous through 3FFFh (16kB). Exceeding the maximum address of on-chip ROM will cause the device to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS87C520/DS83C520 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory, such as Flash, is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory, and then restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 and 2. A depiction of the ROM memory map is shown in Figure 2.

The ROMSIZE register is used to select the maximum on-chip decoded address for ROM. Bits RMS2, RMS1, RMS0 have the following effect.

RMS2	RMS1	RMS0	MAXIMUM ON-CHIP ROM ADDRESS
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB (default)/3FFFh
1	1	0	Invalid—reserved
1	1	1	Invalid—reserved

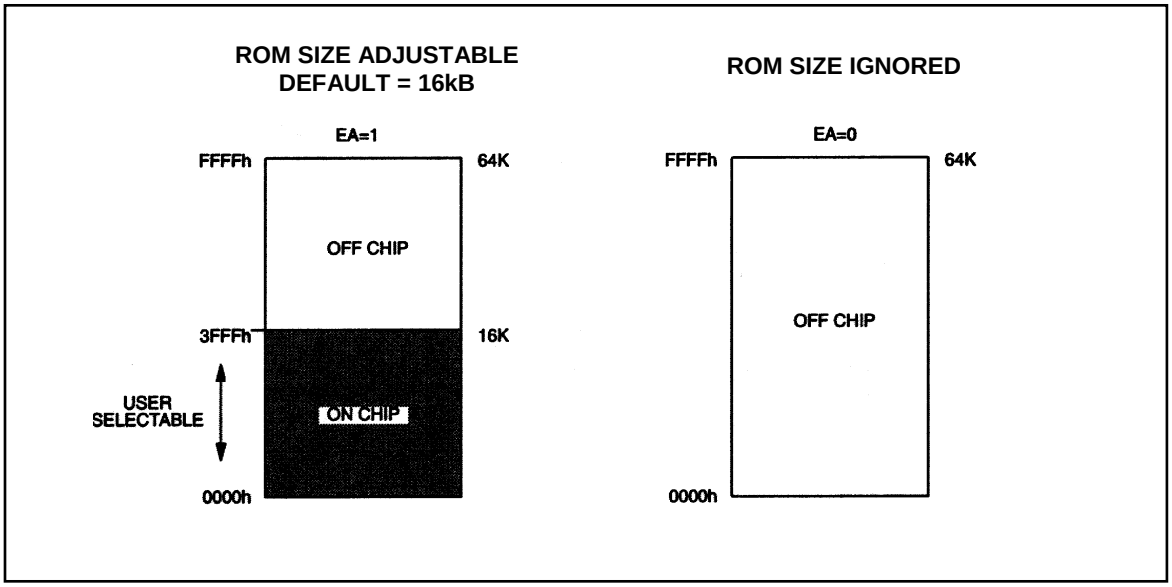
The reset default condition is a maximum on-chip ROM address of 16kB. Thus no action is required if this feature is not used. When accessing external program memory, the first 16kB would be inaccessible. To select a smaller effective ROM size, software must alter bits RMS2–RMS0. Altering these bits requires a Timed-Access procedure as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that the DS87C520/DS83C520 are executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a

16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device will immediately jump to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4kB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

Figure 2. ROM Memory Map



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C520/DS83C520 contain on-chip data memory. They also contain the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

POWER MANAGEMENT

Along with the standard Idle and power down (Stop) modes of the standard 80C52, the DS87C520/DS83C520 provide a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C520/DS83C520 also feature several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C520/DS83C520 use four clocks per machine cycle. Thus the instruction cycle rate is Clock/4. At 33MHz crystal speed, the instruction cycle speed is 8.25MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources - discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 4 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slow and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 5.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle mode, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from Idle, and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)
11.0592	2.765	172.8	10.8
16	4.00	250.0	15.6
25	6.25	390.6	24.4
33	8.25	515.6	32.2

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)
11.0592	13.1	5.3	4.8
16	17.2	6.4	5.6
25	25.7	8.1	7.0
33	32.8	9.8	8.2

Crystal/Ring Operation

The DS87C520/DS83C520 allow software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

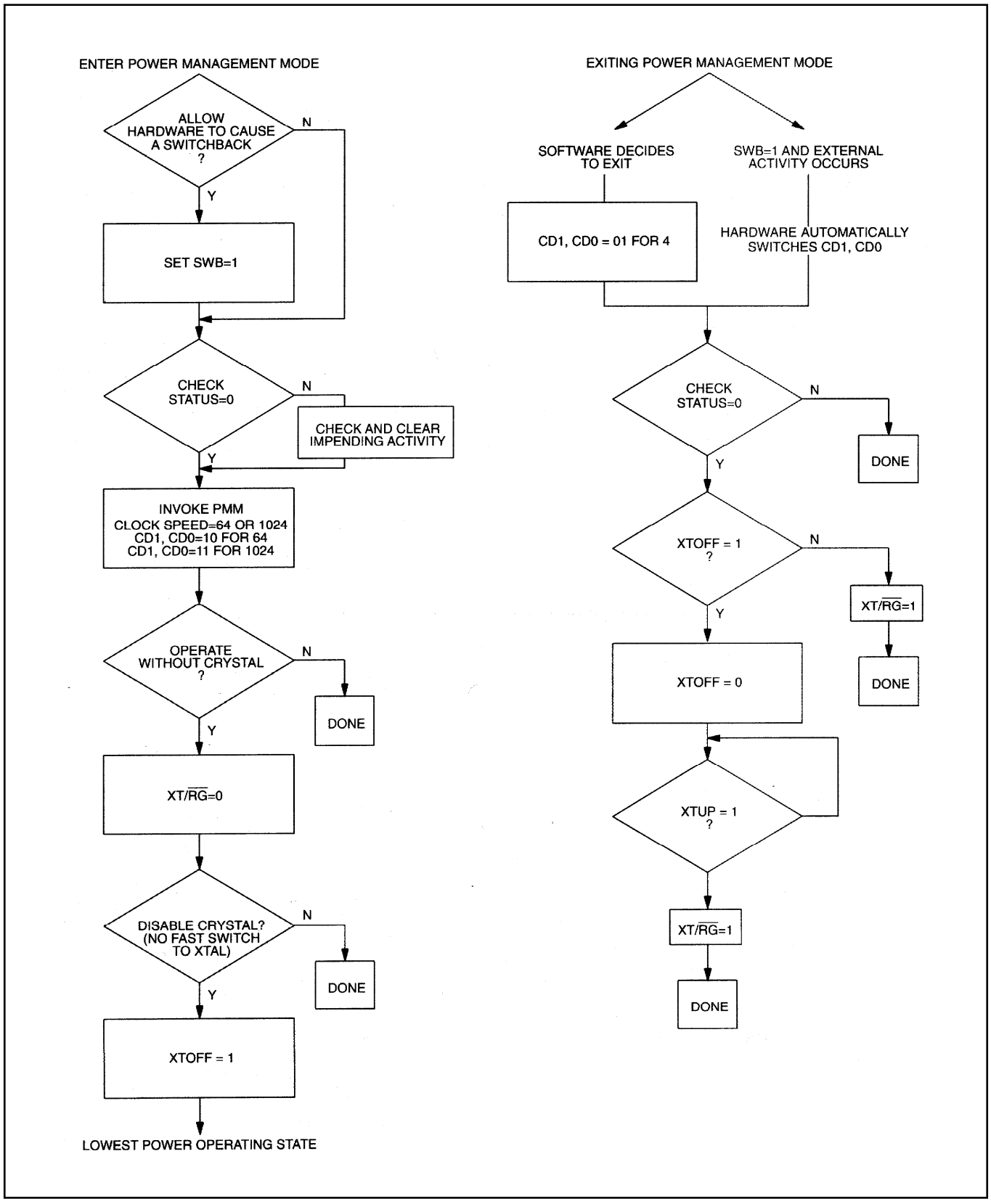
The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one-instruction cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to 0. At this time, the crystal oscillation will begin. The DS87C520/DS83C520 then provide a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to 1 before XTUP=1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystal-less PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

Figure 3 illustrates a typical decision set associated with PMM. Table 6 is a summary of the bits relating to PMM and its operation.

Figure 3. Invoking and Clearing PMM



IDLE MODE

Setting the lsb of the Power Control register (PCON;87h) invokes the Idle mode. Idle will leave internal clocks, serial ports and timers running. Power consumption drops because the CPU is not active. Since clocks are running, the Idle power consumption is a function of crystal frequency. It should be approximately one-half the operational power at a given frequency. The CPU can exit the Idle state with any interrupt or a reset. Idle is available for backward software compatibility. The system can now reduce power consumption to below Idle levels by using PMM1 or PMM2 and running NOPs.

STOP MODE ENHANCEMENTS

Setting Bit 1 of the Power Control register (PCON; 87h) invokes the Stop mode. Stop mode is the lowest power state since it turns off all internal clocking. The I_{CC} f a standard Stop mode is approximately 1µA (but is specified in the Electrical Specifications). The CPU will exit Stop mode from an eternal interrupt or a reset condition. Internally generated interrupts (timer, serial port, Watchdog) are not useful since they require clocking activity.

The DS87C520/DS83C520 provide two enhancements to the Stop mode. As documented below, the device provides a bandgap reference to determine Power-Fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off while in Stop mode. This allows the extremely low-power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. With the bandgap reference enabled, PFI and Power-fail Reset are functional and are a valid means for leaving Stop mode. This allows software to detect and compensate for a brownout or power supply sag, even when in Stop mode. In Stop mode with the bandgap enabled, I_{CC} will be approximately 50µA compared with 1µA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain disabled. Only the most power-sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF; 91h). Setting BGS (EXIF.0) to a 1 will keep the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being off during Stop mode. Note that this bit has no control of the reference during full power, PMM, or Idle modes.

The second feature allows an additional power saving option while also making Stop easier to use. This is the ability to start instantly when exiting Stop mode. It is the internal ring oscillator that provides this feature. This ring can be a clock source when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

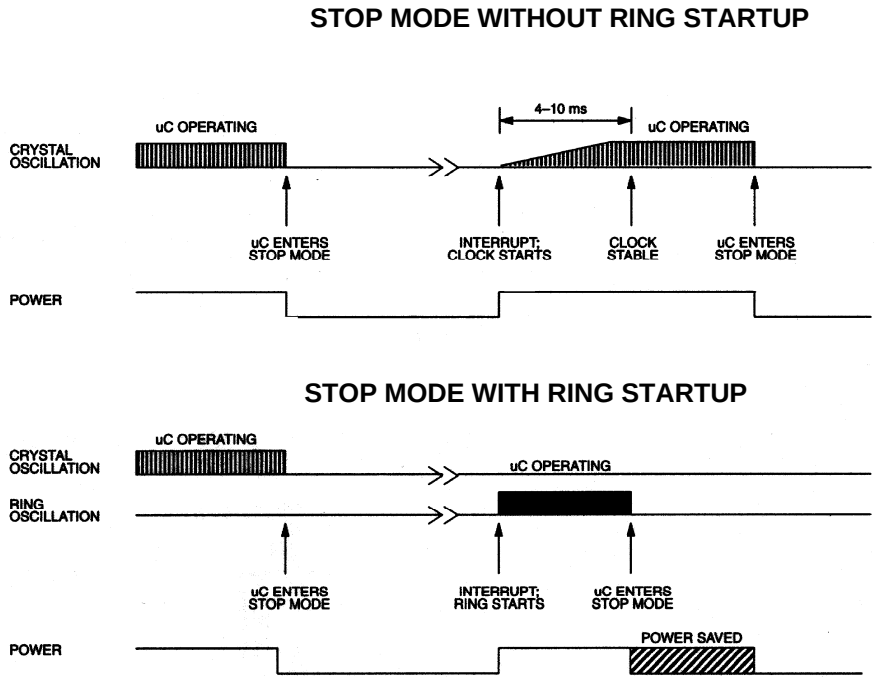
Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual startup time is crystal-dependent, but is normally at least 4ms. A common recommendation is 10 ms. In an application that will wake up, perform a short operation, then return to sleep, the crystal startup can be longer than the real transaction. However, the ring oscillator will start instantly. Running from the ring, the user can perform a simple operation and return to sleep before the crystal has even started. If a user selects the ring to provide the startup clock and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65,536 clocks) has expired. Hardware uses this value to assure proper crystal start even though power is not being cycled.

The ring oscillator runs at approximately 2MHz to 4MHz but will not be a precise value. Do not conduct real-time precision operations (including serial communication) during this ring period. Figure 3 shows

how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL - Ring Select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD-Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

Figure 4. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The microcontroller allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static mode when performing on-chip memory access. The default state of ALEOFF = 0 so ALE toggles at a frequency of XTAL/4.

will set an interrupt flag. Regardless of whether the user enables this interrupt, there are then 512 clocks left until the reset flag is set. Software can enable the interrupt and reset individually. Note that the Watchdog is a free running timer and does not require an enable.

There are 5 control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source.

EWT (WDCON.1) is the enable for the Watchdog timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the timeout. Both of these bits are protected by Timed Access. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4). The Special Function Register map is shown above.

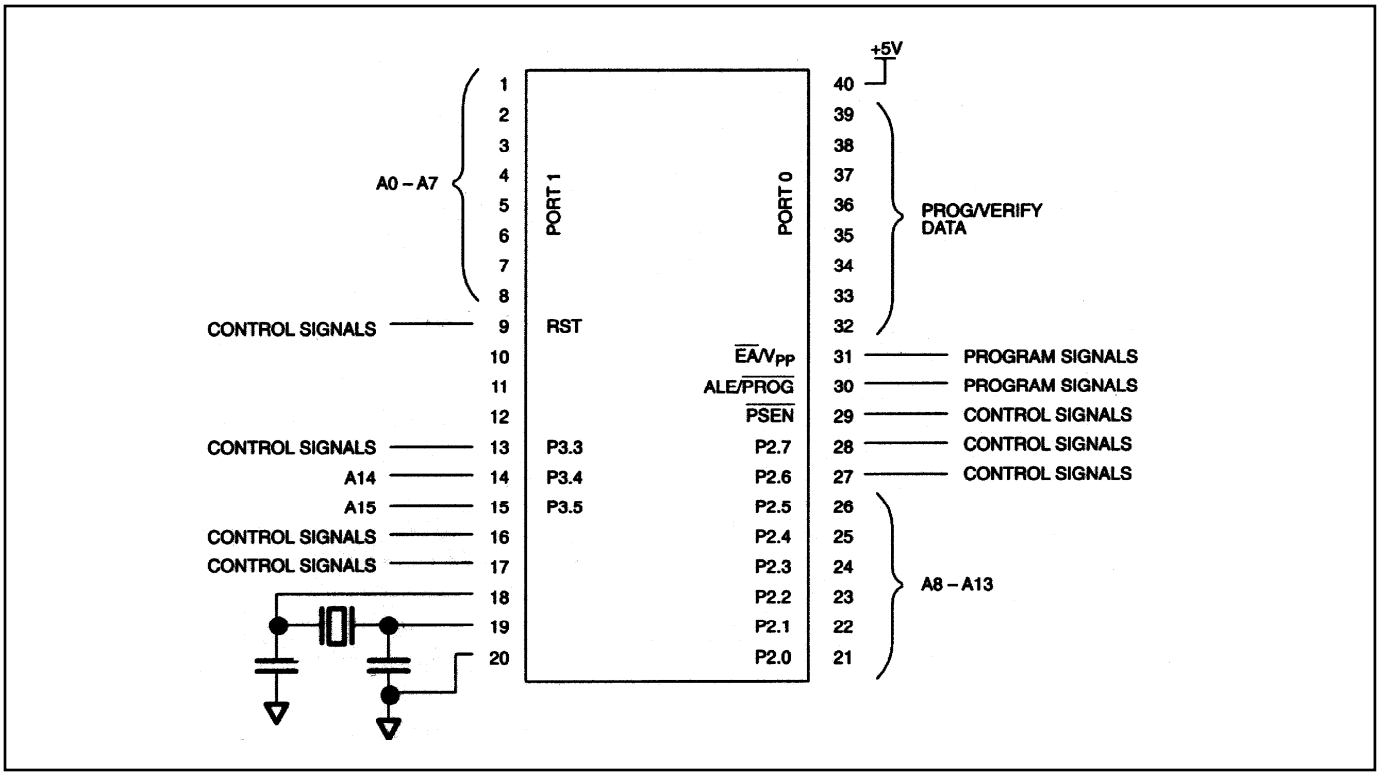
INTERRUPTS

The DS87C520/DS83C520 provide 13 interrupt sources with three priority levels. The Power-Fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

Table 8. Interrupt Sources and Priorities

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power-Fail Interrupt	33h	1	DALLAS
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from serial port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from serial port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Timeout Interrupt	63h	13	DALLAS

Figure 5. EPROM Programming Configuration



ROM-SPECIFIC FEATURES

The DS83C520 supports a subset of the EPROM features found on the DS87C520.

SECURITY OPTIONS

Lock Bits

The DS83C520 employs a lock that restricts viewing of the ROM contents. When set, the lock will prevent MOVC instructions in external memory from reading program bytes in internal memory. When locked, the $\overline{EA}$ pin is sampled and latched on reset. The lock setting is enabled or disabled when the devices are manufactured according to customer specifications. The lock bit cannot be read in software, and its status can only be determined by observing the operation of the device.

Encryption Array

The DS83C520 Encryption Array allows an authorized user to verify ROM without allowing the true memory contents to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the ROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the Encryption Array is programmed (or optionally left unprogrammed) when the devices are manufactured according to customer specifications.

DS83C520 ROM VERIFICATION

The DS83C520 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 5, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C520 SIGNATURE

The Signature bytes identify the DS83C520 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	21h	Model
60h	01h	Extension

MOVX CHARACTERISTICS (continued)

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

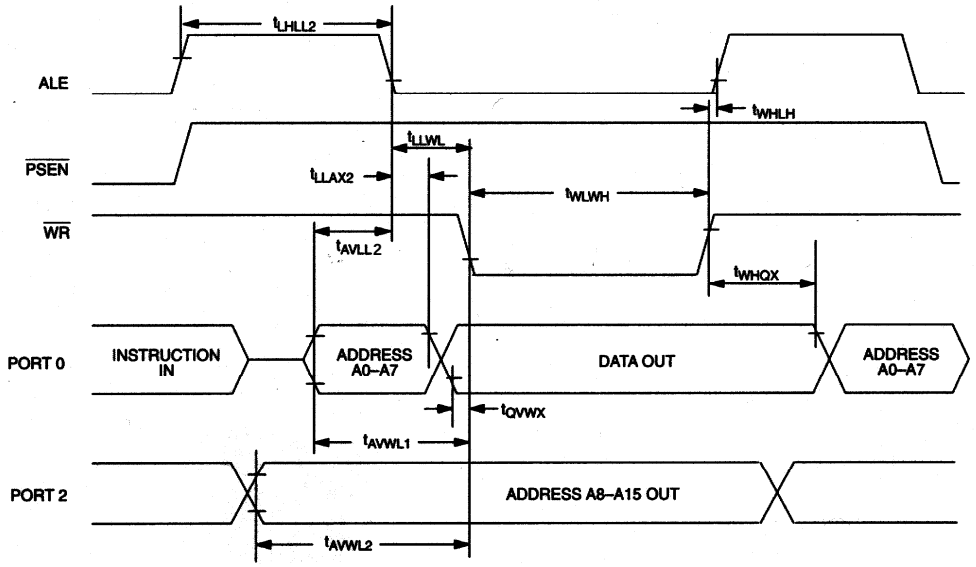
EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCL}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

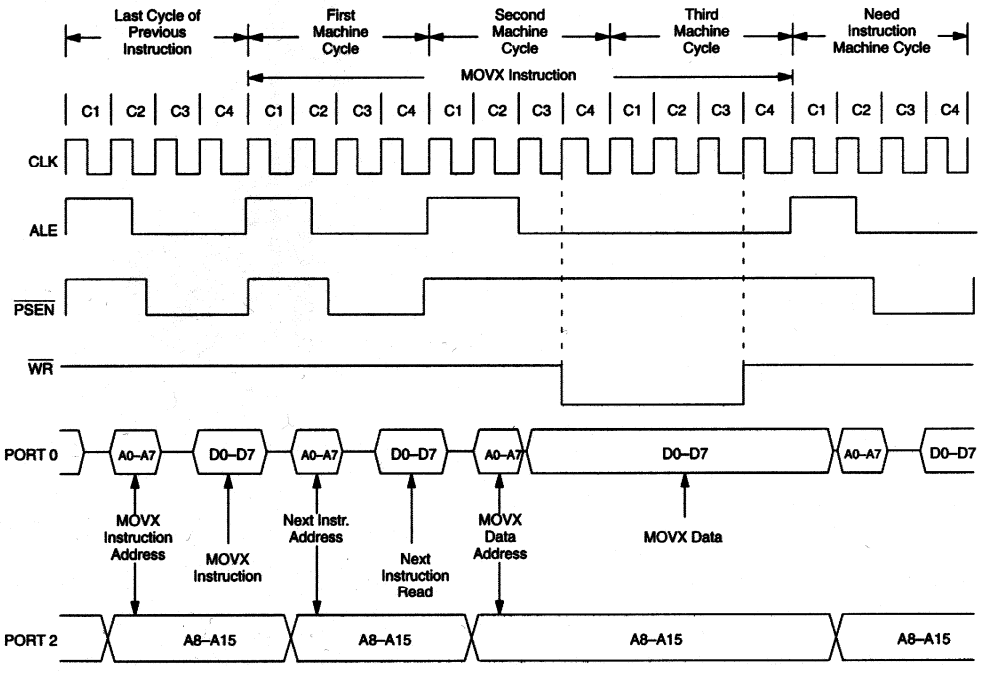
SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0, 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0, 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0, 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0, 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0, 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		

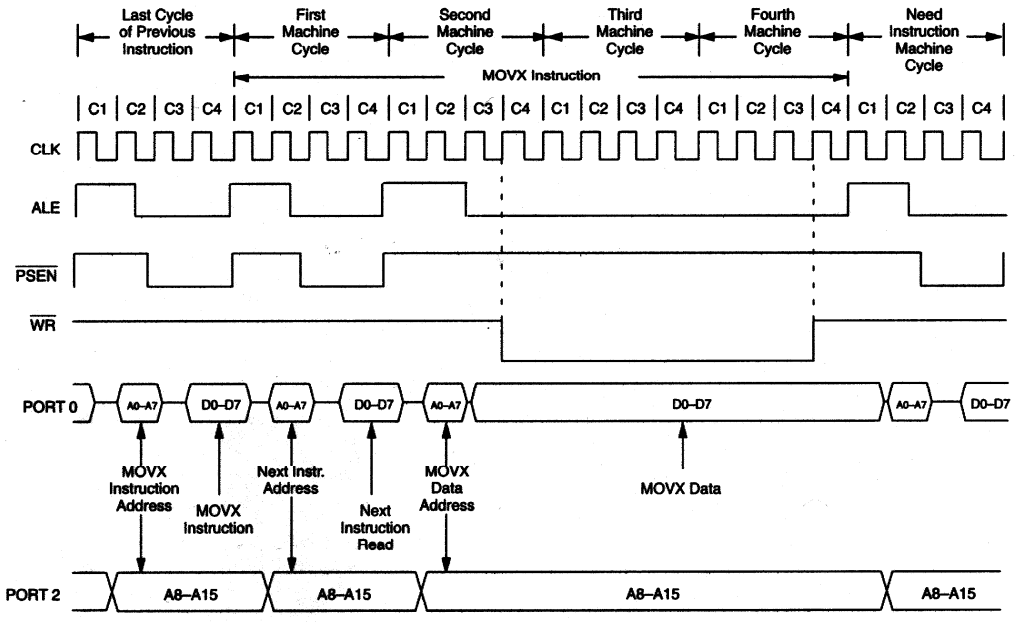
EXTERNAL DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1

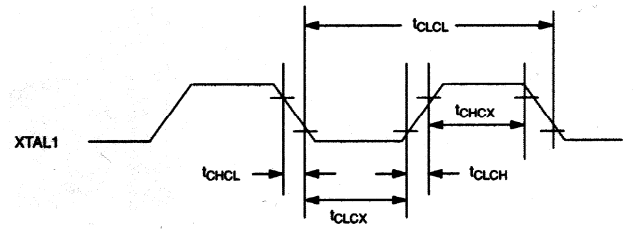


DATA MEMORY WRITE WITH STRETCH = 2

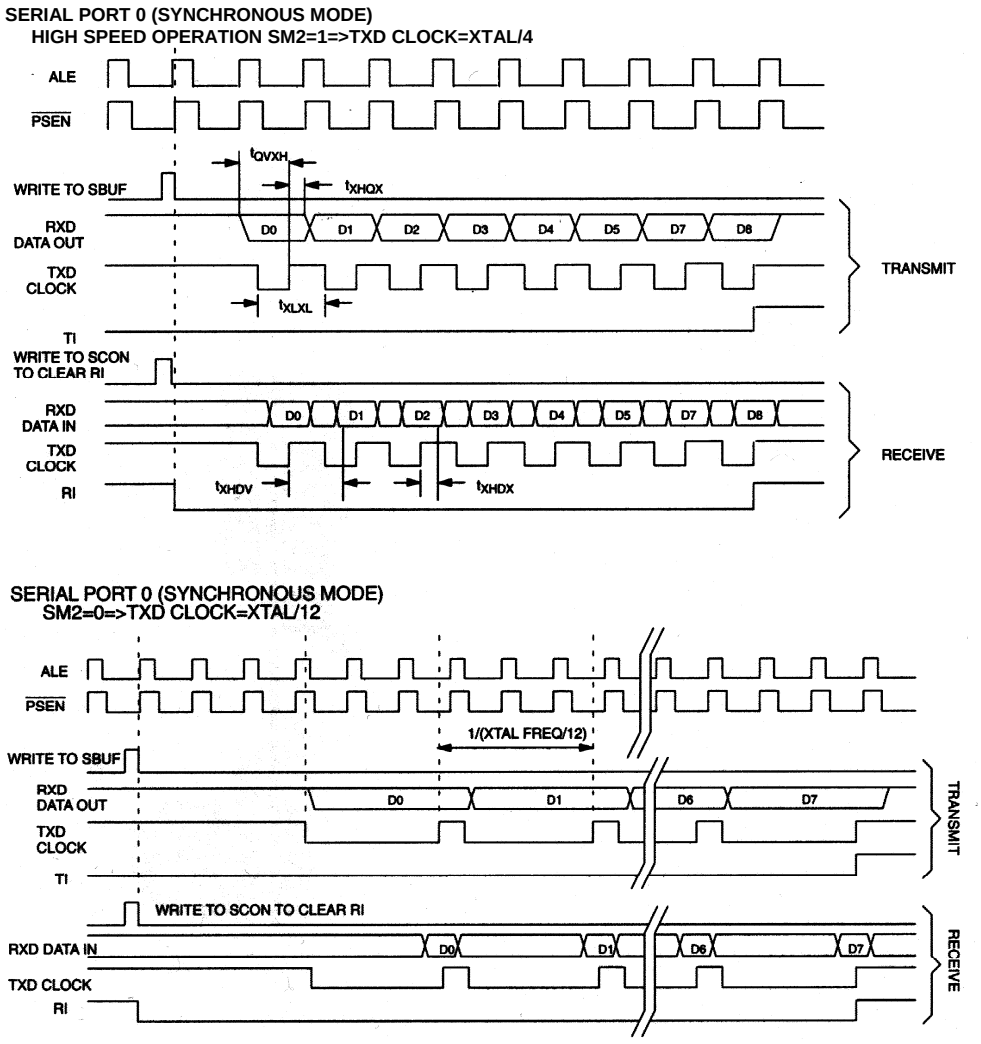


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

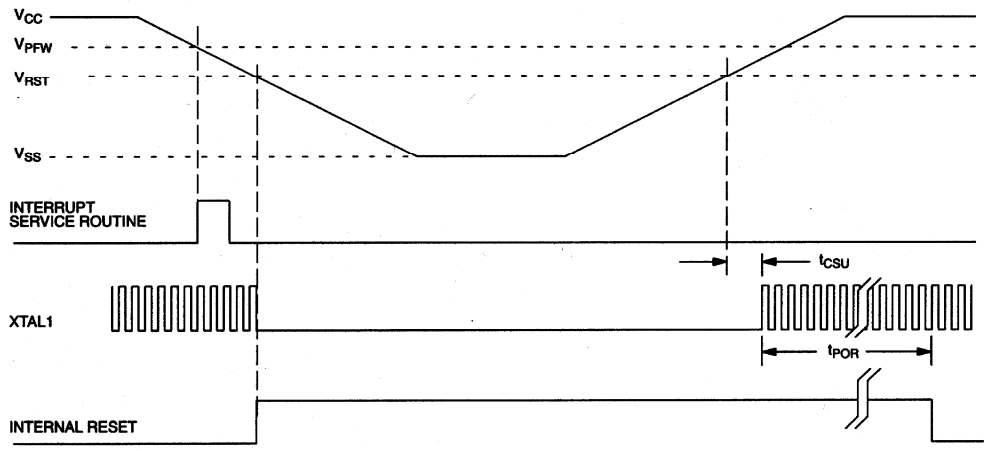
EXTERNAL CLOCK DRIVE



SERIAL PORT MODE 0 TIMING



POWER-CYCLE TIMING



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS