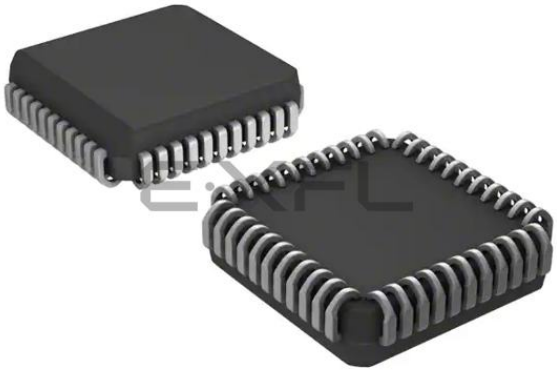
Analog Devices Inc./Maxim Integrated - DS87C520-QCL+ Datasheet



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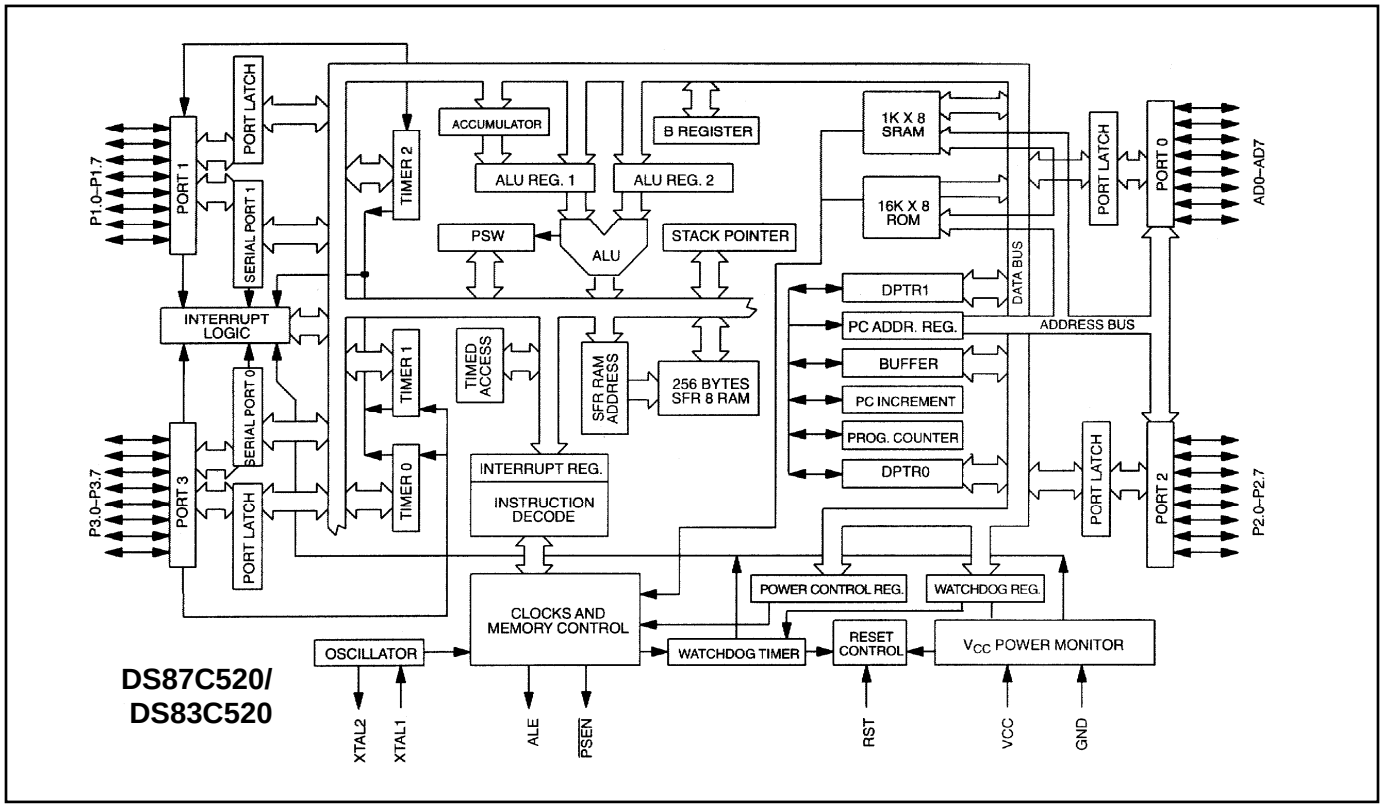
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c520-qcl

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**Positive Supply Voltage.** +5V
20	1, 22, 23	16, 17, 39	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is not required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output.** This active-low signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse and is driven high when external ROM is not being accessed.

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="3">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>DIP</th><th>PLCC</th><th>TQFP</th></tr>
<tr><td>30</td><td>33</td><td>27</td><td>ALE</td><td>Address Latch Enable Output. The ALE functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the DS87C520/DS83C520 are in a reset condition. ALE can also be disabled and forced high by writing ALEOFF = 1 (PMR.2). ALE operates independently of ALEOFF during external memory accesses.</td></tr>
<tr><td>39</td><td>43</td><td>37</td><td>P0.0 (AD0)</td><td rowspan="8">Port 0 (AD0–7), I/O. Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pullup resistors are required when using Port 0 as an I/O port.</td></tr>
<tr><td>38</td><td>42</td><td>36</td><td>P0.1 (AD1)</td></tr>
<tr><td>37</td><td>41</td><td>35</td><td>P0.2 (AD2)</td></tr>
<tr><td>36</td><td>40</td><td>34</td><td>P0.3 (AD3)</td></tr>
<tr><td>35</td><td>39</td><td>33</td><td>P0.4 (AD4)</td></tr>
<tr><td>34</td><td>38</td><td>32</td><td>P0.5 (AD5)</td></tr>
<tr><td>33</td><td>37</td><td>31</td><td>P0.6 (AD6)</td></tr>
<tr><td>32</td><td>36</td><td>30</td><td>P0.7 (AD7)</td></tr>
<tr><td>1</td><td>2</td><td>40</td><td>P1.0</td><td rowspan="8">Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input state; a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are out-lines as follows.

Port Alternate Function
P1.0 T2 External I/O for Timer/Counter 2
P1.1 T2EX EX Timer/Counter 2 Capture/Reload Trigger
P1.2 RXD1 Serial Port 1 Input
P1.3 TXD1 Serial Port 1 Output
P1.4 INT2 External Interrupt 2 (Positive Edge Detect)
P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Negative Edge Detect)
P1.6 INT4 External Interrupt 4 (Positive Edge Detect)
P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Negative Edge Detect)</td></tr>
<tr><td>2</td><td>3</td><td>41</td><td>P1.1</td></tr>
<tr><td>3</td><td>4</td><td>42</td><td>P1.2</td></tr>
<tr><td>4</td><td>5</td><td>43</td><td>P1.3</td></tr>
<tr><td>5</td><td>6</td><td>44</td><td>P1.4</td></tr>
<tr><td>6</td><td>7</td><td>1</td><td>P1.5</td></tr>
<tr><td>7</td><td>8</td><td>2</td><td>P1.6</td></tr>
<tr><td>8</td><td>9</td><td>3</td><td>P1.7</td></tr>
</table>

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C520/DS83C520, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C520/DS83C520 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C520/DS83C520. This allows the DS87C520/DS83C520 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C520/DS83C520 duplicate the SFRs contained in the standard 80C52. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 1. Special Function Register Locations

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	C0h
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	C/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

Note: *New functions are in bold.*

MEMORY RESOURCES

Like the 8051, the DS87C520/DS83C520 use three memory areas. The total memory configuration of the DS87C520/DS83C520 is 16kB of ROM, 1kB of data SRAM and 256 bytes of scratchpad or direct RAM. The 1kB of data space SRAM is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1kB as they use different addressing modes and separate instructions.

OPERATIONAL CONSIDERATION

The erasure window of the windowed CERDIP should be covered without regard to the programmed/unprogrammed state of the EPROM. Otherwise, the device may not meet the AC and DC parameters listed in the data sheet.

PROGRAM MEMORY ACCESS

On-chip ROM begins at address 0000h and is contiguous through 3FFFh (16kB). Exceeding the maximum address of on-chip ROM will cause the device to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS87C520/DS83C520 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory, such as Flash, is used. The maximum memory size is dynamically variable. Thus a portion of memory can be removed from the memory map to access off-chip memory, and then restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map allowing the full 64kB memory space to be addressed from off-chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 and 2. A depiction of the ROM memory map is shown in Figure 2.

The ROMSIZE register is used to select the maximum on-chip decoded address for ROM. Bits RMS2, RMS1, RMS0 have the following effect.

RMS2	RMS1	RMS0	MAXIMUM ON-CHIP ROM ADDRESS
0	0	0	0kB
0	0	1	1kB/03FFh
0	1	0	2kB/07FFh
0	1	1	4kB/0FFFh
1	0	0	8kB/1FFFh
1	0	1	16kB (default)/3FFFh
1	1	0	Invalid—reserved
1	1	1	Invalid—reserved

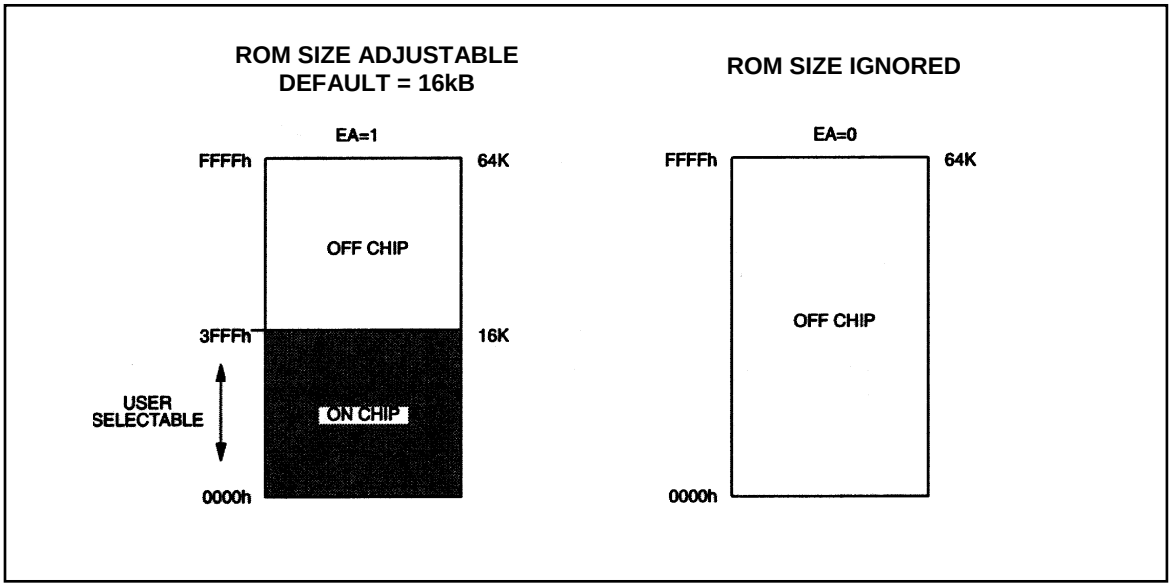
The reset default condition is a maximum on-chip ROM address of 16kB. Thus no action is required if this feature is not used. When accessing external program memory, the first 16kB would be inaccessible. To select a smaller effective ROM size, software must alter bits RMS2–RMS0. Altering these bits requires a Timed-Access procedure as explained later.

Care should be taken so that changing the ROMSIZE register does not corrupt program execution. For example, assume that the DS87C520/DS83C520 are executing instructions from internal program memory near the 12kB boundary (~3000h) and that the ROMSIZE register is currently configured for a

16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device will immediately jump to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4kB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

Figure 2. ROM Memory Map



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C520/DS83C520 contain on-chip data memory. They also contain the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C520/DS83C520 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using 2 bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

Table 2. Data Memory Access Control

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h–FFFFh	External data memory (*default condition)*
0	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFFh	External data memory
1	0	Reserved	Reserved
1	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFBh	Reserved—no external access
		FFFCh	Read access to the status of lock bits
		FFFDh–FFFFh	Reserved—no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2–0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

Note: After internal MOVX SRAM has been initialized, changing the DME0/1 bits has no effect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C520/DS83C520 allow software to adjust the speed of off-chip data memory access. The microcontrollers can perform the MOVX in as few as two instruction cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch

setting. When desiring maximum speed, software should select a Stretch value of 0. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. Also, setup and hold times are increased by 1 clock when using any Stretch greater than 0. This results in a wider read/write strobe and relaxed interface timing, allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is in the *Electrical Specifications* section. Table 3 shows the resulting strobe widths for each Stretch value. The memory Stretch uses the Clock Control Special Function Register at SFR location 8Eh. The Stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first Stretch (default) allows the use of common 120ns RAMs without dramatically lengthening the memory access.

Table 3. Data Memory Cycle Stretch Values

CKCON.2-0			MEMORY CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME at 33MHz (ns)
M2	M1	M0			
0	0	0	2 (forced internal)	2	60
0	0	1	3 (default external)	4	121
0	1	0	4	8	242
0	1	1	5	12	364
1	0	0	6	16	485
1	0	1	7	20	606
1	1	0	8	24	727
1	1	1	9	28	848

DUAL DATA POINTER

The timing of block moves of data memory is faster using the Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS87C520/DS83C520, this data pointer is called DPTR0, located at SFR addresses 82h and 83h. These are the original locations. Using DPTR requires no modification of standard code. The new DPTR at SFR 84h and 85h is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer. Its location is the lsb of the SFR location 86h. No other bits in register 86h have any effect and are 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore it takes only one instruction to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. The software simply switches between DPTR0 and 1 once software loads them. The relevant register locations are as follows:

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C520/DS83C520 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal and ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h).

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Table 6. PMM Control and Status Bit Summary

BIT	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{RG}$	EXIF.3	Control. XT/$\overline{RG}$ = 1, runs from crystal or external clock; XT/$\overline{RG}$ = 0, runs from internal ring oscillator.	X	0 to 1 only when XTUP = 1 and XTOFF = 0
RGMD	EXIF.2	Status. RGMD = 1, CPU clock = ring; RGMD = 0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1, 0 = 01, 4 clocks; CS1, 0 = 10, PMM1; CD1, 0 = 11, PMM2.	0, 1	Write CD1, 0 = 10 or 11 only from CD1, 0 = 01
SWB	PMR.5	Control. SWB = 1, hardware invokes switchback to 4 clocks, SWB = 0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{RG}$ = 0
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

PERIPHERAL OVERVIEW

The DS87C520/DS83C520 provide several of the most commonly needed peripheral functions in micro-computer-based systems. These new functions include a second serial port, power-fail reset, power-fail interrupt, and a programmable watchdog timer. These are described in the following paragraphs. More details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C520/DS83C520 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C520/DS83C520 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C520/DS83C520 architecture normally uses four clocks per machine cycle. However, in the area of timers and serial ports, the DS87C520/DS83C520 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON;8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS87C520/DS83C520 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C520/DS83C520 use 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C520/DS83C520 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

TIMED-ACCESS PROTECTION

It is useful to protect certain SFR bits from an accidental write operation. The Timed Access procedure stops an errant CPU from accidentally changing these bits. It requires that the following instructions precede a write of a protected bit.

```
MOV     0C7h,   #0Aah
MOV     0C7h,   #55h
```

Writing an AAh then a 55h to the Timed Access register (location C7h) opens a 3-cycle window for write access. The window allows software to modify a protected bit(s). If these instructions do not immediately precede the write operation, then the write will not take effect. The protected bits are:

EXIF.0	BGS	Bandgap Select
WDCON.6	POR	Power-On Reset flag
WDCON.1	EWT	Enable Watchdog Reset
WDCON.0	RWT	Restart Watchdog
WDCON.3	WDIF	Watchdog Interrupt Flag
ROMSIZE.2	RMS2	ROM Size Select 2
ROMSIZE.1	RMS1	ROM Size Select 1
ROMSIZE.0	RMS0	ROM Size Select 0

EPROM PROGRAMMING

The DS87C520 follows standards for a 16kB EPROM version in the 8051 family. It is available in a UV-erasable, ceramic-windowed package and in plastic packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options. ROM-specific features are described later in this data sheet.

Most commercially available device programmers will directly support Dallas Semiconductor microcontrollers. If your programmer does not, please contact the manufacturer for updated software.

PROGRAMMING PROCEDURE

The DS87C520 should run from a clock speed between 4MHz and 6MHz when being programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 9. The diagram in Table 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the *Electrical Specifications* section.

Program the DS87C520 as follows:

1) Apply the address value,
2) Apply the data value,
3) Select the programming option from Table 9 using the control signals,
4) Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM,
5) Pulse the $\overline{PROG}$ signal five times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits,
6) Repeat as many times as necessary.

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 9. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

OTHER EPROM OPTIONS

The DS87C520 has user selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

Program the EPROM selectable options as shown in Table 9. The Option Register sets or reads these selections. The bits in the Option Control Register have the following function:

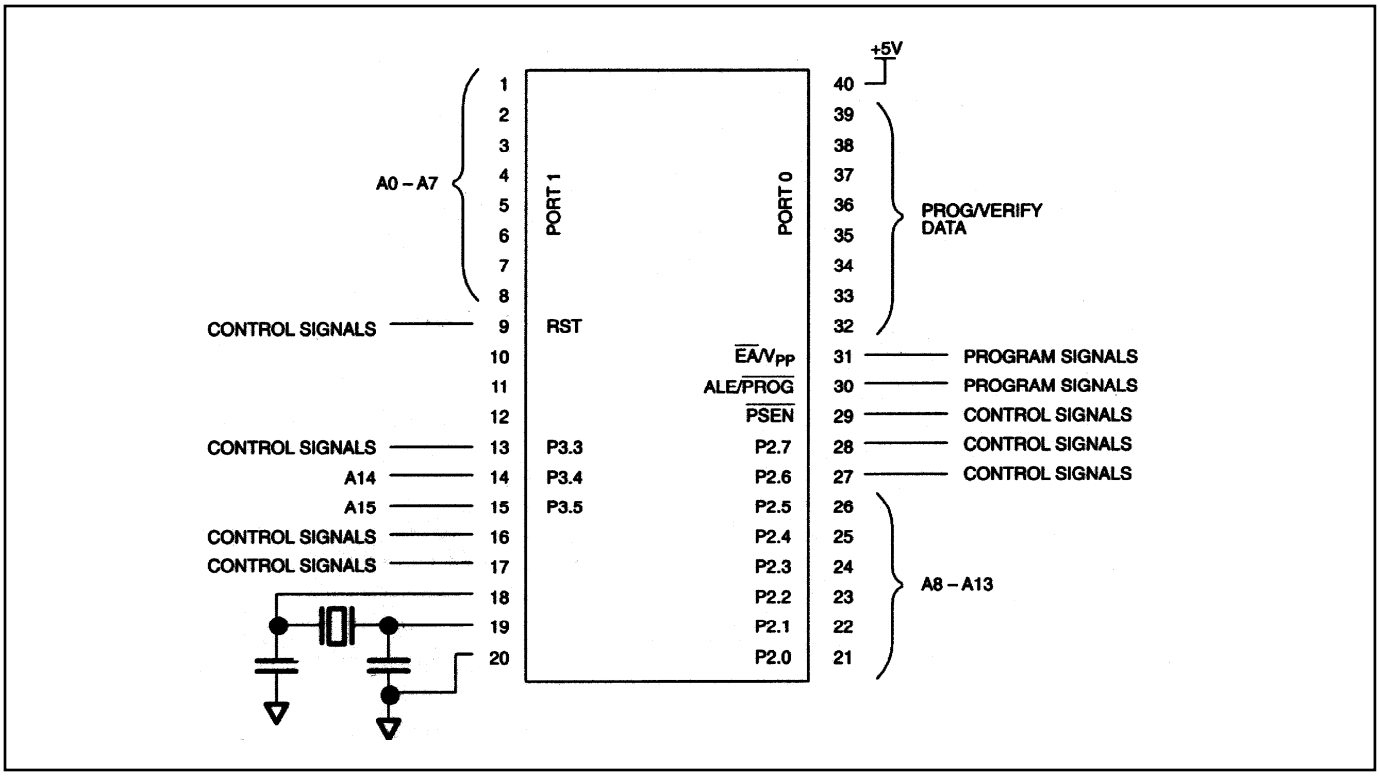
Bits 7 to 4	Reserved, program to a 1.
Bit 3	Watchdog POR default. Set = 1; watchdog reset function is disabled on power-up. Set = 0; watchdog reset function is enabled automatically.
Bits 2 to 0	Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	20h	Model
60h	01h	Extension

Figure 5. EPROM Programming Configuration



ROM-SPECIFIC FEATURES

The DS83C520 supports a subset of the EPROM features found on the DS87C520.

SECURITY OPTIONS

Lock Bits

The DS83C520 employs a lock that restricts viewing of the ROM contents. When set, the lock will prevent MOVC instructions in external memory from reading program bytes in internal memory. When locked, the $\overline{EA}$ pin is sampled and latched on reset. The lock setting is enabled or disabled when the devices are manufactured according to customer specifications. The lock bit cannot be read in software, and its status can only be determined by observing the operation of the device.

Encryption Array

The DS83C520 Encryption Array allows an authorized user to verify ROM without allowing the true memory contents to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the ROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the Encryption Array is programmed (or optionally left unprogrammed) when the devices are manufactured according to customer specifications.

AC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	33 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	40		$1.5t_{CLCL}$-5		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	10		$0.5t_{CLCL}$-5		ns
Address Hold after ALE Low		t_{LLAX1}	(Note 2)		(Note 2)		ns
ALE Low to Valid Instruction In		t_{LLIV}		43		$2.5t_{CLCL}$-33	ns
ALE Low to $\overline{\text{PSEN}}$ Low		t_{LLPL}	4		$0.5t_{CLCL}$-11		ns
$\overline{\text{PSEN}}$ Pulse Width		t_{PLPH}	55		$2t_{CLCL}$-5		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In		t_{PLIV}		37		$2t_{CLCL}$-24	ns
Input Instruction Hold after $\overline{\text{PSEN}}$		t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$		t_{PXIZ}		26		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		59		$3t_{CLCL}$-32	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		68		$3.5t_{CLCL}$-38	ns
$\overline{\text{PSEN}}$ Low to Address Float		t_{PLAZ}		(Note 2)		(Note 2)	ns

Note 1: All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics are not 100% tested, but are characterized and guaranteed by design. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns may cause contention. This will not damage the parts, but will cause an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}$-5		ns	t_{MCS}=0
		$2t_{CLCL}$-5			t_{MCS}>0
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL}$-5		ns	t_{MCS}=0
		t_{CLCL}-5			t_{MCS}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$-10		ns	t_{MCS}=0
		t_{CLCL}-7			t_{MCS}>0
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-22	ns	t_{MCS}=0
			t_{MCS}-24		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	—
Data Float after Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-31	ns	t_{MCS}=0
			$t_{MCS}+t_{CLCL}$-26		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-29	ns	t_{MCS}=0
			$t_{MCS}+2t_{CLCL}$-29		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-37	ns	t_{MCS}=0
			$t_{MCS}+2.5t_{CLCL}$-37		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-10	$0.5t_{CLCL}$+5	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-9		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-17		ns	t_{MCS}=0
		$2.5t_{CLCL}$-16			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-6		ns	—
Data Hold after Write	t_{WHQX}	t_{CLCL}-5		ns	t_{MCS}=0
		$2t_{CLCL}$-6			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 2)	ns	—
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-4	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0

Note 1: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, the DS87C520 and DS83C520 specify the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time	I	Instruction	W	$\overline{WR}$ signal
A	Address	P	$\overline{PSEN}$	X	No longer a valid logic level
C	Clock	Q	Output data		
D	Input data	R	$\overline{RD}$ signal	Z	Tri-State
H	Logic level high	V	Valid		
L	Logic level low				

POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Startup Time	t_{CSU}		1.8		ms	1
Power-On Reset Delay	t_{POR}			65,536	t_{CLCL}	2

Note 1: Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox.

Note 2: Reset delay is a synchronous counter of crystal oscillations after crystal startup. Counting begins when the level on the XTAL1 pin meets the V_{IH2} criteria. At 33MHz, this time is 1.99ms.

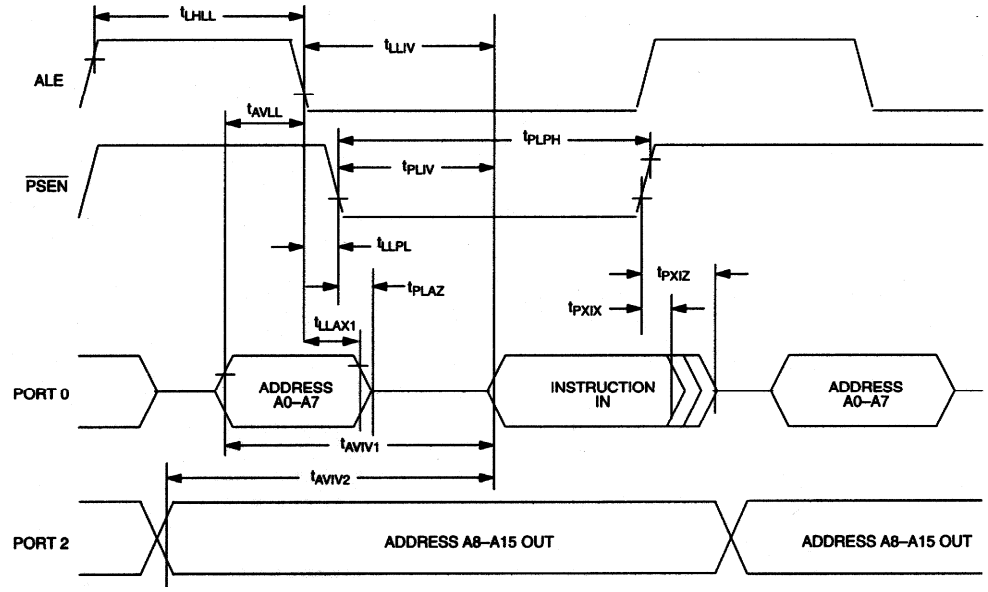
EPROM PROGRAMMING AND VERIFICATION

(V_{CC} = 4.5V to 5.5V, T_A = +21°C to +27°C.)

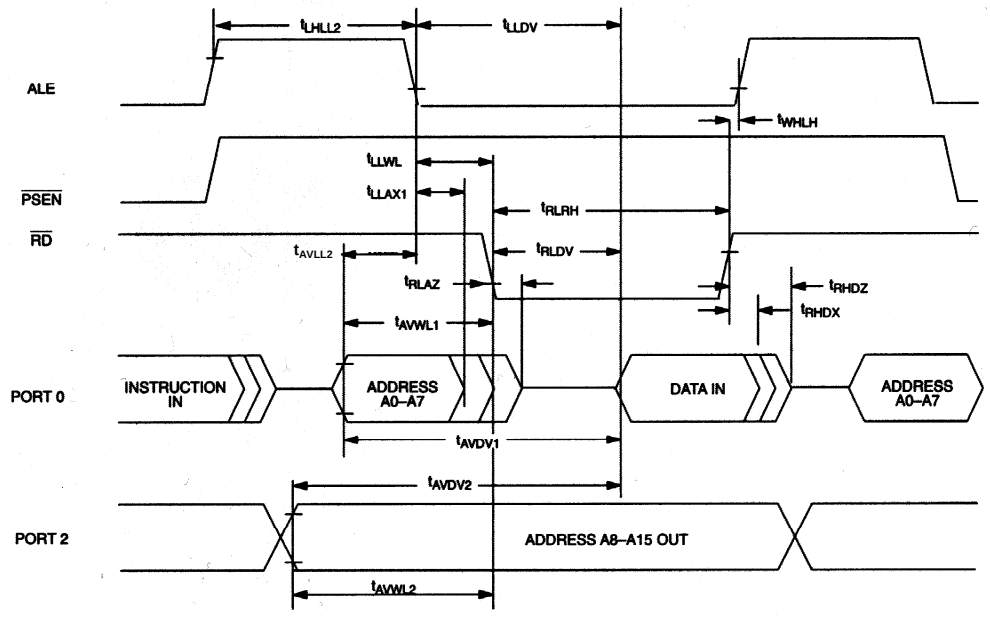
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			50	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
Address Setup to $\overline{PROG}$ Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after $\overline{PROG}$	t_{GHAX}	48 t_{CLCL}				
Data Setup to $\overline{PROG}$ Low	t_{DVGL}	48 t_{CLCL}				
Data Hold after $\overline{PROG}$	t_{GHDX}	48 t_{CLCL}				
Enable High to V_{PP}	t_{EHSH}	48 t_{CLCL}				
V_{PP} Setup to $\overline{PROG}$ Low	t_{SHGL}	10			µs	
V_{PP} Hold after $\overline{PROG}$	t_{SHGL}	10			µs	
$\overline{PROG}$ Width	t_{GLGH}	90		110	µs	
Address to Data Valid	t_{AVQV}			48 t_{CLCL}		
Enable Low to Data Valid	t_{ELQV}			48 t_{CLCL}		
Data Float after Enable	t_{EHQZ}	0		48 t_{CLCL}		
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}	10			µs	

Note 1: All voltages are referenced to ground.

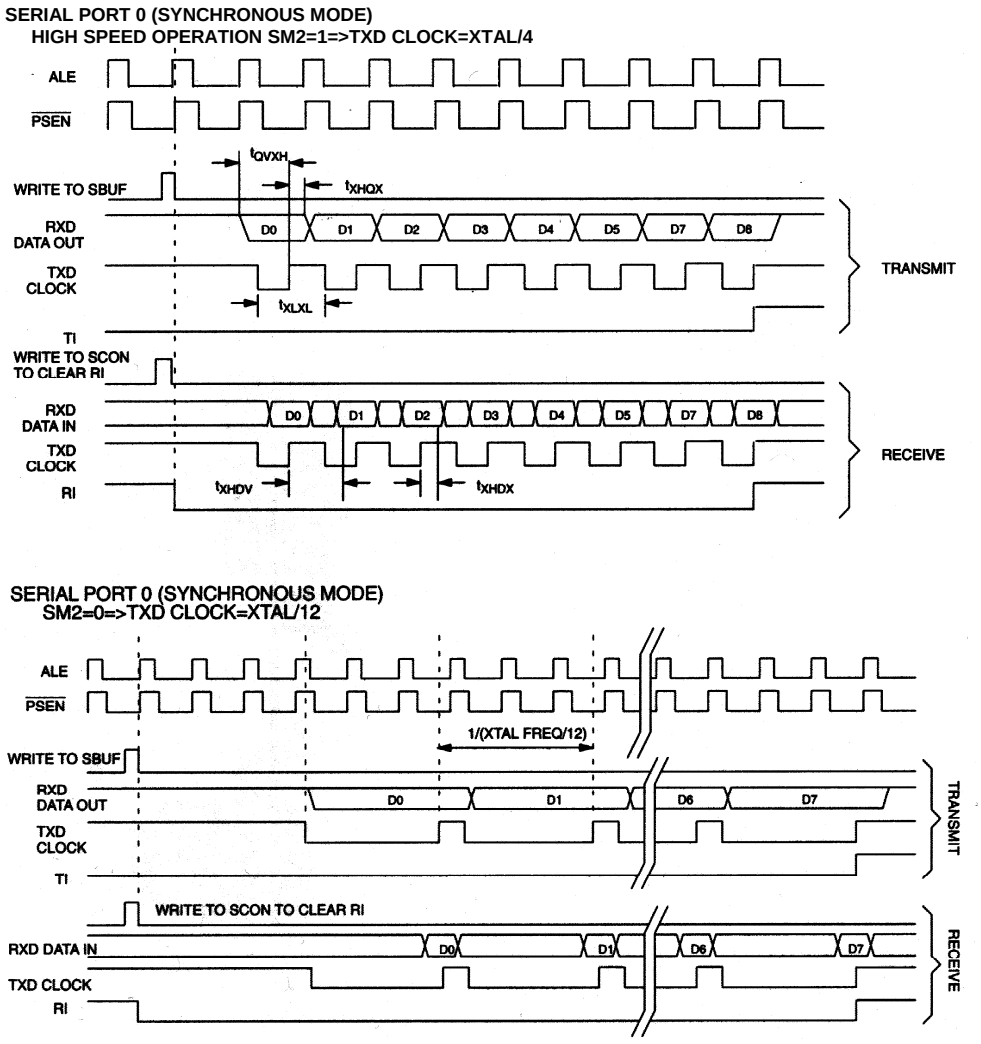
EXTERNAL PROGRAM MEMORY READ CYCLE



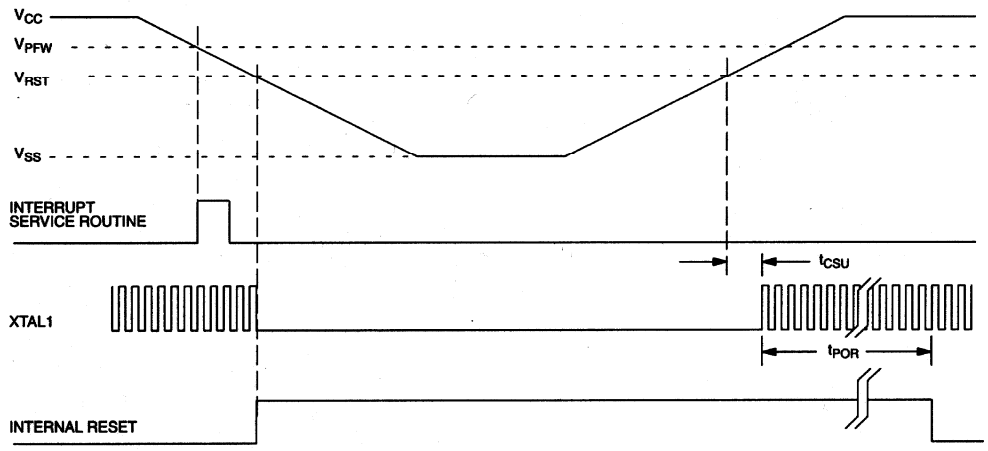
EXTERNAL DATA MEMORY READ CYCLE



SERIAL PORT MODE 0 TIMING



POWER-CYCLE TIMING



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS