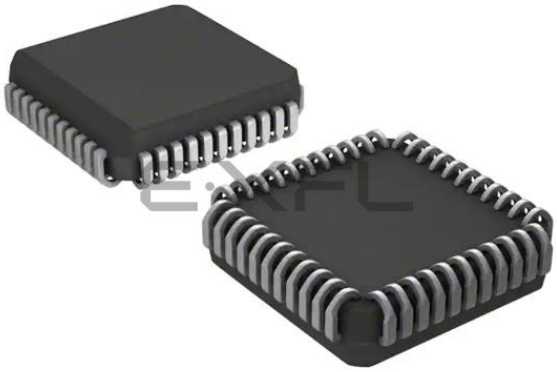
Analog Devices Inc./Maxim Integrated - DS87C520-QNL+ Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c520-qnl

ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS87C520-MCL	0˚C to +70˚C	33	40 Plastic DIP
DS87C520-MCL+	0˚C to +70˚C	33	40 Plastic DIP
DS87C520-QCL	0˚C to +70˚C	33	44 PLCC
DS87C520-QCL+	0˚C to +70˚C	33	44 PLCC
DS87C520-ECL	0˚C to +70˚C	33	44 TQFP
DS87C520-ECL+	0˚C to +70˚C	33	44 TQFP
DS87C520-MNL	-40˚C to +85˚C	33	40 Plastic DIP
DS87C520-MNL+	-40˚C to +85˚C	33	40 Plastic DIP
DS87C520-QNL	-40˚C to +85˚C	33	44 PLCC
DS87C520-QNL+	-40˚C to +85˚C	33	44 PLCC
DS87C520-ENL	-40˚C to +85˚C	33	44 TQFP
DS87C520-ENL+	-40˚C to +85˚C	33	44 TQFP
DS87C520-WCL*	0˚C to +70˚C	33	40 Windowed CERDIP
DS83C520-MCL	0˚C to +70˚C	33	40 Plastic DIP
DS83C520-MCL+	0˚C to +70˚C	33	40 Plastic DIP
DS83C520-QCL	0˚C to +70˚C	33	44 PLCC
DS83C520-QCL+	0˚C to +70˚C	33	44 PLCC
DS83C520-ECL	0˚C to +70˚C	33	44 TQFP
DS83C520-ECL+	0˚C to +70˚C	33	44 TQFP
DS83C520-MNL	-40˚C to +85˚C	33	40 Plastic DIP
DS83C520-MNL+	-40˚C to +85˚C	33	40 Plastic DIP
DS83C520-QNL	-40˚C to +85˚C	33	44 PLCC
DS83C520-QNL+	-40˚C to +85˚C	33	44 TQFP
DS83C520-ENL	-40˚C to +85˚C	33	44 TQFP
DS83C520-ENL+	-40˚C to +85˚C	33	44 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

** The windowed ceramic DIP package is intrinsically lead(Pb) free.*

DESCRIPTION

The DS87C520/DS83C520 EPROM/ROM high-speed microcontrollers are fast 8051-compatible microcontrollers. They feature a redesigned processor core without wasted clock and memory cycles. As a result, the devices execute every 8051 instruction between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS87C520/DS83C520 offer a maximum crystal speed of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS87C520/DS83C520 are pin compatible with all three packages of the standard 8051, and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. They feature 16kB of EPROM or mask ROM with an extra 1kB of data RAM. Both OTP and windowed packages are available.

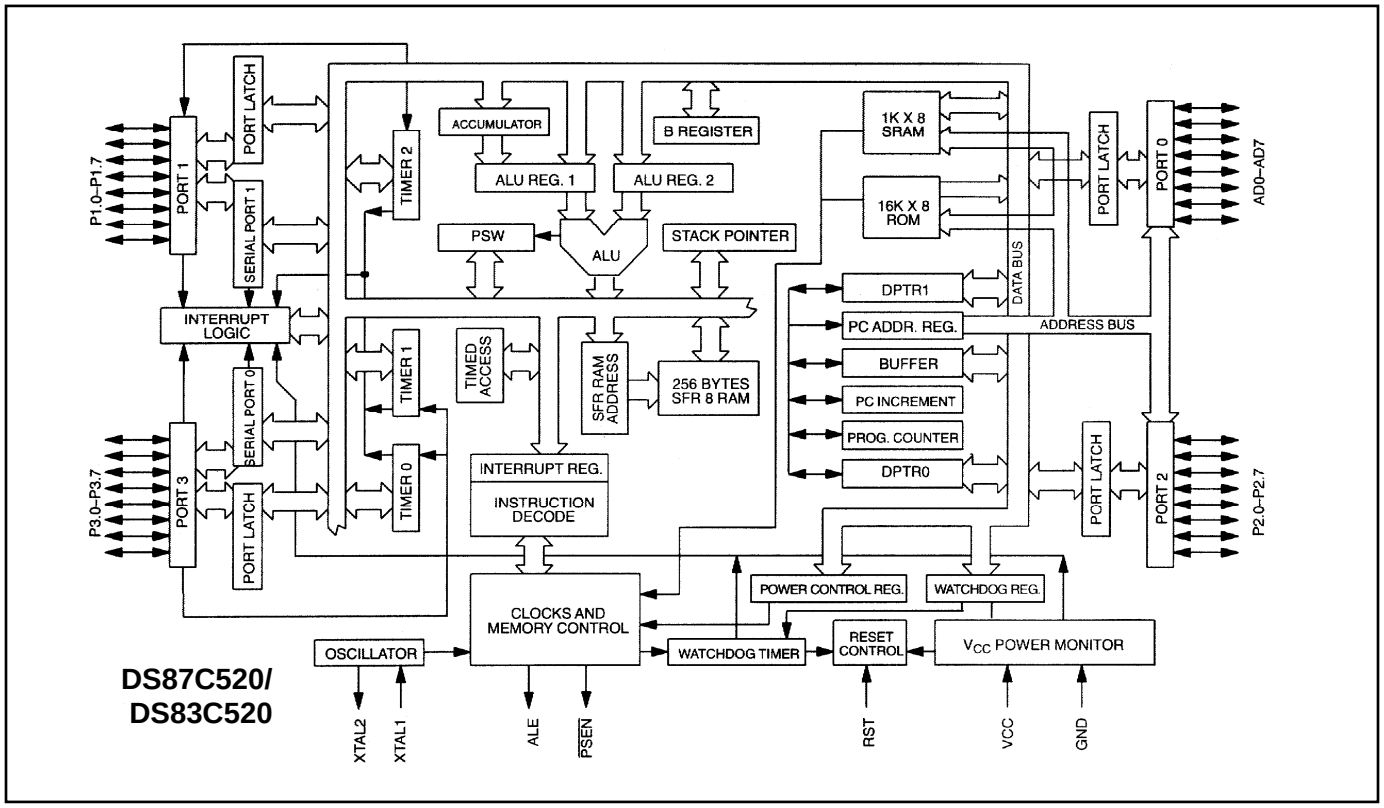
Besides greater speed, the microcontroller includes a second full hardware serial port, seven additional interrupts, programmable Watchdog Timer, Brownout Monitor, and Power-Fail Reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It also can adjust the speed of MOVX data memory access from two to nine machine cycles for flexibility in selecting external memory and peripherals.

A new Power Management Mode (PMM) is useful for portable applications. This feature allows software to select a lower speed clock as the main time base. While normal operation has a machine cycle rate of 4 clocks per cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. For example, at 12MHz, standard operation has a machine cycle rate of 3MHz. In Power Management Mode, software can select either 187.5kHz or 11.7kHz machine cycle rate. There is a corresponding reduction in power consumption when the processor runs slower.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

The DS83C520 is a factory mask ROM version of the DS87C520 designed for high-volume, cost-sensitive applications. It is identical in all respects to the DS87C520, except that the 16kB of EPROM is replaced by a user-supplied application program. All references to features of the DS87C520 will apply to the DS83C520, with the exception of EPROM-specific features where noted. Please contact your local Dallas Semiconductor sales representative for ordering information.

Figure 1. Block Diagram



PIN DESCRIPTION

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
40	44	38	V_{CC}	**Positive Supply Voltage.** +5V
20	1, 22, 23	16, 17, 39	GND	**Digital Circuit Ground**
9	10	4	RST	**Reset Input.** The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is not required for power-up, as the device provides this function internally.
18	20	14	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier.
19	21	15	XTAL1	
29	32	26	$\overline{\text{PSEN}}$	**Program Store-Enable Output.** This active-low signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ provides an active-low pulse and is driven high when external ROM is not being accessed.

PIN DESCRIPTION (continued)

PIN			NAME	FUNCTION
DIP	PLCC	TQFP		
21	24	18	P2.0 (A8)	**Port 2 (A8–15), I/O**. Port 2 is a bidirectional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
22	25	19	P2.1 (A9)	
23	26	20	P2.2 (A10)	
24	27	21	P2.3 (A11)	
25	28	22	P2.4 (A12)	
26	29	23	P2.5 (A13)	
27	30	24	P2.6 (A14)	
28	31	25	P2.7 (A15)	
10	11	5	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for External Interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the DS87C520/DS83C520 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below. **Port — Alternate — Mode** P3.0 — RXD0 — Serial Port 0 Input P3.1 — TXD0 — Serial Port 0 Output P3.2 — $\overline{INT0}$ — External Interrupt 0 P3.3 — $\overline{INT1}$ — External Interrupt 1 P3.4 — T0 — Timer 0 External Input P3.5 — T1 — Timer 1 External Input P3.6 — $\overline{WR}$ — External Data Memory Write Strobe P3.7 — $\overline{RD}$ — External Data Memory Read Strobe
11	13	7	P3.1	
12	14	8	P3.2	
13	15	9	P3.3	
14	16	10	P3.4	
15	17	11	P3.5	
16	18	12	P3.6	
17	19	13	P3.7	
31	35	29	$\overline{EA}$	**External Access Input, Active Low.** Connect to ground to force the DS87C520/DS83C520 to use an external ROM. The internal RAM is still accessible as determined by register settings. Connect $\overline{EA}$ to V_{CC} to use internal ROM.
—	12, 34	6, 28	N.C.	**Not Connected.** These pins should not be connected. They are reserved for use with future devices in this family.

Table 1. Special Function Register Locations

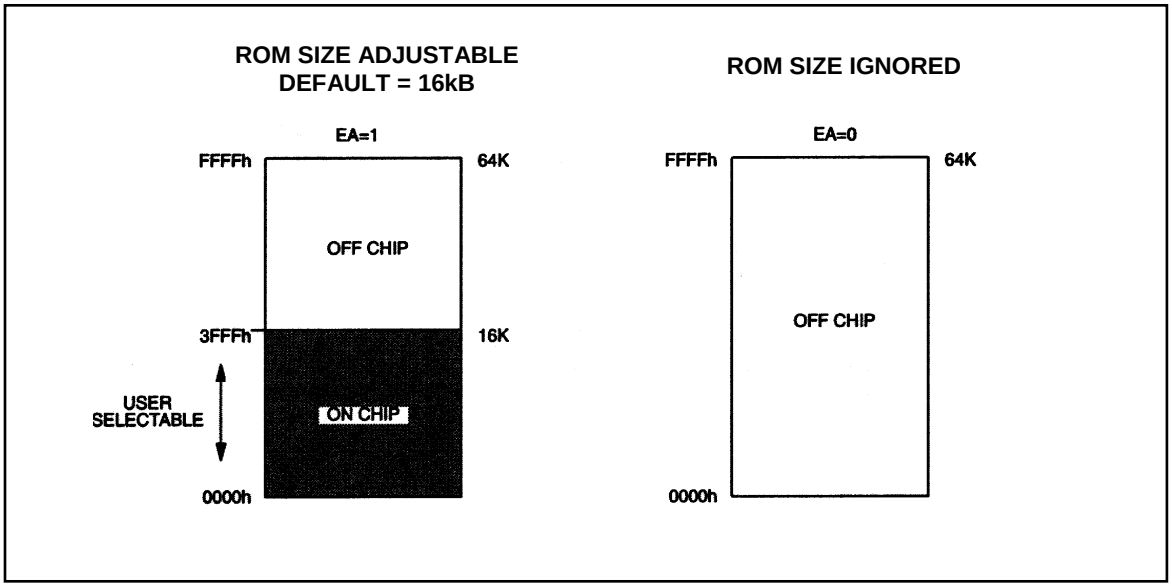
REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE**	**XT/$\overline{RG}$**	**RGMD**	**RGSL**	**BGS**	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**R1_1**	C0h
SBUF1	**SB7**	**SB6**	**SB5**	**SB4**	**SB3**	**SB2**	**SB1**	**SB0**	C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPTA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	C/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	—	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
EIP	—	—	—	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h

Note: *New functions are in bold.*

16kB internal program space. If software reconfigures the ROMSIZE register to 4kB (0000h–0FFFh) in the current state, the device will immediately jump to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4kB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the $\overline{EA}$ pin is a logic 0. $\overline{EA}$ overrides all bit settings. The $\overline{PSEN}$ signal goes active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

Figure 2. ROM Memory Map



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C520/DS83C520 contain on-chip data memory. They also contain the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

POWER MANAGEMENT

Along with the standard Idle and power down (Stop) modes of the standard 80C52, the DS87C520/DS83C520 provide a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C520/DS83C520 also feature several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C520/DS83C520 use four clocks per machine cycle. Thus the instruction cycle rate is Clock/4. At 33MHz crystal speed, the instruction cycle speed is 8.25MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources - discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 4 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slow and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 5.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle mode, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from Idle, and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)
11.0592	2.765	172.8	10.8
16	4.00	250.0	15.6
25	6.25	390.6	24.4
33	8.25	515.6	32.2

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)
11.0592	13.1	5.3	4.8
16	17.2	6.4	5.6
25	25.7	8.1	7.0
33	32.8	9.8	8.2

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C520/DS83C520 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal and ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h).

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Crystal/Ring Operation

The DS87C520/DS83C520 allow software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

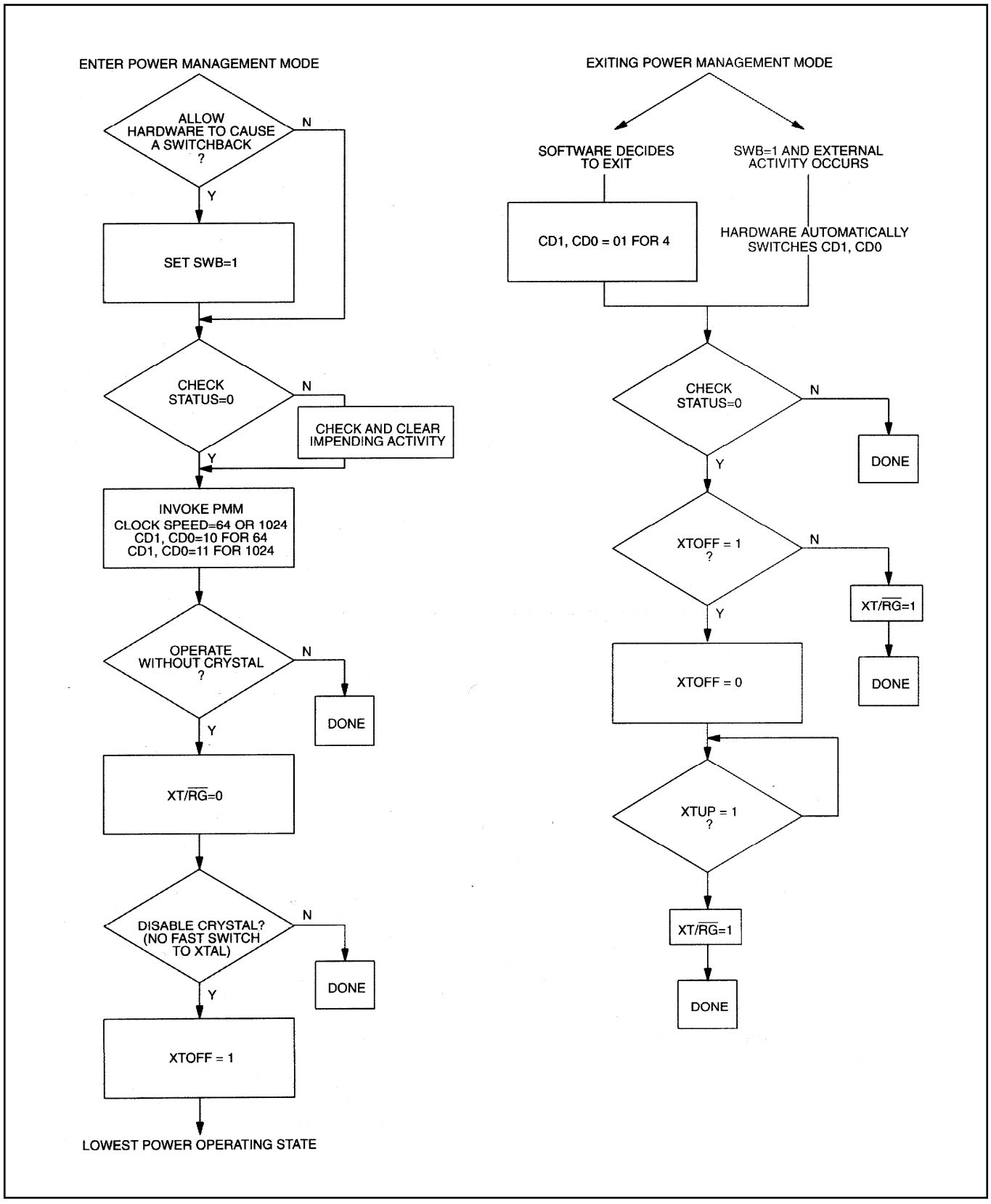
The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one-instruction cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to 0. At this time, the crystal oscillation will begin. The DS87C520/DS83C520 then provide a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to 1 before XTUP=1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystal-less PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

Figure 3 illustrates a typical decision set associated with PMM. Table 6 is a summary of the bits relating to PMM and its operation.

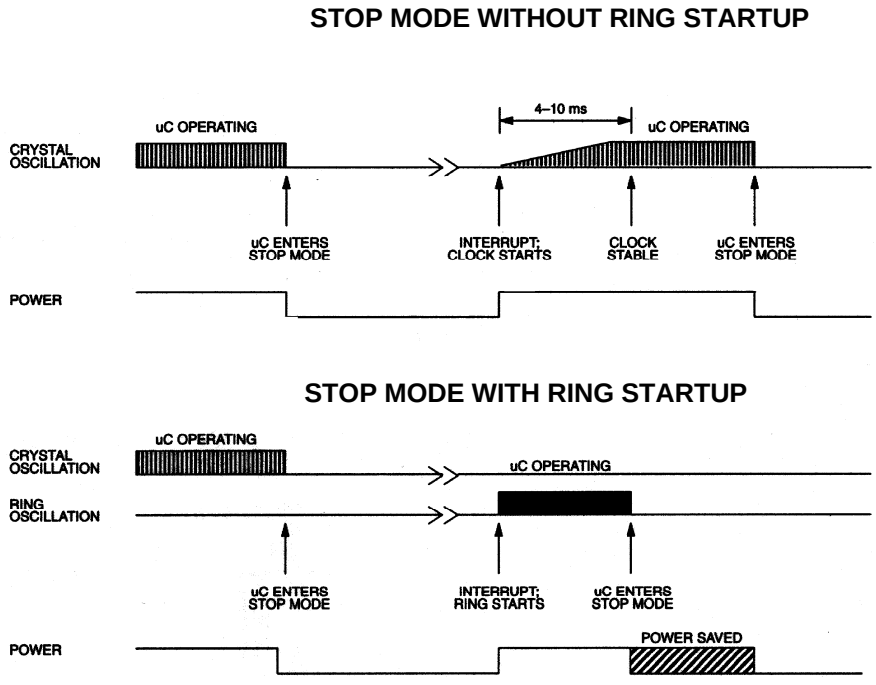
Figure 3. Invoking and Clearing PMM



how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL - Ring Select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD-Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

Figure 4. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The microcontroller allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static mode when performing on-chip memory access. The default state of ALEOFF = 0 so ALE toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C520/DS83C520 provide several of the most commonly needed peripheral functions in micro-computer-based systems. These new functions include a second serial port, power-fail reset, power-fail interrupt, and a programmable watchdog timer. These are described in the following paragraphs. More details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C520/DS83C520 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C520/DS83C520 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C520/DS83C520 architecture normally uses four clocks per machine cycle. However, in the area of timers and serial ports, the DS87C520/DS83C520 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON;8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the DS87C520/DS83C520 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C520/DS83C520 use 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C520/DS83C520 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

will set an interrupt flag. Regardless of whether the user enables this interrupt, there are then 512 clocks left until the reset flag is set. Software can enable the interrupt and reset individually. Note that the Watchdog is a free running timer and does not require an enable.

There are 5 control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source.

EWT (WDCON.1) is the enable for the Watchdog timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the timeout. Both of these bits are protected by Timed Access. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4). The Special Function Register map is shown above.

INTERRUPTS

The DS87C520/DS83C520 provide 13 interrupt sources with three priority levels. The Power-Fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

Table 8. Interrupt Sources and Priorities

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power-Fail Interrupt	33h	1	DALLAS
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from serial port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from serial port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Timeout Interrupt	63h	13	DALLAS

TIMED-ACCESS PROTECTION

It is useful to protect certain SFR bits from an accidental write operation. The Timed Access procedure stops an errant CPU from accidentally changing these bits. It requires that the following instructions precede a write of a protected bit.

```
MOV     0C7h,   #0Aah
MOV     0C7h,   #55h
```

Writing an AAh then a 55h to the Timed Access register (location C7h) opens a 3-cycle window for write access. The window allows software to modify a protected bit(s). If these instructions do not immediately precede the write operation, then the write will not take effect. The protected bits are:

EXIF.0	BGS	Bandgap Select
WDCON.6	POR	Power-On Reset flag
WDCON.1	EWT	Enable Watchdog Reset
WDCON.0	RWT	Restart Watchdog
WDCON.3	WDIF	Watchdog Interrupt Flag
ROMSIZE.2	RMS2	ROM Size Select 2
ROMSIZE.1	RMS1	ROM Size Select 1
ROMSIZE.0	RMS0	ROM Size Select 0

EPROM PROGRAMMING

The DS87C520 follows standards for a 16kB EPROM version in the 8051 family. It is available in a UV-erasable, ceramic-windowed package and in plastic packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options. ROM-specific features are described later in this data sheet.

Most commercially available device programmers will directly support Dallas Semiconductor microcontrollers. If your programmer does not, please contact the manufacturer for updated software.

PROGRAMMING PROCEDURE

The DS87C520 should run from a clock speed between 4MHz and 6MHz when being programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 9. The diagram in Table 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the *Electrical Specifications* section.

Program the DS87C520 as follows:

1) Apply the address value,
2) Apply the data value,
3) Select the programming option from Table 9 using the control signals,
4) Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM,
5) Pulse the $\overline{PROG}$ signal five times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits,
6) Repeat as many times as necessary.

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 9. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

OTHER EPROM OPTIONS

The DS87C520 has user selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

Program the EPROM selectable options as shown in Table 9. The Option Register sets or reads these selections. The bits in the Option Control Register have the following function:

Bits 7 to 4	Reserved, program to a 1.
Bit 3	Watchdog POR default. Set = 1; watchdog reset function is disabled on power-up. Set = 0; watchdog reset function is enabled automatically.
Bits 2 to 0	Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	20h	Model
60h	01h	Extension

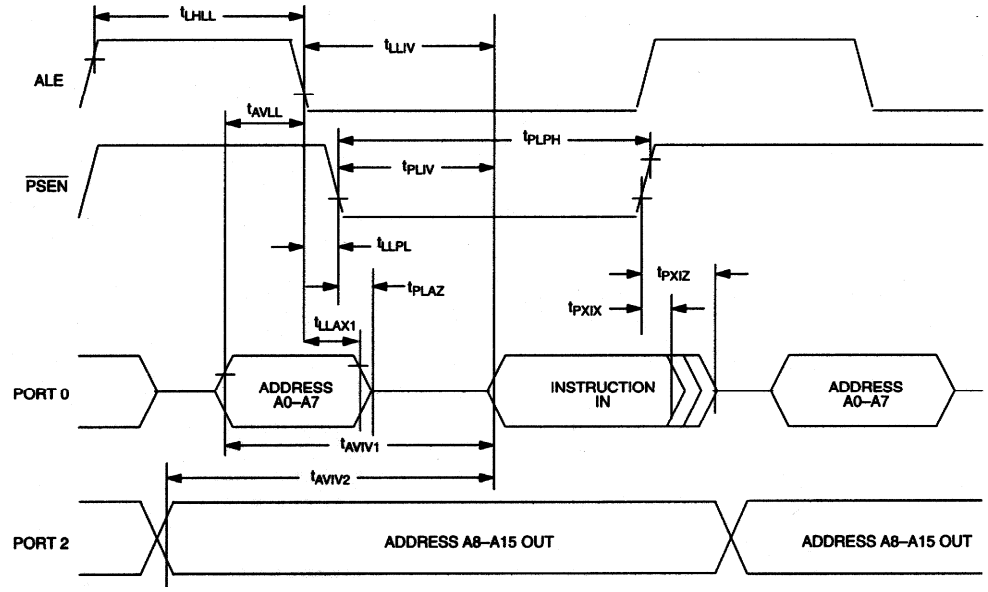
AC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	33 MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	40		$1.5t_{CLCL}$-5		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	10		$0.5t_{CLCL}$-5		ns
Address Hold after ALE Low		t_{LLAX1}	(Note 2)		(Note 2)		ns
ALE Low to Valid Instruction In		t_{LLIV}		43		$2.5t_{CLCL}$-33	ns
ALE Low to $\overline{\text{PSEN}}$ Low		t_{LLPL}	4		$0.5t_{CLCL}$-11		ns
$\overline{\text{PSEN}}$ Pulse Width		t_{PLPH}	55		$2t_{CLCL}$-5		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In		t_{PLIV}		37		$2t_{CLCL}$-24	ns
Input Instruction Hold after $\overline{\text{PSEN}}$		t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$		t_{PXIZ}		26		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		59		$3t_{CLCL}$-32	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		68		$3.5t_{CLCL}$-38	ns
$\overline{\text{PSEN}}$ Low to Address Float		t_{PLAZ}		(Note 2)		(Note 2)	ns

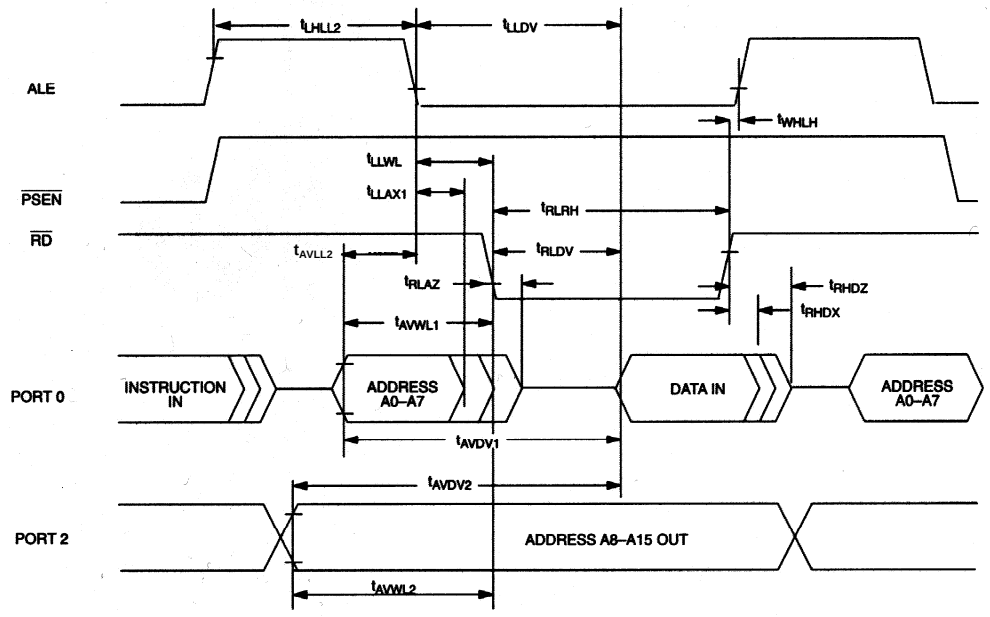
Note 1: All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics are not 100% tested, but are characterized and guaranteed by design. All signals characterized with load capacitance of 80pF except Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns may cause contention. This will not damage the parts, but will cause an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

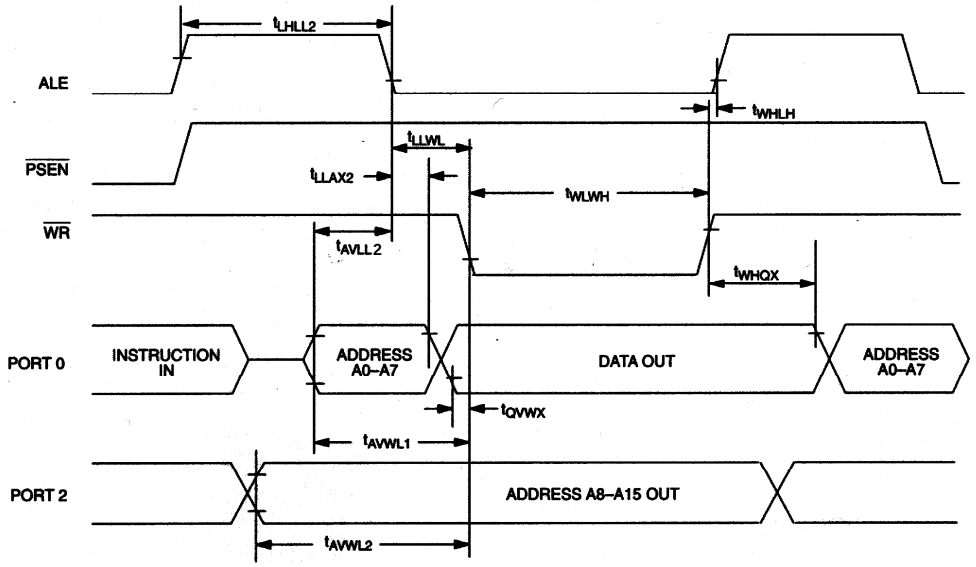
EXTERNAL PROGRAM MEMORY READ CYCLE



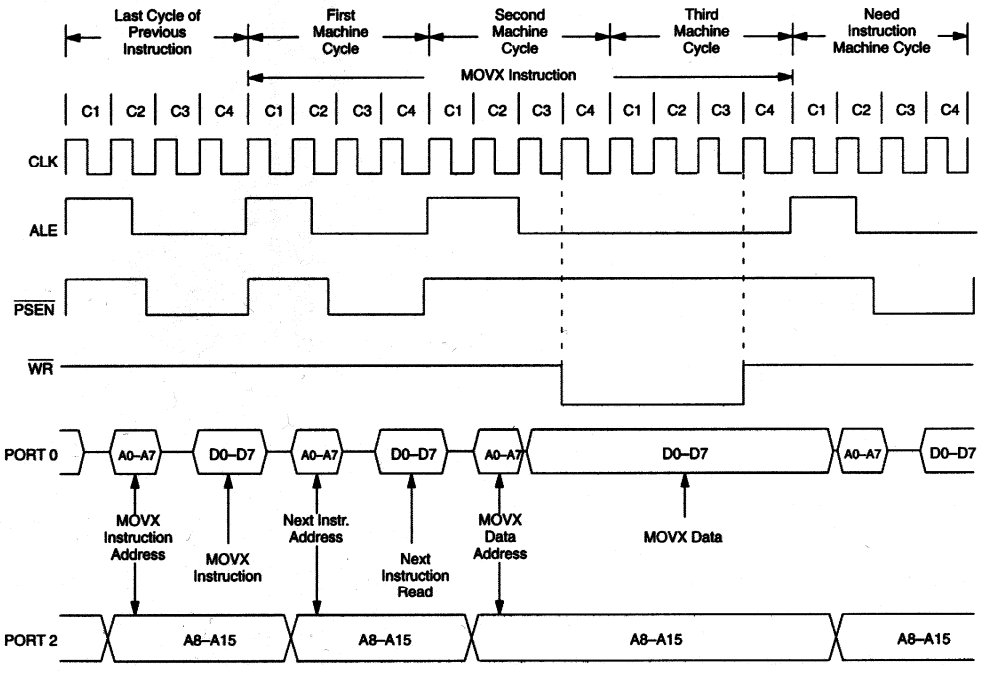
EXTERNAL DATA MEMORY READ CYCLE



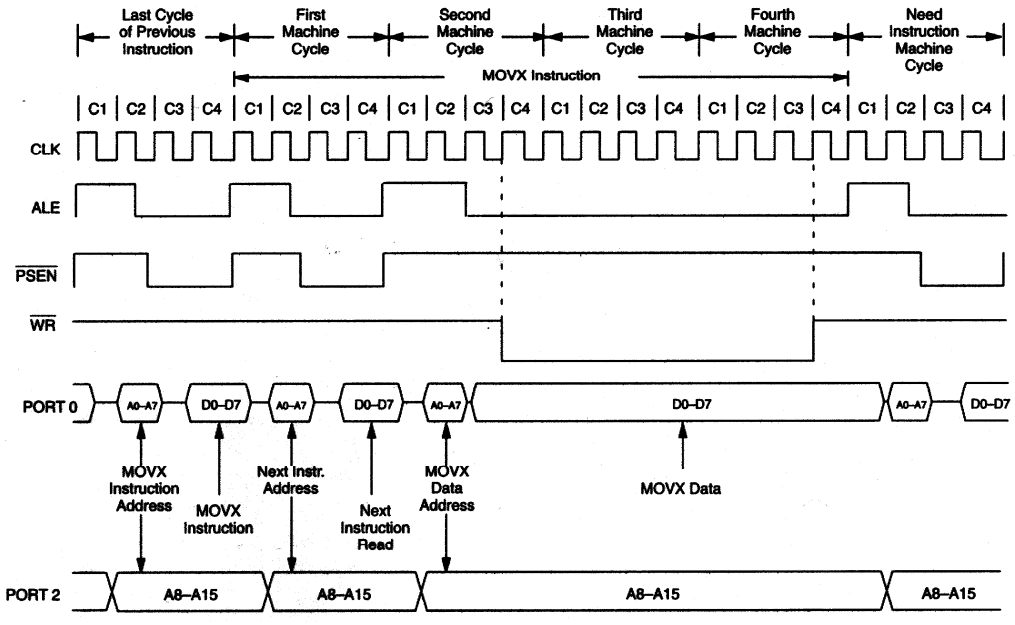
EXTERNAL DATA MEMORY WRITE CYCLE



DATA MEMORY WRITE WITH STRETCH = 1



DATA MEMORY WRITE WITH STRETCH = 2



FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

EXTERNAL CLOCK DRIVE