Analog Devices Inc./Maxim Integrated - DS87C520-WCL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	EPROM, UV
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-CDIP (0.600", 15.24mm) Window
Supplier Device Package	40-CDIP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c520-wcl

DESCRIPTION

The DS87C520/DS83C520 EPROM/ROM high-speed microcontrollers are fast 8051-compatible microcontrollers. They feature a redesigned processor core without wasted clock and memory cycles. As a result, the devices execute every 8051 instruction between 1.5 and 3 times faster than the original for the same crystal speed. Typical applications will see a speed improvement of 2.5 times using the same code and the same crystal. The DS87C520/DS83C520 offer a maximum crystal speed of 33MHz, resulting in apparent execution speeds of 82.5MHz (approximately 2.5X).

The DS87C520/DS83C520 are pin compatible with all three packages of the standard 8051, and include standard resources such as three timer/counters, serial port, and four 8-bit I/O ports. They feature 16kB of EPROM or mask ROM with an extra 1kB of data RAM. Both OTP and windowed packages are available.

Besides greater speed, the microcontroller includes a second full hardware serial port, seven additional interrupts, programmable Watchdog Timer, Brownout Monitor, and Power-Fail Reset. The device also provides dual data pointers (DPTRs) to speed block data memory moves. It also can adjust the speed of MOVX data memory access from two to nine machine cycles for flexibility in selecting external memory and peripherals.

A new Power Management Mode (PMM) is useful for portable applications. This feature allows software to select a lower speed clock as the main time base. While normal operation has a machine cycle rate of 4 clocks per cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. For example, at 12MHz, standard operation has a machine cycle rate of 3MHz. In Power Management Mode, software can select either 187.5kHz or 11.7kHz machine cycle rate. There is a corresponding reduction in power consumption when the processor runs slower.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

The DS83C520 is a factory mask ROM version of the DS87C520 designed for high-volume, cost-sensitive applications. It is identical in all respects to the DS87C520, except that the 16kB of EPROM is replaced by a user-supplied application program. All references to features of the DS87C520 will apply to the DS83C520, with the exception of EPROM-specific features where noted. Please contact your local Dallas Semiconductor sales representative for ordering information.

COMPATIBILITY

The DS87C520/DS83C520 are fully static CMOS 8051-compatible microcontrollers designed for high performance. In most cases, the DS87C520/DS83C520 can drop into an existing socket for the 8xc51 family to improve the operation significantly. While remaining familiar to 8051 family users, the devices have many new features. In general, software written for existing 8051-based systems works without modification on the DS87C520/DS83C520. The exception is critical timing since the high-speed microcontrollers performs instructions much faster than the original for any given crystal selection. The DS87C520/DS83C520 run the standard 8051 family instruction set and are pin compatible with DIP, PLCC, or TQFP packages.

The DS87C520/DS83C520 provide three 16-bit timer/counters, full-duplex serial port (2), 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12-clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new four clocks per cycle if desired. The PCA is not supported.

The DS87C520/DS83C520 provide several new hardware features implemented by new special function registers. A summary of these SFRs is provided below.

PERFORMANCE OVERVIEW

The DS87C520/DS83C520 feature a high-speed 8051-compatible core. Higher speed comes not just from increasing the clock frequency but also from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C520/DS83C520, the same machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C520/DS83C520 will see the full 3-to-1 speed improvement. Some instructions will get between 1.5 and 2.4 to 1 improvement. All instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual instructions used. Speed-sensitive applications would make the most use of instructions that are three times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any code. These architecture improvements produce a peak instruction cycle in 121ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions perform the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the *High-Speed Microcontroller User's Guide*. However, counter/timers default to run at the older 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C520/DS83C520 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using 2 bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

Table 2. Data Memory Access Control

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h–FFFFh	External data memory (*default condition)*
0	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFFh	External data memory
1	0	Reserved	Reserved
1	1	0000h–03FFh	Internal SRAM data memory
		0400h–FFFBh	Reserved—no external access
		FFFCh	Read access to the status of lock bits
		FFFDh–FFFFh	Reserved—no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2–0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

Note: After internal MOVX SRAM has been initialized, changing the DME0/1 bits has no effect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C520/DS83C520 allow software to adjust the speed of off-chip data memory access. The microcontrollers can perform the MOVX in as few as two instruction cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C520/DS83C520 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal and ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h).

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Switchback

To return to a 4-clock rate from PMM, software can simply select the CD1 and CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C520/DS83C520 provide several hardware alternatives for automatic Switchback. If Switchback is enabled, then the device will automatically return to a 4-clock per cycle speed when an interrupt occurs from an enabled, valid external interrupt source. A Switchback will also occur when a UART detects the beginning of a serial start bit if the serial receiver is enabled (REN = 1). Note the beginning of a start bit does not generate an interrupt; this occurs on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception. A switchback will also occur when a byte is written to SBUF0 or SBUF1 for transmission.

Switchback is enabled by setting the SWB bit (PMR.5) to a 1 in software. For an external interrupt, Switchback will occur only if the interrupt source could really generate the interrupt. For example, if $\overline{\text{INT0}}$ is enabled but has a low priority setting, then Switchback will not occur on $\overline{\text{INT0}}$ if the CPU is servicing a high priority interrupt.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C520/DS83C520 support three levels of interrupt priority. These levels are Power-fail, High, and Low. Bits STATUS.7-5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS. 7) is a 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port 0 Receive Activity (SPRA0;STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port 0 Transmit Activity (SPTA0; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 and STATUS.3 provide the same information for Serial Port 1, respectively. These bits should be interrogated before entering PMM1 or PMM2 to ensure that no serial port operations are in progress. Changing the clock divisor rate during a serial transmission or reception will corrupt the operation.

Crystal/Ring Operation

The DS87C520/DS83C520 allow software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one-instruction cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to 0. At this time, the crystal oscillation will begin. The DS87C520/DS83C520 then provide a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to a 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to 1 before XTUP=1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

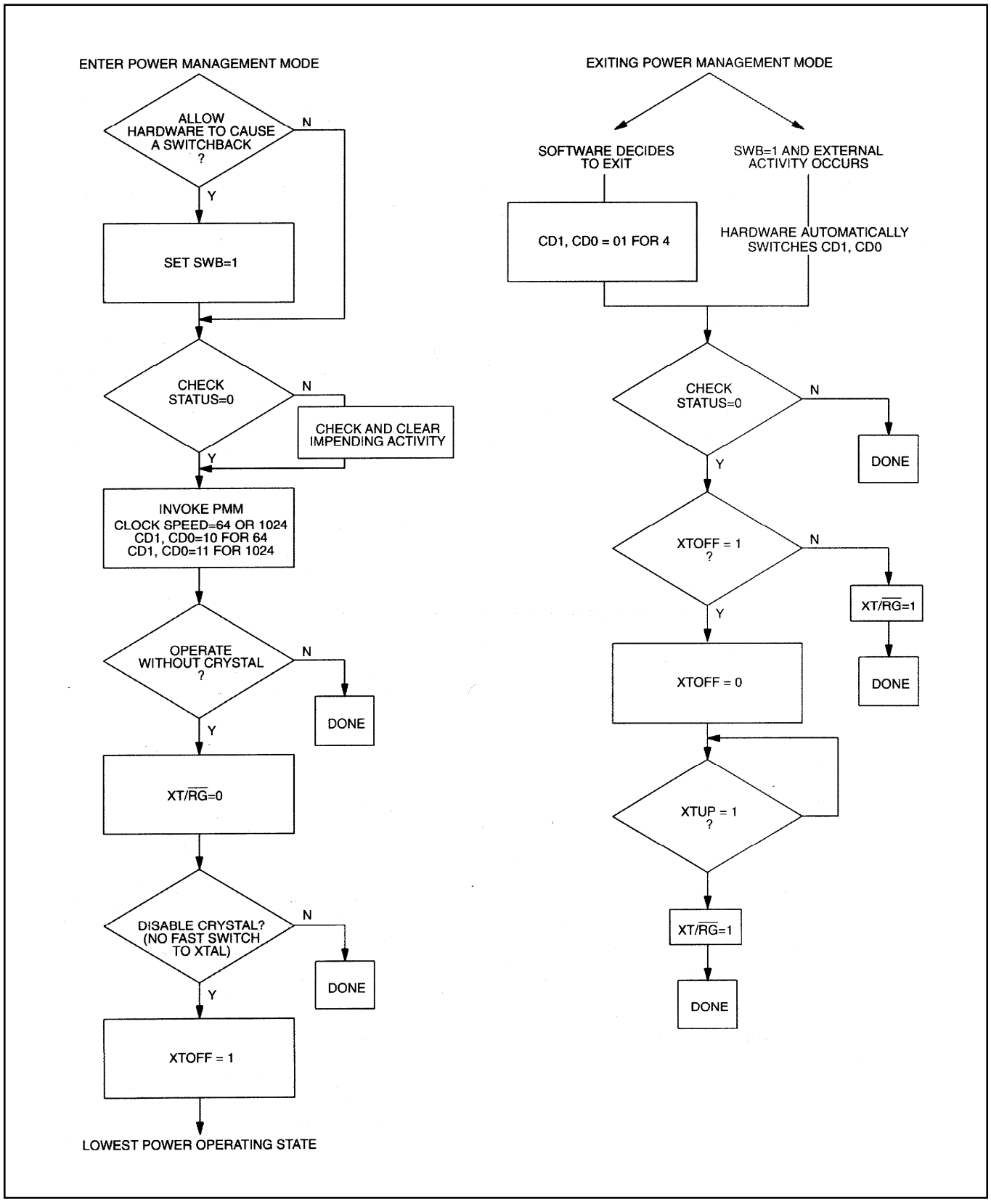
Switchback has no effect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystal-less PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

Figure 3 illustrates a typical decision set associated with PMM. Table 6 is a summary of the bits relating to PMM and its operation.

Table 6. PMM Control and Status Bit Summary

BIT	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{RG}$	EXIF.3	Control. XT/$\overline{RG}$ = 1, runs from crystal or external clock; XT/$\overline{RG}$ = 0, runs from internal ring oscillator.	X	0 to 1 only when XTUP = 1 and XTOFF = 0
RGMD	EXIF.2	Status. RGMD = 1, CPU clock = ring; RGMD = 0, CPU clock = crystal.	0	None
CD1, CD0	PMR.7, PMR.6	Control. CD1, 0 = 01, 4 clocks; CS1, 0 = 10, PMM1; CD1, 0 = 11, PMM2.	0, 1	Write CD1, 0 = 10 or 11 only from CD1, 0 = 01
SWB	PMR.5	Control. SWB = 1, hardware invokes switchback to 4 clocks, SWB = 0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{RG}$ = 0
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

Figure 3. Invoking and Clearing PMM



POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning Power-Fail Interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to a logic 1 will enable the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it.

WATCHDOG TIMER

To prevent software from losing control, the DS87C520/DS83C520 include a programmable Watchdog Timer. The Watchdog is a free-running timer that sets a flag if allowed to reach a preselected timeout. It can be (re)started by software.

A typical application is to select the flag as a reset source. When the Watchdog times out, it sets its flag, which generates reset. Software must restart the timer before it reaches its timeout or the processor is reset.

Software can select one of four timeout values. Then, it restarts the timer and enables the reset function. After enabling the reset function, software must then restart the timer before its expiration or hardware will reset the CPU. Both the Watchdog Reset Enable and the Watchdog Restart control bits are protected by a “Timed Access” circuit. This prevents errant software from accidentally clearing the Watchdog. Timeout values are precise since they are a function of the crystal frequency as shown in Table 7. For reference, the time periods at 33MHz also are shown.

The Watchdog also provides a useful option for systems that do not require a reset circuit. It will set an interrupt flag 512 clocks before setting the reset flag. Software can optionally enable this interrupt source. The interrupt is independent of the reset. A common use of the interrupt is during debug, to show developers where the Watchdog times out. This indicates where the Watchdog must be restarted by software. The interrupt also can serve as a convenient time-base generator or can wake-up the processor from power saving modes.

The Watchdog function is controlled by the Clock Control (CKCON-8Eh), Watchdog Control (WDCON-D8h), and Extended Interrupt Enable (EIE-E8h) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively and they select the Watchdog timeout period as shown in Table 7.

Table 7. Watchdog Timeout Values

WD1	WD2	INTERRUPT TIMEOUT	TIME (33 MHz)	RESET TIMEOUT	TIME (33 MHz)
0	0	2^{17} clocks	3.9718 ms	2^{17} + 512 clocks	3.9874 ms
0	1	2^{20} clocks	31.77 ms	2^{20} + 512 clocks	31.79 ms
1	0	2^{23} clocks	254.20 ms	2^{23} + 512 clocks	254.21 ms
1	1	2^{26} clocks	2033.60 ms	2^{26} + 512 clocks	2033.62 ms

As shown in Table 7, the Watchdog Timer uses the crystal frequency as a time base. A user selects one of four counter values to determine the timeout. These clock counter lengths are 2^{17} = 131,072 clocks; 2^{20} = 1,048,576; 2^{23} = 8,388,608 clocks; and 2^{26} = 67,108,864 clocks. The times shown in Table 7 are with a 33MHz crystal frequency. Once the counter chain has completed a full interrupt count, hardware

will set an interrupt flag. Regardless of whether the user enables this interrupt, there are then 512 clocks left until the reset flag is set. Software can enable the interrupt and reset individually. Note that the Watchdog is a free running timer and does not require an enable.

There are 5 control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source.

EWT (WDCON.1) is the enable for the Watchdog timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the timeout. Both of these bits are protected by Timed Access. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4). The Special Function Register map is shown above.

INTERRUPTS

The DS87C520/DS83C520 provide 13 interrupt sources with three priority levels. The Power-Fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

Table 8. Interrupt Sources and Priorities

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power-Fail Interrupt	33h	1	DALLAS
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from serial port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from serial port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Timeout Interrupt	63h	13	DALLAS

DS83C520 ROM VERIFICATION

The DS83C520 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 5, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C520 SIGNATURE

The Signature bytes identify the DS83C520 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	21h	Model
60h	01h	Extension

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transition Current from 1 to 0 Ports 1, 2, 3 at 2V	I_{TL}			-800	µA	9
Input Leakage Port 0, and $\overline{EA}$ pins, I/O Mode	I_L	-10		+10	µA	11
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	10
RST Pulldown Resistance	R_{RST}	50		200	kΩ	

Note 1: All parameters apply to both commercial and industrial temperature operation, unless otherwise noted.

Note 2: All voltages are referenced to ground.

Note 3: Active current measured with 33MHz clock source on XTAL1, V_{CC} = RST = 5.5V, other pins disconnected.

Note 4: Idle mode current measured with 33MHz clock source on XTAL1, V_{CC} = 5.5V, RST at ground, other pins disconnected.

Note 5: Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.

Note 6: When addressing external memory. This specification only applies to the first clock cycle following the transition.

Note 7: RST = V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tri-stated in reset and when at a logic high state during I/O mode.

Note 8: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

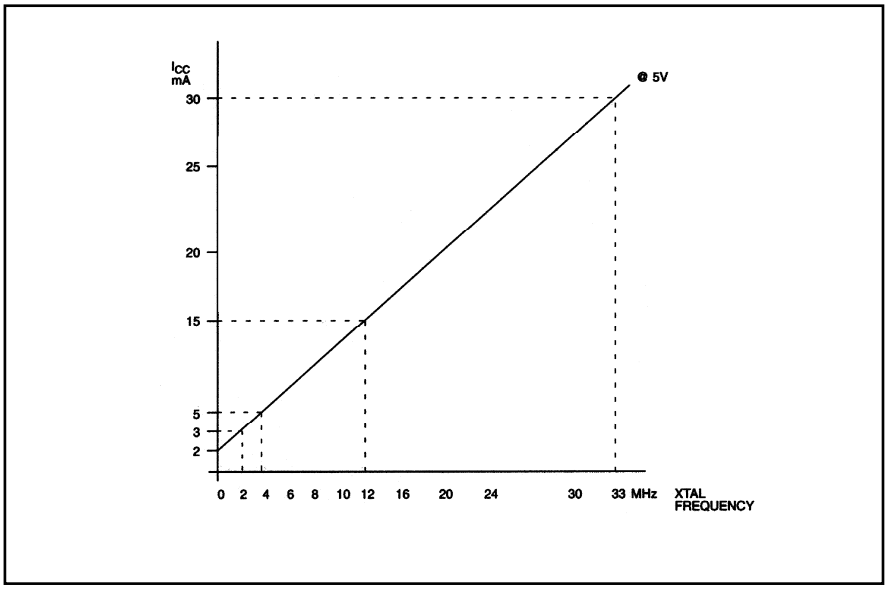
Note 9: Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.

Note 10: 0.45 < V_{IN} < V_{CC}. Not a high-impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

Note 11: 0.45 < V_{IN} < V_{CC}. RST = V_{CC}. This condition mimics operation of pins in I/O mode.

Note 12: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

TYPICAL I_{CC} vs. FREQUENCY



MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$1.5t_{CLCL}$-5		ns	t_{MCS}=0
		$2t_{CLCL}$-5			t_{MCS}>0
Port 0 Address Valid to ALE Low	t_{AVLL2}	$0.5t_{CLCL}$-5		ns	t_{MCS}=0
		t_{CLCL}-5			t_{MCS}>0
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$-10		ns	t_{MCS}=0
		t_{CLCL}-7			t_{MCS}>0
$\overline{RD}$ Pulse Width	t_{RLRH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2t_{CLCL}$-5		ns	t_{MCS}=0
		t_{MCS}-10			t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2t_{CLCL}$-22	ns	t_{MCS}=0
			t_{MCS}-24		t_{MCS}>0
Data Hold After Read	t_{RHDX}	0		ns	—
Data Float after Read	t_{RHDZ}		t_{CLCL}-5	ns	t_{MCS}=0
			$2t_{CLCL}$-5		t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$-31	ns	t_{MCS}=0
			$t_{MCS}+t_{CLCL}$-26		t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3t_{CLCL}$-29	ns	t_{MCS}=0
			$t_{MCS}+2t_{CLCL}$-29		t_{MCS}>0
Port 2 Address to Valid Data In	t_{AVDV2}		$3.5t_{CLCL}$-37	ns	t_{MCS}=0
			$t_{MCS}+2.5t_{CLCL}$-37		t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$-10	$0.5t_{CLCL}$+5	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	t_{CLCL}-9		ns	t_{MCS}=0
		$2t_{CLCL}$-7			t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$-17		ns	t_{MCS}=0
		$2.5t_{CLCL}$-16			t_{MCS}>0
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-6		ns	—
Data Hold after Write	t_{WHQX}	t_{CLCL}-5		ns	t_{MCS}=0
		$2t_{CLCL}$-6			t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		(Note 2)	ns	—
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	-4	10	ns	t_{MCS}=0
		t_{CLCL}-5	t_{CLCL}+5		t_{MCS}>0

Note 1: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

MOVX CHARACTERISTICS (continued)

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

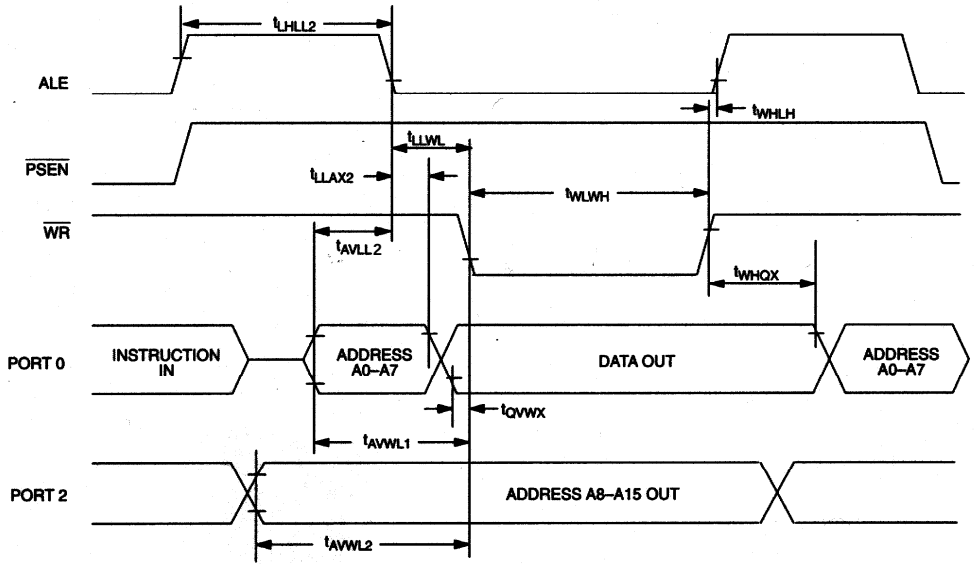
EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCL}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

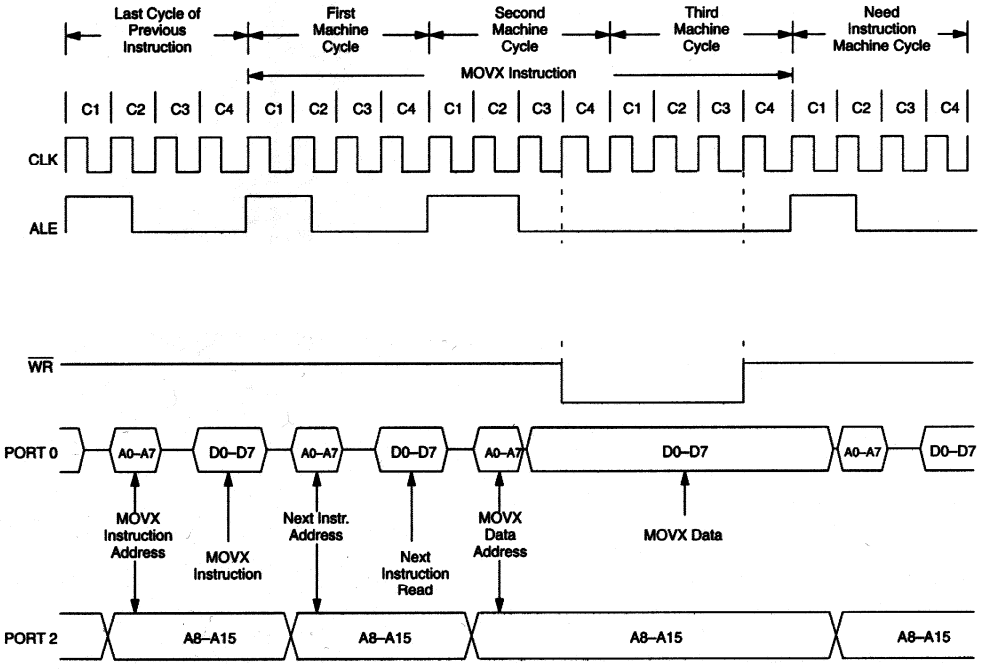
SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0, 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0, 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0, 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0, 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0, 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		

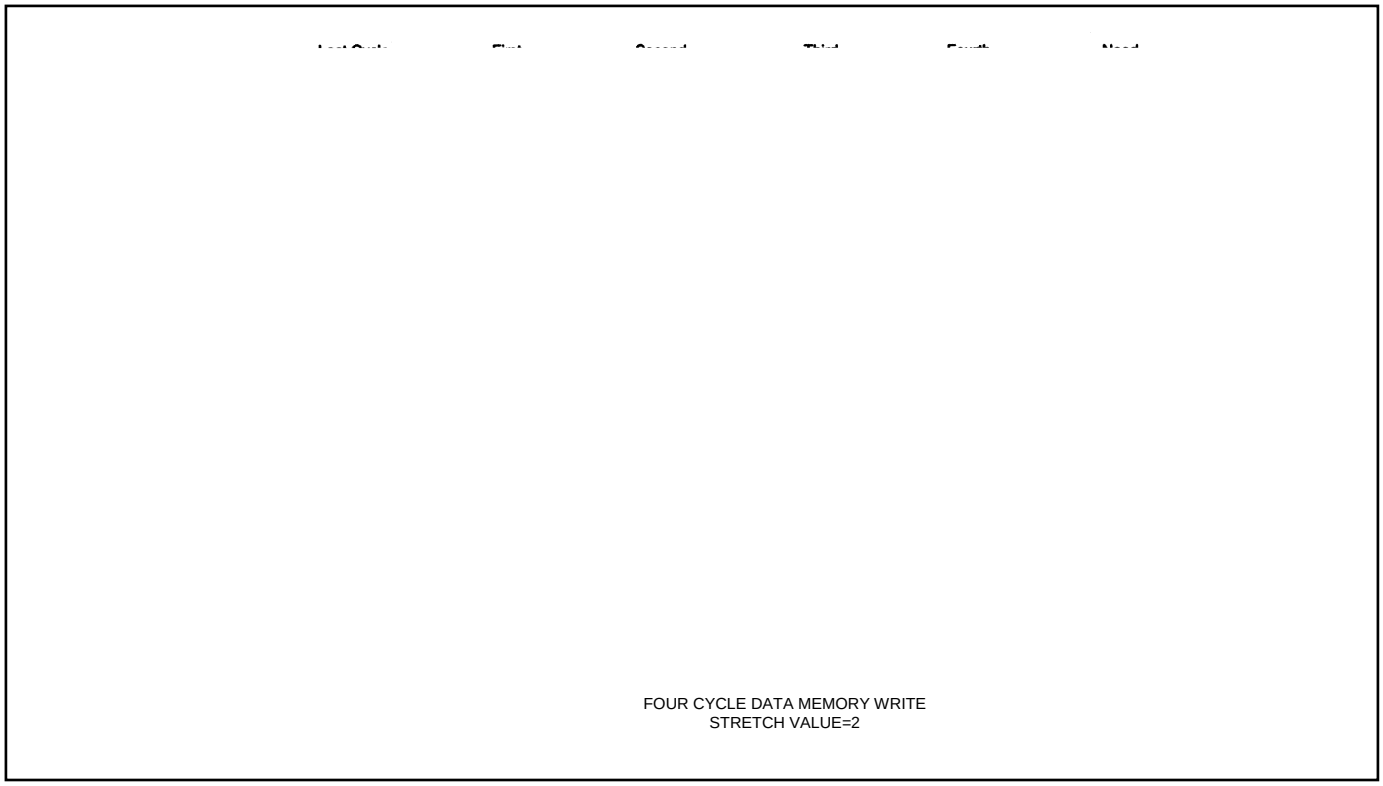
EXTERNAL DATA MEMORY WRITE CYCLE



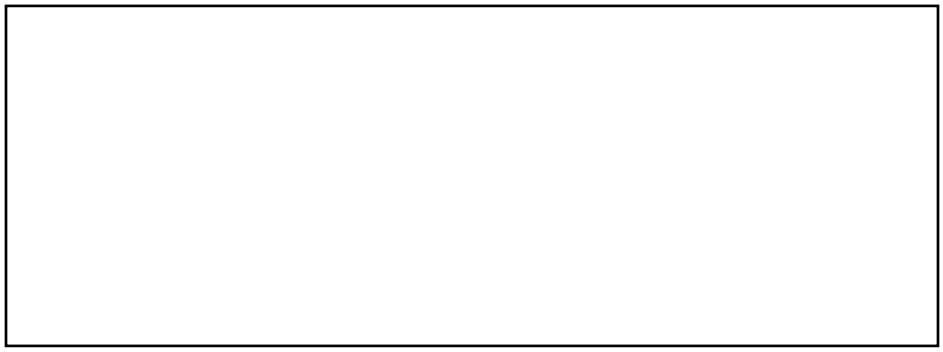
DATA MEMORY WRITE WITH STRETCH = 1



DATA MEMORY WRITE WITH STRETCH = 2



EXTERNAL CLOCK DRIVE



PACKAGE INFORMATION

For the latest package outline information, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFP	C44+3	**21-0293**
40 CDIP	J40-5	**21-0384**
40 PDIP	P40+4	**21-0044**
44 PLCC	Q44+9	**21-0049**

DATA SHEET REVISION SUMMARY

REVISION	DESCRIPTION
110195	Preliminary release.
022097	1) Update ALE pin description. 2) Add note pertaining to erasure window. 3) Add note pertaining to internal MOVX SRAM. 4) Change Note 10 from RST = 5.5V to RST = V_{CC}. 5) Change serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}.
070698	1) Update PMM operating current estimates 2) Added note to clarify I_{IL} specification. 3) Added note to prevent accidental corruption of Watchdog Timer count while changing counter length. 4) Changed minimum oscillator frequency to 1MHz when using external crystal. 5) Changed RST pulldown resistance from 170kΩ to 200kΩ maximum. 6) Corrected "Data memory write with stretch" diagrams to show falling edge of ALE coincident with rising edge of C3 clock.
070300	1) Corrected P0 pinout description for TQFP package. 2) Clarified point at which reset delay begins.
040104	1) Removed "Preliminary" status. 2) Soldering temperature parameter now references JEDEC specification. 3) Added note to absolute maximums clarifying voltages referenced to ground. 4) Updated I_{CC}, I_{IDLE}, I_{STOP}, I_{SPBG}, I_{IL}, and I_{TL} to incorporate errata conditions. 5) Added note clarifying DC electrical test conditions. 6) Added note clarifying V_{OH3} specification applies to first clock cycle following the transition. 7) Updated AC and MOVX electrical characteristics with final characterization values. Added t_{AVLL2} specification and corrected MOVX timing diagrams to show t_{AVLL2} instead of t_{AVLL}.
070505	1) Added Pb-free/RoHS-compliant part numbers to Ordering Information table. 2) Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.
091605	1) In DC Electrical Characteristics table, added separate specification for DS83C520 V_{PFW}. 2) Changed V_{RST} max to from 4.25V to 4.275V for DS83C520 value.
022207	1) (Page 30) In the Absolute Maximum Ratings table, changed the operating range from 0°C to +70°C to -40°C to +85°C (correction for typographical error; this does not reflect a change in the device or device testing). 2) (Page 33) In the MOVX Characteristics table, added Note 2 and changed t_{RLAZ} max from Note 1 to Note 2.

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