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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

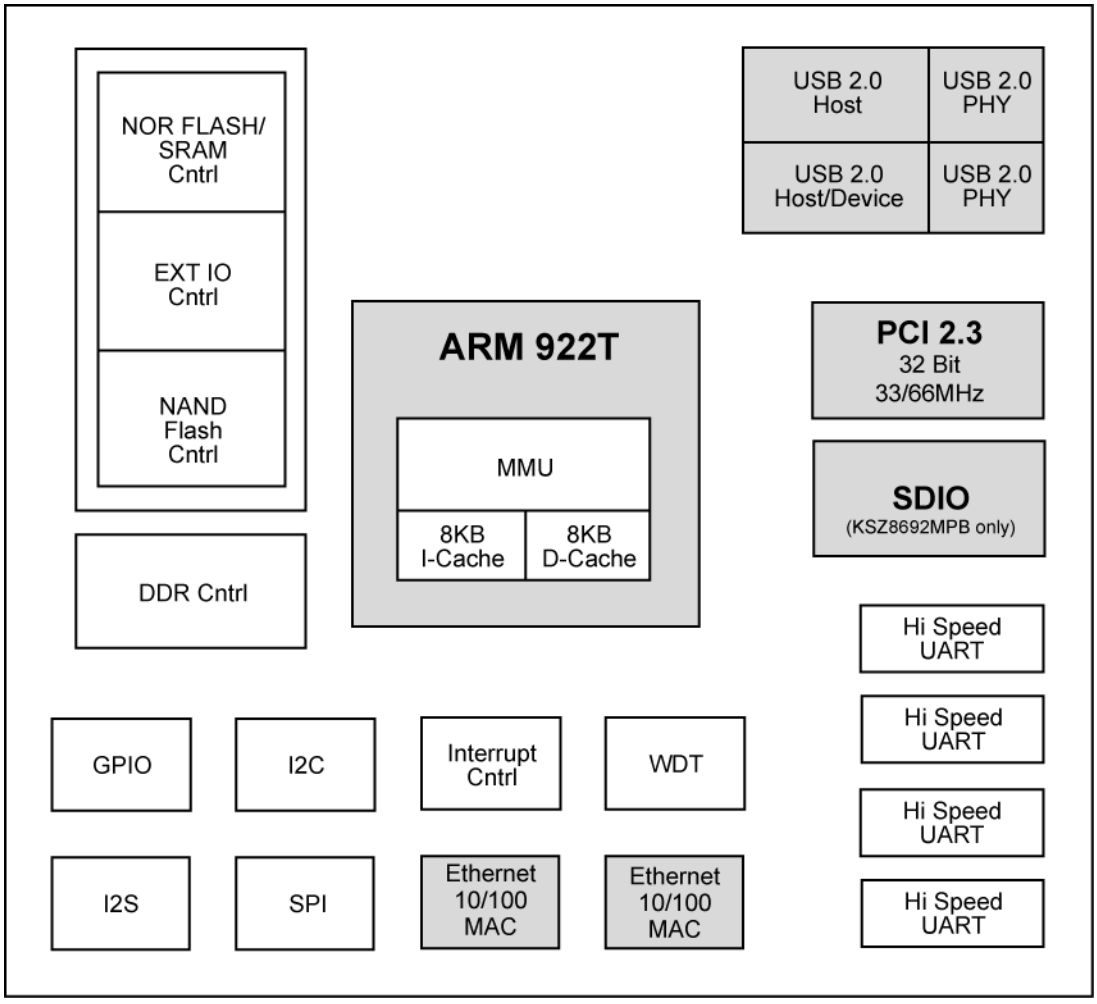
Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Networking and Communications
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	KSZ
RAM Size	-
Interface	EBI/EMI, Ethernet, I²C, I²S,PCI, SPI, UART/USART, USB
Number of I/O	20
Voltage - Supply	1.235V ~ 1.365V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	400-BGA
Supplier Device Package	400-PBGA (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ksz8692xpb

Block Diagram



Note: SDIO block for KSZ8692MPB only.

Figure 1. KSZ8692MPB/XPB Block Diagram

Applications

- Enhanced residential gateways
- High-end printer servers
- USB device servers
- IP-based multimedia systems
- Voice-over-Internet Protocol (VoIP) systems
- Set-top box
- Industrial control
- Wireless Access Points or Mesh Nodes

Ordering Information

Part Number	Temp. Range	Package	Lead Finish
KSZ8692MPB	0°C to 70°C	400-Pin PBGA	Pb-Free
KSZ8692MPBI[1]	-40°C to 85°C	400-Pin PBGA	Pb-Free
KSZ8692XPB[2]	0°C to 70°C	400-Pin PBGA	Pb-Free

Notes:

1. Industrial version of KSZ8692MPB.
2. Support for one PCI Master. No SDIO.

Revision History

Revision	Date	Summary of Changes
1.0	10/14/08	Initial Release
2.0	3/10/09	Power Sequencing, Added A1 (PMEN) to pin list, 1.3V Supply for Core, Power Consumption table
3.0	8/10/09	DDR Data Width Changed to 16-bit
4.0	01/28/10	DDR Data Width Changed to 32-bit

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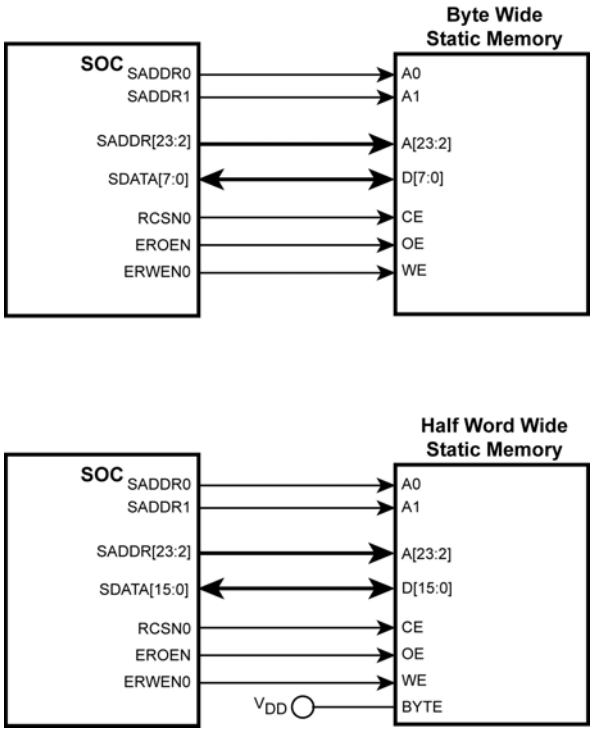

Figure 4. Static Memory Interface Examples

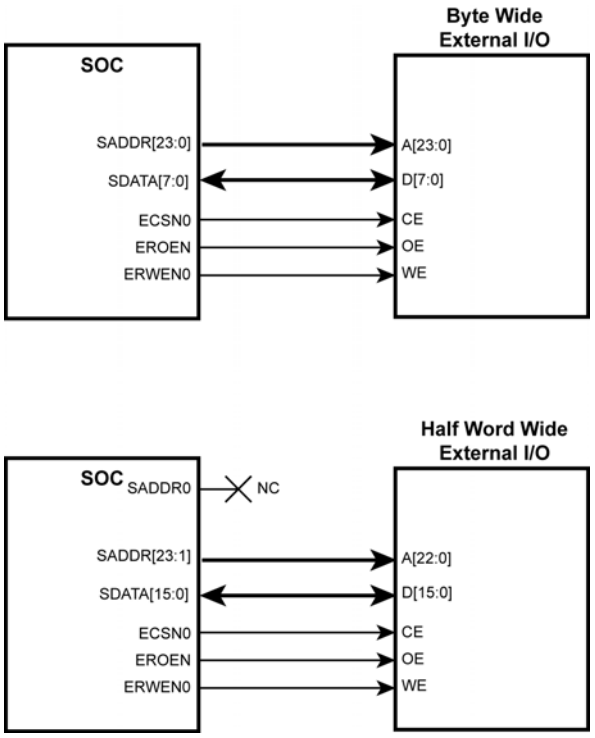

Figure 5. External I/O Interface Examples

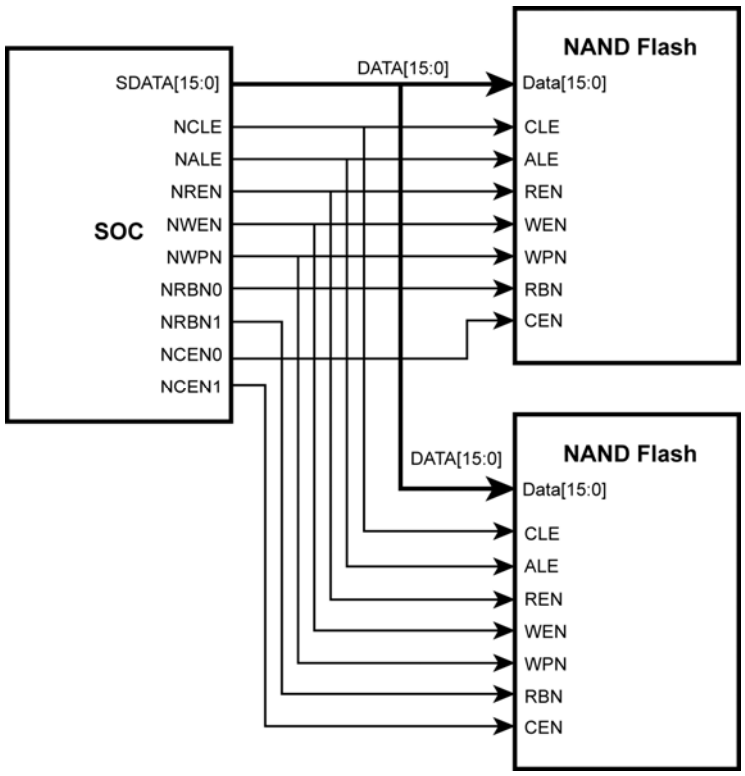

Figure 7. 16-bit NAND Interface Examples

DDR Controller

The KSZ8692MPB/KSZ8692XPB DDR memory controller provides interface for accessing external Double Data Rate Synchronous DRAM. In addition, the KSZ8692MPB/KSZ8692XPB provides two integrated DDR differential clock drivers for a complete glueless DDR interface solution.

- Up to 200MHz clock frequency (400 MHz data rate)
- Supports one 32-bit data width bank (16-bit optional)
- Up to 128 MB of addressable space is available with 12 columns and 14 row address lines
- Supports all DDR device densities up to 1Gb
- Supports all DDR device data width x8 and x16
- Configurable DDR RAS and CAS timing parameters
- Two integrated JEDEC Specification JESD82-1 compliant differential clock drivers for a glueless DDR interface solution
- JEDEC Specification SSTL_2 I/Os

A dedicated internal PLL provides clocking to the DDR memory controller and the two differential clock drivers. This PLL is programmable up to 200MHz and independent of AHB and ARM processor core clocks.

Figures 8 and 9 illustrate examples of bank configurations.

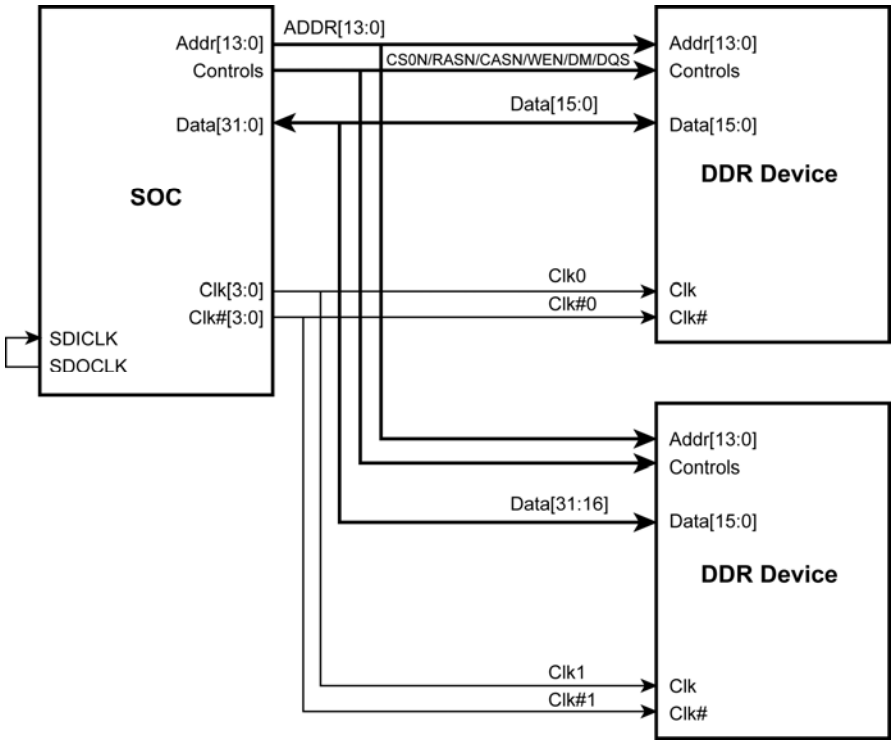

Figure 8. Two 16-bit DDR Memory Device Interface Example

SDIO/SD Host Controller (for KSZ8692MPB only)

Integrated SDIO/SD host controller provides interface for removable mass storage memory card and I/O devices.

- Meets SD Host Controller Standard Specification Version 1.0
- Meets SD memory card spec 1.01 . MMC spec 3.31
- Meets SDIO card specification version 1.0
- 1or 4 bit mode supported
- Card detection-insertion/removal
- Line Status LED driver
- Password protection of cards
- Supports read wait control, suspend/resume operation
- Support multi block read and write
- Up to 12.5 Mbytes per second read and write rates using 4 parallel line for full speed card.
- Dedicated DMA or programmed I/O data transfer

USB 2.0 Interface

Integrated dual USB 2.0 interface can be configured as 2-port host, or host + device. Figures 12 and 13 illustrate examples of USB 2.0 interface applications.

- Compliant with USB Specification Revision 2.0
- Compliant with Open Host Controller Interface (OHCI) Specification Rev 1.0a
- Compliant with Enhanced Host Controller Interface (EHCI) Specification Rev 1.0
- Root hub with 2 (max) downstream facing ports which are shared by OHCI and EHCI host controller cores
- All downstream facing ports can handle High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) transaction
- OTG not supported
- Integrated 45-ohm termination, 1.5K pull-up and 15K pull-down resistors
- Support endpoint zero, and up to 6 configurable endpoints (IN/OUT, isochronous/ control/ interrupt/ bulk)
- One isochronous endpoint (IN or OUT)
- Dedicated DMA Channel for each port

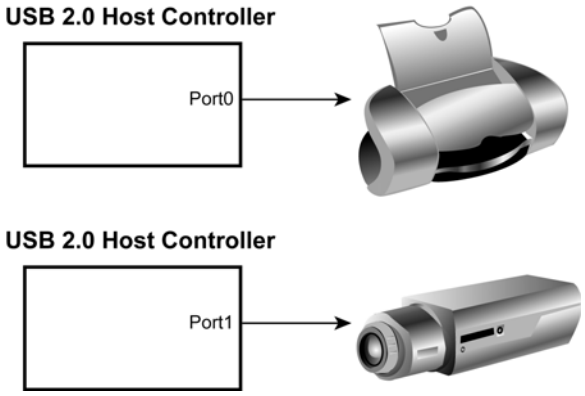

Figure 12. USB 2.0 Configuration as Two-Port Host

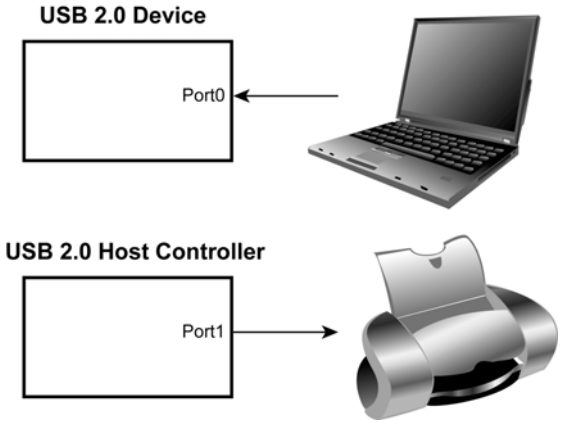

Figure 13. USB 2.0 Configuration as Host + Device

pre-programmed by the policy owner or other software with information on how to identify wake frames from other network traffic.

A wake-up event is a request for hardware and/or software external to the network device to put the system into a powered state.

A wake-up signal is caused by:

1. Detection of a change in the network link state
2. Receipt of a network wake-up frame
3. Receipt of a Magic Packet

There are also other types of wake-up events that are not listed here as manufacturers may choose to implement these in their own way.

Link Change

Link status wake events are useful to indicate a change in the network's availability, especially when this change may impact the level at which the system should re-enter the sleeping state. For example, a change from link off to link on may trigger the system to re-enter sleep at a higher level (D2 versus D3[1]) so that wake frames can be detected. Conversely, a transition from link on to link off may trigger the system to re-enter sleep at a deeper level (D3 versus D2) since the network is not currently available.

Wake-up Packet

Wake-up packets are certain types of packets with specific CRC values that a system recognizes to as a 'wake up' frame. The KSZ8692MPB/KSZ8692XPB supports up to four user defined wake-up frames on each network controller port:

Magic Packet

Magic Packet technology is used to remotely wake up a sleeping or powered off PC or device on network. This is accomplished by sending a specific packet of information, called a Magic Packet frame, to a node on the network. When a PC or device capable of receiving the specific frame goes to sleep, it enables the Magic Packet RX mode in the networkcontroller, and when the networkcontroller receives a Magic Packet frame, it will alerts the system to wake up.

Magic Packet is a standard feature integrated into the KSZ8692MPB/KSZ8692XPB. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently.

Once the KSZ8692MPB/KSZ8692XPB has been put into Magic Packet Enable mode, it scans all incoming frames addressed to the node for a specific data sequence, which indicates to the controller this is a Magic Packet (MP) frame.

A Magic Packet frame must also meet the basic requirements for the networktechnology chosen, such as Source Address (SA), or Destination Address (DA), which may be the receiving station's IEEE address or a multicast or broadcast address and CRC.

The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler. The synchronization stream is defined as 6 bytes of XoffFFh. The device will also accept a broadcast frame, as long as the 16 duplications of the IEEE address match the address of the machine to be awakened.

Example:

If the IEEE address for a particular node on a network is 11h 22h, 33h, 44h, 55h, 66h, the networkcontroller would be scanning for the data sequence (assuming an Ethernet frame):

DESTINATION SOURCE – MISC - .: FF FF FF FF FF FF - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - 11 22 33 44 55 66 - MISC - CIRC.

There are no further restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet or an IPX packet. The frame may be bridged or routed across the network without affecting its ability to wake-up a node at the

[1] References to D0, D1, D2, and D3 are power management states defined in a similar fashion to the way they are defined for PCI. For more information, refer to the PCI specification at www.pcisig.com/specifications/conventional/pcipm1.2.pdf.

Pin Number	Pin Name	Pin Type	Pin Description
T2, U1, L5, N4, P3, R2, T1, M4, K5, N3, P2, R1, L4, M3, P1, K4	SDATA[15..0]	Ipu/O	SRAM DATA Bus. Bidirectional Bus for 16-bit DATA In and DATA Out. The KSZ8692MPB/KSZ8692XPB also supports 8-bit data bus for ROM/SRAM/FLASH/EXTIO cycles. This data bus is shared between NAND, ROM/SRAM/FLASH/EXTIO devices.
L3	ECS2	O	External I/O Chip Select 2, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
N1	ECS1	O	External I/O Chip Select 1, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
M2	ECS0	O	External I/O Chip Select 0, asserted Low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. ECSN signals indicate which of the three I/O banks is selected.
K3	RCSN1	O	ROM/SRAM/FLASH(NOR) Chip select 1, asserted Low. The KSZ8692MPB/KSZ8692XPB can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
L1	RCSN0	O	ROM/SRAM/FLASH(NOR) Chip select 0, asserted Low. The KSZ8692MPB/KSZ8692XPB can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks. This bank is configurable as boot option
N2	EWAITN	I	External Wait asserted Low. This signal is asserted when an external I/O device or ROM/SRAM/FLASH(NOR) bank needs more access cycles than those defined in the corresponding control register.
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device.
J5	ERWEN1	O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[15..8] for ROM/SRAM/FLASH and EXTIO access.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, this signal controls the byte write enable of the memory device SDATA[7..0 or 15..0] for ROM/SRAM/FLASH and EXTIO access.
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash.
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash.
T3	NCEN1	O	NAND Bank Chip Enable 1, asserted low NAND device bank 1 selection control.

Ethernet Port 0			
M16	P0_RXC	Ipd/O	MAC mode MII: input RX clock PHY mode MII: output RX clock
P18, N17, P17, N16	P0_RXD[3:0]	I	RX data[3:0]
N18	P0_RXDV	I	MII mode: RX data valid
P19	P0_RXER	I	MII mode: RX error
M17	P0_CRS	I	MAC mode MII: input carrier sense
P20	P0_COL	I	MAC mode MII: input collision
M18	P0_TXC	Ipd/O	MAC mode MII: input TX clock PHY mode MII: output TX clock
L17, M19, N20, N19	P0_TXD[3:0]	O	TX data[3:0]
L16	P0_TXEN	O	MII: TX enable
Ethernet Port 1			
K19	P1_RXC	Ipd/O	MAC mode MII: input RX clock PHY mode MII: output RX clock
L20, L19, L18, M20	P1_RXD[3:0]	I	RX data[3:0]
K16	P1_RXDV	I	MII mode: RX data valid
K17	P1_RXER	I	MII mode: RX error
K18	P1_CRS	I	MAC mode MII: input carrier sense
K20	P1_COL	I	MAC mode MII: input collision
J17	P1_TXC	Ipd/O	MAC mode MII: input TX clock PHY mode MII: output TX clock
H20, J19, J18, J20	P1_TXD[3:0]	O	TX data[3:0] output.
J16	P1_TXEN	O	MII: TX enable
USB Interface			
G19	U1P	I/O (analog)	USB port 1 differential + signal
G20	U1M	I/O (analog)	USB port 1 differential - signal
F19	U2P	I/O (analog)	USB port 2 differential + signal
F20	U2M	I/O (analog)	USB port 2 differential - signal
G17	USBXI	I (analog)	Crystal in for USB PLL
G18	USBXO	O (analog)	Crystal out for USB PLL
H16	USBREXT	I (analog)	Connect to an external resistor 3.4K ohm to GND

G16	USBTEST	O (analog)	USB analog test output (factory reserved)

Pin Number	Pin Name	Pin Type	Pin Description
G15	USBCFG	I	USB port 2 configuration "1" = port 2 is host "0" = port 2 is device (port 1 is always host)
F18	USBHOVC0	I	Over current sensing input for Host Controller downstream port 1
F15	USBHOVC1	I	Over current sensing input for Host Controller downstream port 2
F17	USBHPWR0	Ipu/O (open drain)	Power switching control output for downstream port 1; open drain output
F16	USBHPWR1	Ipu/O (open drain)	Power switching control output for downstream port 2; open drain output
SDIO Interface (for KSZ8692MPB only)			
D14	KCMD	Ipd/O	SD 4-bit mode: Command line SD 1-bit mode: Command line
C18	KCLK	Ipd/O	SDIO/SD Clock
C15	KDATA3	I/O	SD 4-bit mode : data line 3 SD 1-bit mode : not used
C16	KDATA2	I/O	SD 4-bit mode : data line 2 or read wait (optional) SD 1-bit mode : read wait (optional)
E13	KDATA1	I/O	SD 4-bit mode : data line 1 or interrupt (optional) SD 1-bit mode : interrupt
C17	KDATA0	I/O	SD 4-bit mode : data line 0 SD 1-bit mode : data line
C14	KSDCDN	I	Active low used for Card Detection
D13	KSDWP	I	Active high used for Card write protection
General Purpose I/O			
B14	SLED/GPIO[19]	I/O	SDIO Line Status LED output (for KSZ8692MPB only) or General Purpose I/O Pin[19]
B15	CPUINTN/ GPIO[18]	I/O	Internal CPU interrupt request or General Purpose I/O Pin[18] As CPUINTN, any interrupt generated to ARM CPU asserts logic low on this pin. Useful for software development.
B16, B17, B18, D18, E15, D19	GPIO[17:12]	I/O	General Purpose I/O Pin[17:12]
F14	UART 4 RTSN /GPIO[11]	I/O	UART 4 RTS or general purpose I/O Pin[11]
E16	UART 4 CTSN /GPIO[10]	I/O	UART 4 CTS or general purpose I/O Pin[10]
E17	UART 3 RTSN /GPIO[9]	I/O	UART 3 RTS or general purpose I/O Pin[9]
E19	UART 3 CTSN /GPIO[8]	I/O	UART 3 CTS or general purpose I/O Pin[8]
E20	UART 2 RTSN /GPIO[7]	I/O	UART 2 RTS or general purpose I/O Pin[7]

Pin Number	Pin Name	Pin Type	Pin Description
E18	UART 2 CTSN /GPIO[6]	I/O	UART 2 CTS or general purpose I/O Pin[6]

Pin Number	Pin Name	Pin Type	Pin Description
U20, U19	TOUT[1:0]/ GPIO[5:4]	I/O	Timer 1/0 out or General Purpose I/O Pin[5:4]
V20, T18, V19, U18	EINT[3:0]/ GPIO[3:0]	I/O	External Interrupt Request or General Purpose I/O Pin[3:0]
I2S Interface			
C20	SCKIN	I	External crystal or clock input for I2S clock The maximum supported frequency is 49.2MHz
D20	SCKOUT	O	External crystal out for I2S clock
C19	I2S_MCLK	O	I2S master clock out This clock is of same frequency as SCKIN
B20	I2S_BCLK	O	I2S bit clock out
B19	I2S_LRCLK	O	Left/right select
A19	I2S_SDO	O	Serial data out
A20	I2S_SDI	I	Serial data in
MDIO/MDC Interface			
H18	MDC	Ipu/O	Clock for station management
H17	MDIO	Ipu/O	Serial data for station management
I2C/SPI Interface			
E14	SPCK_SCL	Ipu/O	SPI mode: master clock Output I2C mode: serial clock output
D17	SPMOSI_SDA	Ipu/O	SPI mode: master data out, slave data in I2C mode: serial data
D16	SPMISO	I	SPI master data in, slave data out
D15	SPICS	Ipu/O	SPI chip select
F13	SPI_RDY	I	Micrel SPI mode ready signal
PCI Interface Signals			
C3	PRSTN	I	PCI Reset, asserted Low In Host Bridge Mode, the PCI Reset pin is an input. This pin as well as the reset pin of all the devices on the PCI bus could be driven by WRSTO. In Guest Bridge Mode, this pin is input. The system reset to drive this pin.
B2	PCLK	I	PCI Bus Clock input. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz.
E4	GNT3N	O	PCI Bus Grant 3 Assert Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the master driving REQ3N. In Guest Bridge Mode, this is unused. (No connect for KSZ8692XPB)

Pin Number	Pin Name	Pin Type	Pin Description
A10	PERRN	I/O	PCI Parity Error signal, asserted Low. The KSZ8692MPB/KSZ8692XPB asserts PERRN when it checks and detects a bus parity error. When it generates the PAR output, the KSZ8692MPB/KSZ8692XPB monitors for any reported parity error on PERRN. When the KSZ8692MPB/KSZ8692XPB is the bus master and a parity error is detected, the KSZ8692MPB/KSZ8692XPB sets error bits on the control status registers. It completes the current data burst transaction, then stop the operation. After the Host clears the system error, the KSZ8692MPB/KSZ8692XPB continues its operation.
C9	SERRN	O (open drain)	PCI System Error signal, asserted Low. If an address parity error is detected, the KSZ8692MPB/KSZ8692XPB asserts the SERRN signal two clocks after the failing address.
C4	M66EN	I	PCI 66MHz Enable When asserted, this signal indicates the PCI Bus segment is operating at 66MHz. This pin is mainly used in Guest bridge mode when the PCLK is driven by the Host bridge.
F6	PCLKOUT3	O	PCI Clock output 3 (No connect for KSZ8692XPB)
D1	PCLKOUT2	O	PCI Clock output 2 (No connect for KSZ8692XPB)
D2	PCLKOUT1	O	PCI Clock output 1
E5	PCLKOUT0	O	PCI Clock output 0. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz, or 66MHz. In Host Bridge Mode, this is an output signal for all the devices on the PCI bus to sample data and control signals. Connect this clock to drive PCLK input. In Guest Bridge Mode, this is not used.
A8	CLKRUNN	I/O	This is a CardBus only signal. The CLKRUNN signal is used by portable CardBus devices to request the system to turn on the bus clock. Output is not generated.
C2	MPCIACTN	I/O	Mini-PCI active. This signal is asserted by the PCI device to indicate that its current function requires full system performance. MPCIACTN is an open drain output signal.
D5	PBMS	I	PCI Bridge Mode Select Select the operating mode of the PCI Bridge. When PBMS is High, the Host Bridge Mode is selected and on chip PCI bus arbiter is enabled. When PBMS is Low, the Guest Bridge Mode is selected and the on-chip arbiter is disabled.
A1	PMEN	O (open drain)	PCI Power Management Enable (active low) This pin is to inform the external PCI host that KSZ8692MPB/KSZ8692XPB has detected a wake-up event.

Pin Number	Pin Name	Pin Type	Pin Description
UART Signals			
P16	U1RXD	Ipd	UART 1 Receive Data
R16	U1TXD	O (Tri-State)	UART 1Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
R19	U1CTSN	Ipd	UART 1Clear to Send
R20	U1DCDN	Ipd	UART 1 Data Carrier Detect
P15	U1DSRN	Ipd	UART 1 Data Set Ready
R15	U2RXD	Ipd	UART 2 Receive Data
R17	U2TXD	O (Tri-State)	UART 2 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
R18	U3RXD	Ipd	UART 3 Receive Data
N15	U3TXD	O (Tri-State)	UART 3 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
T19	U4RXD	Ipd	UART 4 Receive Data
T20	U4TXD	O (Tri-State)	UART 4 Transmit Data Must be enabled as output by software, otherwise tri-stated upon power-up. External pull-up recommended.
TAP Control Signals			
A18	TCK	I	JTAG Test Clock
A17	TMS	I	JTAG Test Mode Select
A16	TDI	I	JTAG Test Data In
A15	TDO	O	JTAG Test Data Out
A14	TRSTN	I	JTAG Test Reset, asserted Low
Test Signals			
P5	SCANEN	Ipd	1 = Scan Enable (Factory reserved) 0 = Normal Operation
V2	TESTEN	Ipd	1 = Test Enable (Factory reserved) 0 = Normal Operation
V1	TESTEN1	Ipd	1 = Test Enable1 (Factory reserved) 0 = Normal Operation
Y2	TEST1	O (analog)	Factory reserved
W2	TEST2	O (analog)	Factory reserved
Power and Ground (96)			
N6, M6, M7, G7, G8, G9, M14, M15, N14, P11, P12,P13,P14	VDD1.2	P	Digital power supply 1.3V (13)

Pin Number	Pin Name	Pin Type	Pin Description
G6, H6, J6, K6, F7, F8, F9, F10, F11, G10, G11, H14, J14, K14,K15,L15	VDD3.3	P	Digital power supply 3.3V (16)
R6, R7, R8, R9, R10, R11, R12, R13, R14, T8, T9, T10, T11	VDD2.5	P	DDR Pad Driver 2.5V or 2.6V Power Supply. (13)
H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, K12, L7, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, N9, N10, N11, N12, N13, P7, P8, P9, P10	GND	GROUND	Digital Ground. (37)
L6	PLLVDDA3.3	P	Band Gap Reference Analog Power. (1)
M8	PLLVSSA3.3	GROUND	Band Gap Reference Analog Ground. (1)
P6	PLLDVDD1.2	P	De-skew PLL Analog and Digital Power. (1)
M5	PLLSVDD1.2	P	System PLL Analog and Digital Power. (1)
N7, N8	PLLVSS1.2	GROUND	De-skew PLL and System PLL Ground. (2)
L8	PLLVSSISO	GROUND	Ground Isolation PLL and other circuit. (1)
G12	USB1VDDA3.3	P	Analog Power for USB Channel 1. (1)
G13	USBCVDDA3.3	P	Analog Power for Common Circuit of USB Channel 1 and 2. (1)
G14	USB2VDDA3.3	P	Analog Power for USB Channel 2. (1)
H13, J13, K13	USBVSSA3.3	GROUND	Analog Ground for both USB Channels Analog Circuit. (3)
J15	USB1VDD1.2	P	Digital Power for USB Channel 1 Controller. (1)
H15	USB2VDD1.2	P	Digital Power for USB Channel 2 Controller. (1)
J12	USBVSS1	GROUND	Digital Ground for USB Channel 1 Controller. (1)
H12	USBVSS2	GROUND	Digital Ground for USB Channel 2 Controller. (1)

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   O/I = Output in normal mode; input pin during reset.
   Ipu = Internal 55kΩ pull-up resistor.
   Ipd = Internal 55kΩ pull-down resistor.

Pin Number	Pin Name	Pin Type	Pin Description
M1	EROEN (WRSTPLS)	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Output Enable, asserted Low. When asserted, this signal controls the output enable port of the specified ROM/SRAM/FLASH memory and EXTIO device. During reset, this pin is used for Watchdog Timer Reset Polarity Select. This is a power strapping option pin for watchdog reset output polarity. “0” = WRSTO is selected as active high (default) “1” = WRSTO is selected as active low. This pin is shared with the EROEN pin.
J4	ERWEN0	Ipd/O	ROM/SRAM/FLASH(NOR) and EXTIO Write Byte Enable, asserted Low. When asserted, these signals control the byte write enable of the memory device for ROM/SRAM/FLASH and EXTIO access. During ARM tic test mode, this pin is TESTACK. During reset, this pin is the input strap option to enable MII mode at port0 (WAN port) 0: MII mode (default) 1: Factory Reserved
R3	NCLE	Ipd/O	NAND command Latch Enable NCLE controls the activating path for command sent to NAND flash. During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [2]. This bit along with configuration register bits [1:0] is used for boot program. This pin, along with NALE and NWEN, is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit
U2	NALE	Ipd/O	NAND Address Latch Enable NALE controls the activating path for address sent to NAND flash. During reset, this pin is the input strap option for NAND Flash configuration register (0x8054) bit [1]. This bit along with configuration register bits [2], [0] is used for boot program. This pin, along with NCLE and NWEN, is used to specify NAND Flash size. [NCLE, NALE, NWEN] 000 = 64Mbit 001 = 128Mbit (default) 010 = 256Mbit 011 = 512Mbit 100 = 1Gbit 101 = 2Gbit 110 = 4Gbit 111 = 8Gbit

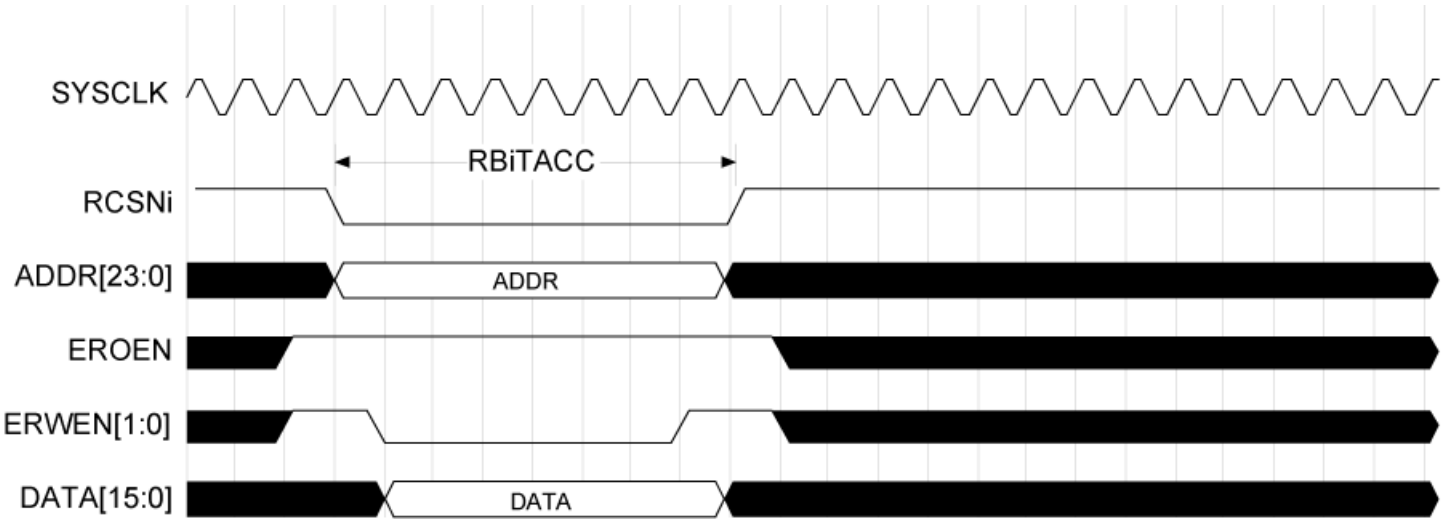

Figure 18. Static Memory Write Cycle

Symbol	Parameter[1]	Registers
RBiTACC	Programmable bank i access time	0x5010, 0x5014
RBiTPA	Programmable bank i page access time	0x5010, 0x5014

Table 2. Programmable Static Memory Timing Parameters

Note:

1. "i" Refers to chip select parameters 0 and 1.

Figure 19 provides external I/O ports interface timing.

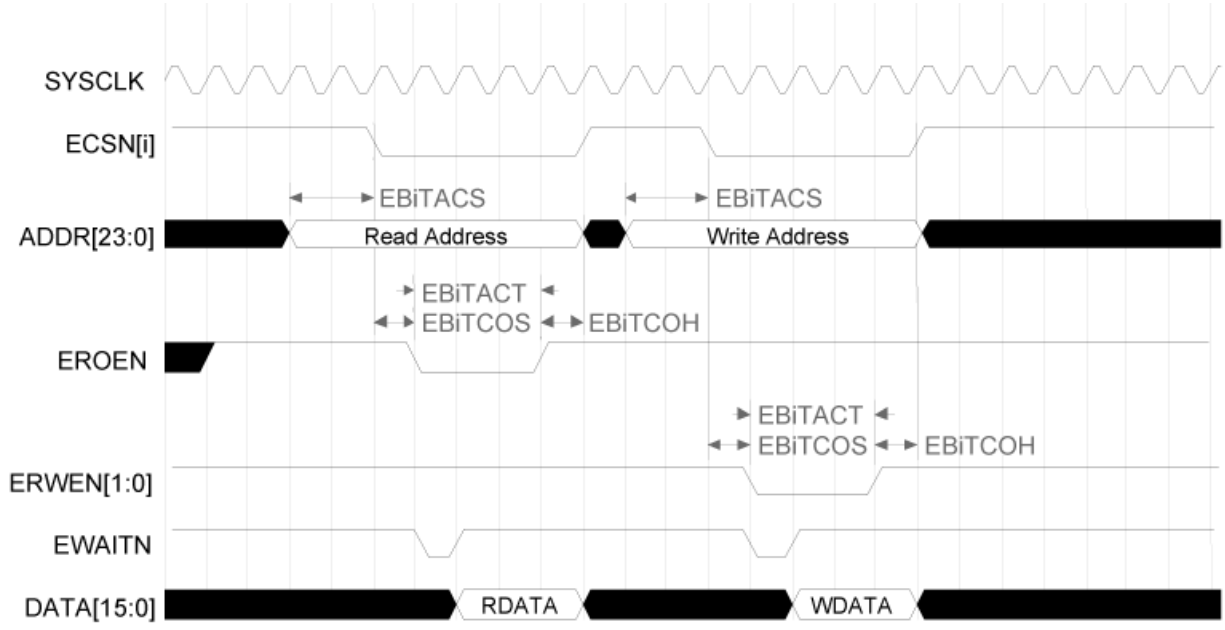

Figure 19. External I/O Read and Write Cycles

Symbol	Parameter	Min[1]	Typ[1]	Max[1]	Units
T_{cta}	Valid address to CS setup time	EBiTACS +0.8	EBiTACS +1.1	EBiTACS +1.3	ns
T_{cos}	OE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dsu}	Valid read data to OE setup time	2.0			ns
T_{cws}	WE valid to CS setup time	EBiTCOS +0.6	EBiTCOS +0.6	EBiTCOS +1.0	ns
T_{dh}	Write data to CS hold time	0			ns
T_{cah}	Address to CS hold time	EBiTCOH +1.0	EBiTCOH +1.0	EBiTCOH +1.4	ns
T_{oew}	OE/WE pulsewidth	EBiTACT		EBiTACT	ns
T_{ocs}, T_{csw}	Rising edge CS to OE/WE hold time	0			ns

Table 3. External I/O Memory Timing Parameters

Note:

1. Measurements for minimum were taken at 0°C, typical at 25°C, and maximum at 100°C.

Symbol	Parameter[1]	Registers
EBiTACS	Programmable bank i address setup time before chip select	0x5000, 0x5004, 0x5008
EBiTACT	Programmable bank i write enable/output enable access time	0x5000, 0x5004, 0x5008
EBiTCOS	Programmable bank i chip select setup time before OEN	0x5000, 0x5004, 0x5008
EBiTCOH	Programmable bank i chip select hold time	0x5000, 0x5004, 0x5008

Table 4. Programmable External I/O Timing Parameters

Note:

1. "i" Refers to chip select parameters 0, 1, or 2.