# STMicroelectronics - STM32L162VCT6D Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 25x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l162vct6d |

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## 2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From proprietary 8-bit to up to Cortex-M3, including the Cortex-M0+, the STM32Lx series are the best choice to answer the user needs, in terms of ultra-low-power features. The STM32 ultra-low-power series are the best fit, for instance, for gas/water meter, keyboard/mouse or fitness and healthcare, wearable applications. Several built-in features like LCD drivers, dual-bank memory, Low-power run mode, op-amp, AES 128-bit, DAC, USB crystal-less and many others will clearly allow to build very cost-optimized applications by reducing BOM.

*Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxxx and STM32Lxxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, the old applications can be upgraded to respond to the latest market features and efficiency demand.*

### 2.2.1 Performance

All the families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

### 2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

### 2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

### 2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

### 3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage $V_{SENSE}$ that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 61: Temperature sensor calibration values*.

### 3.10.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the $V_{DD}$ value (when no external voltage, VREF+, is available for ADC). The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 16: Embedded internal reference voltage calibration values*.

## 3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage $V_{REF+}$

Eight DAC trigger inputs are used in the STM32L162xC devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

## 3.12 Operational amplifier

The STM32L162xC devices embed two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

## 3.13 Ultra-low-power comparators and reference voltage

The STM32L162xC devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage ($V_{REFINT}$) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

## 3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage $V_{REFINT}$.

## 3.15 Touch sensing

The STM32L162xC devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 23 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven

## Alternate functions

**Table 10. Alternate function input/output**

| Port name | Digital alternate function number | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **AFIO0** | **AFIO1** | **AFIO2** | **AFIO3** | **AFIO4** | **AFIO5** | **AFIO6** | **AFIO7** | **..** | **AFIO11** | **..** | **AFIO14** | **AFIO15** |
| | **Alternate function** | | | | | | | | | | | | |
| | **SYSTEM** | **TIM2** | **TIM3/4/5** | **TIM9/ 10/11** | **I2C1/2** | **SPI1/2** | **SPI3** | **USART1/2/3** | | **LCD** | | **CPRI** | **SYSTEM** |
| BOOT0 | BOOT0 | - | - | - | - | - | - | - | | - | | - | EVENT OUT |
| NRST | NRST | - | - | - | - | - | - | - | | - | | - | - |
| PA0-WKUP1 | - | TIM2_CH1_ ETR | TIM5_CH1 | - | - | - | - | USART2_CTS | | - | | TIMx_IC1 | EVENT OUT |
| PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | USART2_RTS | | SEG0 | | TIMx_IC2 | EVENT OUT |
| PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | - | USART2_TX | | SEG1 | | TIMx_IC3 | EVENT OUT |
| PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | - | USART2_RX | | SEG2 | | TIMx_IC4 | EVENT OUT |
| PA4 | - | - | - | - | - | SPI1_NSS | SPI3_NSS<br>I2S3_WS | USART2_CK | | - | | TIMx_IC1 | EVENT OUT |
| PA5 | - | TIM2_CH1_ETR | - | - | - | SPI1_SCK | - | - | | - | | TIMx_IC2 | EVENT OUT |
| PA6 | - | - | TIM3_CH1 | TIM10_ CH1 | - | SPI1_MISO | - | - | | SEG3 | | TIMx_IC3 | EVENT OUT |
| PA7 | - | - | TIM3_CH2 | TIM11_ CH1 | - | SPI1_MOSI | - | - | | SEG4 | | TIMx_IC4 | EVENT OUT |
| PA8 | MCO | - | - | - | - | - | - | USART1_CK | | COM0 | | TIMx_IC1 | EVENT OUT |
| PA9 | - | - | - | - | - | - | - | USART1_TX | | COM1 | | TIMx_IC2 | EVENT OUT |
| PA10 | - | - | - | - | - | - | - | USART1_RX | | COM2 | | TIMx_IC3 | EVENT OUT |
| PA11 | - | - | - | - | - | SPI1_MISO | - | USART1_CTS | | - | | TIMx_IC4 | EVENT OUT |
| PA12 | - | - | - | - | - | SPI1_MOSI | - | USART1_RTS | | - | | TIMx_IC1 | EVENT OUT |
| PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | | - | | TIMx_IC2 | EVENT OUT |
| PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | | - | | TIMx_IC3 | EVEN TOUT |
| PA15 | JTDI | TIM2_CH1_ETR | - | - | - | SPI1_NSS | SPI3_NSS<br>I2S3_WS | - | | SEG17 | | TIMx_IC4 | EVEN TOUT |

### 6.3.3 Embedded internal reference voltage

The parameters given in *Table 17* are based on characterization results, unless otherwise specified.

**Table 16. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 30 °C ±5 °C<br>$V_{DDA}$= 3 V ±10 mV | 0x1FF8 00F8 - 0x1FF8 00F9 |

**Table 17. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\ out}$ (1) | Internal reference voltage | – 40 °C < $T_J$ < +110 °C | 1.202 | 1.224 | 1.242 | V |
| $I_{REFINT}$ | Internal reference current consumption | - | - | 1.4 | 2.3 | µA |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ and $V_{REF+}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REF}$ value(2) | Including uncertainties due to ADC and $V_{DDA}/V_{REF+}$ values | - | - | ±5 | mV |
| $T_{Coeff}$(3) | Temperature coefficient | –40 °C < $T_J$ < +110 °C | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$(3) | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$(3) | Voltage coefficient | 3.0 V < $V_{DDA}$ < 3.6 V | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$(3) | ADC sampling time when reading the internal reference voltage | - | 4 | - | - | µs |
| $T_{ADC\_BUF}$(3) (4) | Startup time of reference voltage buffer for ADC | - | - | - | 10 | µs |
| $I_{BUF\_ADC}$(3) | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | µA |
| $I_{VREF\_OUT}$(3) | VREF_OUT output current (5) | - | - | - | 1 | µA |
| $C_{VREF\_OUT}$(3) | VREF_OUT output load | - | - | - | 50 | pF |
| $I_{LPBUF}$(3) | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$(3) | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$(3) | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$(3) | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Guaranteed by test in production.
2. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.

5. To guarantee less than 1% VREF_OUT deviation.

### 6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to the Dhrystone 2.1 code, unless otherwise specified. The current consumption values are derived from tests performed under ambient temperature $T_A$ = 25 °C and $V_{DD}$ supply voltage conditions summarized in *Table 14: General operating conditions*, unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on $f_{HCLK}$ frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$.
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSCI_IN input follows the characteristic specified in *Table 27: High-speed external user clock characteristics*.
- For maximum current consumption $V_{DD} = V_{DDA}$ = 3.6 V is applied to all supply pins.
- For typical current consumption $V_{DD} = V_{DDA}$ = 3.0 V is applied to all supply pins if not specified otherwise.

Table 24. Typical and maximum current consumptions in Standby mode

| Symbol | Parameter | Conditions | | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ (Standby with RTC) | Supply current in Standby mode with RTC enabled | RTC clocked by LSI (no independent watchdog) | $T_A$ = -40 °C to 25 °C<br>$V_{DD}$ = 1.8 V | 0.905 | - | µA |
| | | | $T_A$ = -40 °C to 25 °C | 1.15 | 1.9 | |
| | | | $T_A$ = 55 °C | 1.5 | 2.2 | |
| | | | $T_A$= 85 °C | 1.750 | 4 | |
| | | | $T_A$ = 105 °C | 2.1 | 8.3[2] | |
| | | RTC clocked by LSE external quartz (no independent watchdog)[3] | $T_A$ = -40 °C to 25 °C<br>$V_{DD}$ = 1.8 V | 0.98 | - | |
| | | | $T_A$ = -40 °C to 25 °C | 1.3 | - | |
| | | | $T_A$ = 55 °C | 1.7 | - | |
| | | | $T_A$= 85 °C | 2.05 | - | |
| | | | $T_A$ = 105 °C | 2.45 | - | |
| $I_{DD}$ (Standby) | Supply current in Standby mode (RTC disabled) | Independent watchdog and LSI enabled | $T_A$ = -40 °C to 25 °C | 1 | 1.7 | |
| | | Independent watchdog and LSI OFF | $T_A$ = -40 °C to 25 °C | 0.29 | 0.6 | |
| | | | $T_A$ = 55 °C | 0.345 | 0.9 | |
| | | | $T_A$ = 85 °C | 0.575 | 2.75 | |
| | | | $T_A$ = 105 °C | 1.45 | 7[2] | |
| $I_{DD}$ (WU from Standby) | Supply current during wakeup time from Standby mode | - | $T_A$ = -40 °C to 25 °C | 1 | - | mA |

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

**Table 25. Peripheral current consumption(1) (continued)**

| Peripheral | | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|---|
| | | Range 1, $V_{CORE}$= 1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$= 1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$= 1.2 V VOS[1:0] = 11 | Low-power sleep and run | |
| APB2 | SYSCFG & RI | 2.6 | 2.0 | 1.6 | 2.0 | µA/MHz ($f_{HCLK}$) |
| | TIM9 | 7.9 | 6.4 | 5.0 | 6.4 | |
| | TIM10 | 5.9 | 4.7 | 3.8 | 4.7 | |
| | TIM11 | 5.9 | 4.6 | 3.7 | 4.6 | |
| | ADC(2) | 10.5 | 8.3 | 6.6 | 8.3 | |
| | SPI1 | 4.3 | 3.4 | 2.8 | 3.4 | |
| | USART1 | 8.8 | 7.1 | 5.6 | 7.1 | |
| AHB | GPIOA | 4.3 | 3.3 | 2.6 | 3.3 | |
| | GPIOB | 4.3 | 3.5 | 2.8 | 3.5 | |
| | GPIOC | 4.0 | 3.2 | 2.5 | 3.2 | |
| | GPIOD | 4.1 | 3.3 | 2.5 | 3.3 | |
| | GPIOE | 4.2 | 3.4 | 2.7 | 3.4 | |
| | GPIOH | 3.7 | 3.0 | 2.3 | 3.0 | |
| | CRC | 0.8 | 0.6 | 0.5 | 0.6 | |
| | AES | 5 | 4 | 3 | 4 | |
| | FLASH | 11.1 | 9.4 | 8 | -(3) | |
| | DMA1 | 15.6 | 12.7 | 10 | 12.7 | |
| | DMA2 | 16.3 | 13.4 | 10.5 | 13.4 | |
| All enabled | | 192 | 158 | 123 | 148.6 | |
| $I_{DD (RTC)}$ | | 0.4 | | | | µA |
| $I_{DD (LCD)}$ | | 3.1 | | | | |
| $I_{DD (ADC)}$(4) | | 1450 | | | | |
| $I_{DD (DAC)}$(5) | | 340 | | | | |
| $I_{DD (COMP1)}$ | | 0.16 | | | | |
| $I_{DD (COMP2)}$ | Slow mode | 2 | | | | |
| | Fast mode | 5 | | | | |
| $I_{DD (PVD / BOR)}$(6) | | 2.6 | | | | |
| $I_{DD (IWDG)}$ | | 0.25 | | | | |

1. Data based on differential $I_{DD}$ measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: $f_{HCLK}$ = 32 MHz (range 1), $f_{HCLK}$ = 16 MHz (range 2), $f_{HCLK}$ = 4 MHz (range 3), $f_{HCLK}$ = 64kHz (Low-power run/sleep), $f_{APB1}$ = $f_{HCLK}$, $f_{APB2}$ = $f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.

### Multi-speed internal (MSI) RC oscillator

Table 33. MSI oscillator characteristics

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{MSI}$ | Frequency after factory calibration, done at $V_{DD}$= 3.3 V and $T_A$ = 25 °C | MSI range 0 | 65.5 | - | kHz |
| | | MSI range 1 | 131 | - | |
| | | MSI range 2 | 262 | - | |
| | | MSI range 3 | 524 | - | |
| | | MSI range 4 | 1.05 | - | MHz |
| | | MSI range 5 | 2.1 | - | |
| | | MSI range 6 | 4.2 | - | |
| $ACC_{MSI}$ | Frequency error after factory calibration | - | ±0.5 | - | % |
| $D_{TEMP(MSI)}$(1) | MSI oscillator frequency drift<br>0 °C ≤ $T_A$ ≤ 105 °C | - | ±3 | - | % |
| $D_{VOLT(MSI)}$(1) | MSI oscillator frequency drift<br>1.65 V ≤ $V_{DD}$ ≤ 3.6 V, $T_A$ = 25 °C | - | - | 2.5 | %/V |
| $I_{DD(MSI)}$(2) | MSI oscillator power consumption | MSI range 0 | 0.75 | - | µA |
| | | MSI range 1 | 1 | - | |
| | | MSI range 2 | 1.5 | - | |
| | | MSI range 3 | 2.5 | - | |
| | | MSI range 4 | 4.5 | - | |
| | | MSI range 5 | 8 | - | |
| | | MSI range 6 | 15 | - | |
| $t_{SU(MSI)}$ | MSI oscillator startup time | MSI range 0 | 30 | - | µs |
| | | MSI range 1 | 20 | - | |
| | | MSI range 2 | 15 | - | |
| | | MSI range 3 | 10 | - | |
| | | MSI range 4 | 6 | - | |
| | | MSI range 5 | 5 | - | |
| | | MSI range 6, Voltage range 1 and 2 | 3.5 | - | |
| | | MSI range 6, Voltage range 3 | 5 | - | |

### 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 38. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 32 MHz conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 32 MHz conforms to IEC 61000-4-4 | 4A |

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 39. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. frequency range | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 4 MHz voltage range 3 | 16 MHz voltage range 2 | 32 MHz voltage range 1 | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V,<br>$T_A$ = 25 °C,<br>LQFP100 package compliant with IEC 61967-2 | 0.1 to 30 MHz | 3 | -6 | -5 | dBµV |
| | | | 30 to 130 MHz | 18 | 4 | -7 | |
| | | | 130 MHz to 1GHz | 15 | 5 | -7 | |
| | | | SAE EMI Level | 2.5 | 2 | 1 | - |

## 6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1. standard.

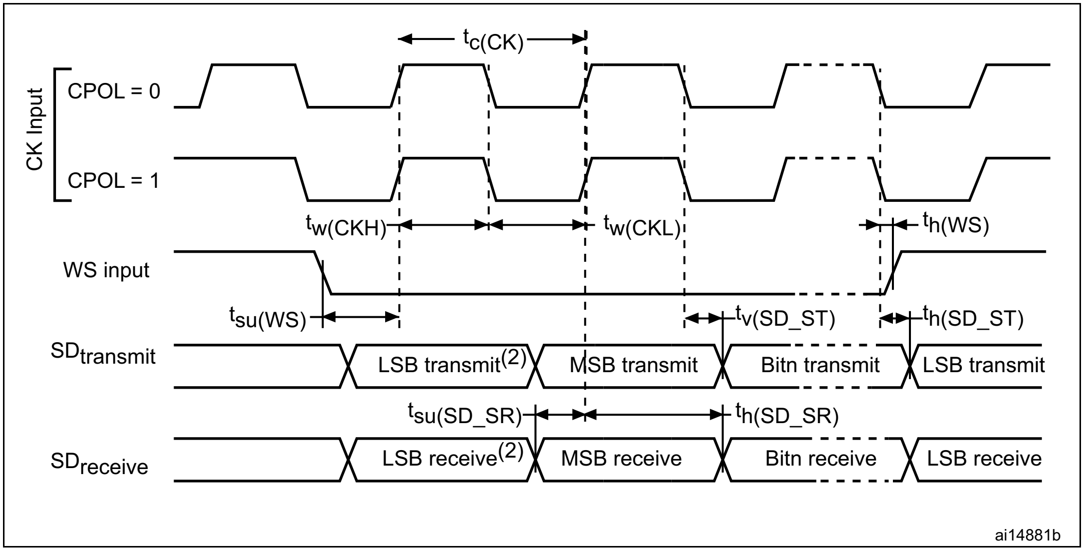
**Table 40. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value[1] | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1. | C4 | 500 | V |

1. Guaranteed by characterization results.

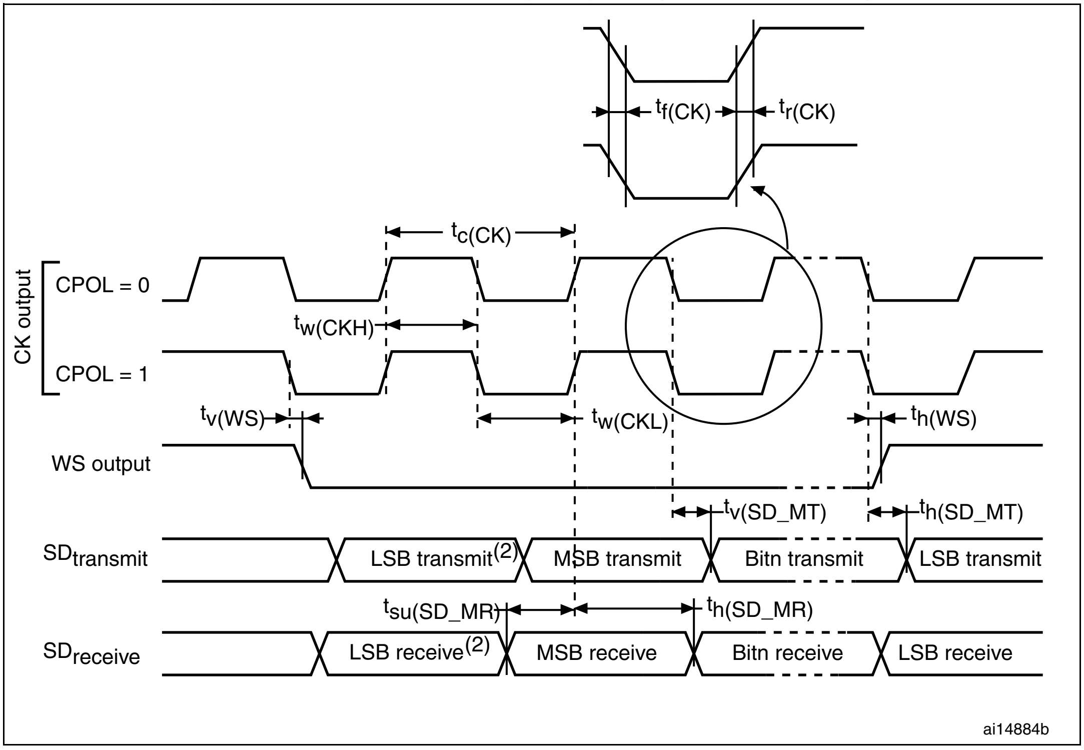
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

**Figure 23. I$^2$S slave timing diagram (Philips protocol)(1)**



1. Measurement points are done at CMOS levels: 0.3 × $V_{DD}$ and 0.7 × $V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 24. I$^2$S master timing diagram (Philips protocol)(1)**



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

## 6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 56* are guaranteed by design.

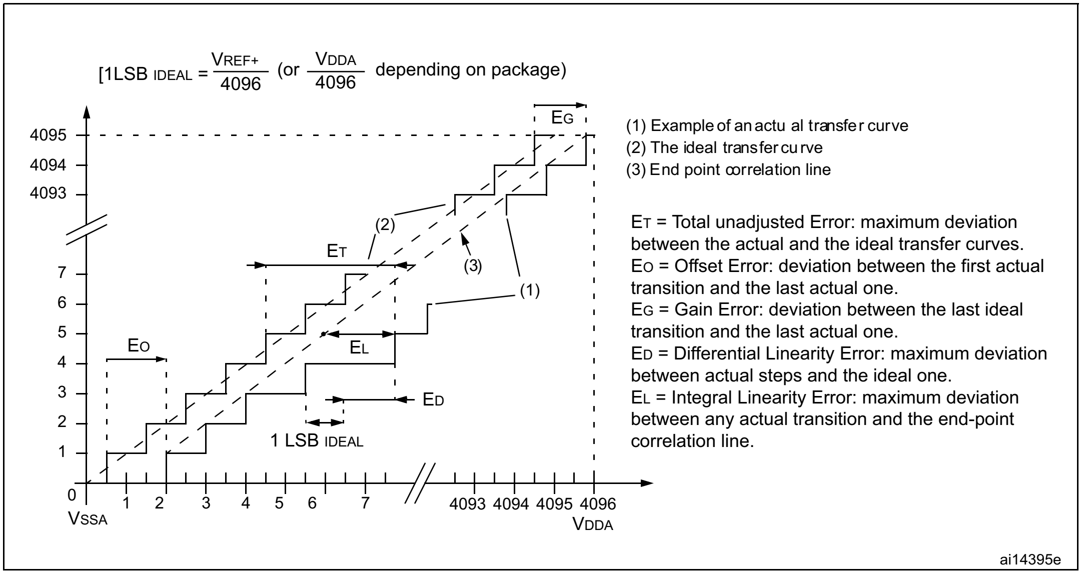
**Table 55. ADC clock frequency**

| Symbol | Parameter | Conditions | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | Voltage range 1 & 2 | 2.4 V $\leq V_{DDA} \leq$ 3.6 V | $V_{REF+} = V_{DDA}$ | 0.480 | 16 | MHz |
| | | | | $V_{REF+} < V_{DDA}$<br>$V_{REF+} >$ 2.4 V | | 8 | |
| | | | | $V_{REF+} < V_{DDA}$<br>$V_{REF+} \leq$ 2.4 V | | 4 | |
| | | | 1.8 V $\leq V_{DDA} \leq$ 2.4 V | $V_{REF+} = V_{DDA}$ | | 8 | |
| | | | | $V_{REF+} < V_{DDA}$ | | 4 | |
| | | Voltage range 3 | | | | 4 | |

**Table 56. ADC characteristics**

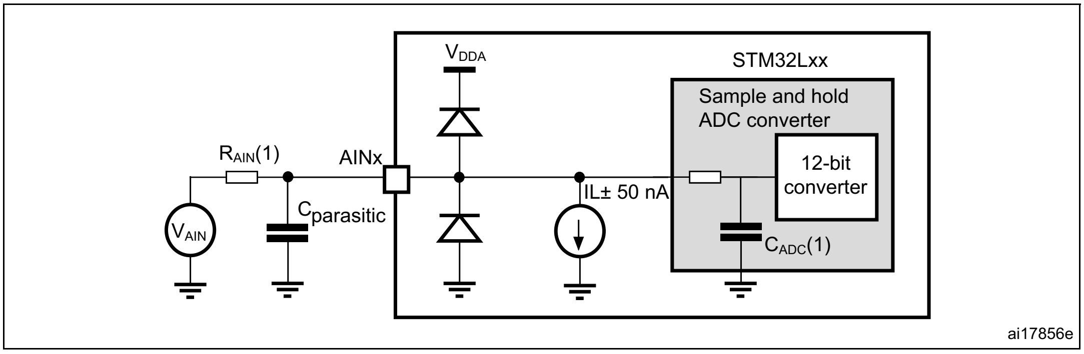
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | 1.8(1) | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | - | $V_{SSA}$ | - | |
| $I_{VDDA}$ | Current on the $V_{DDA}$ input pin | - | - | 1000 | 1450 | µA |
| $I_{VREF}$(2) | Current on the $V_{REF}$ input pin | Peak | - | 400 | 700 | |
| | | Average | - | | 450 | |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0(4) | - | $V_{REF+}$ | V |
| $f_S$ | 12-bit sampling rate | Direct channels | - | - | 1 | Msps |
| | | Multiplexed channels | - | - | 0.76 | |
| | 10-bit sampling rate | Direct channels | - | - | 1.07 | Msps |
| | | Multiplexed channels | - | - | 0.8 | |
| | 8-bit sampling rate | Direct channels | - | - | 1.23 | Msps |
| | | Multiplexed channels | - | - | 0.89 | |
| | 6-bit sampling rate | Direct channels | - | - | 1.45 | Msps |
| | | Multiplexed channels | - | - | 1 | |

Figure 25. ADC accuracy characteristics



ET = Total unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
EO = Offset Error: deviation between the first actual transition and the last actual one.
EG = Gain Error: deviation between the last ideal transition and the last actual one.
ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
EL = Integral Linearity Error: maximum deviation between any actual transition and the end-point correlation line.

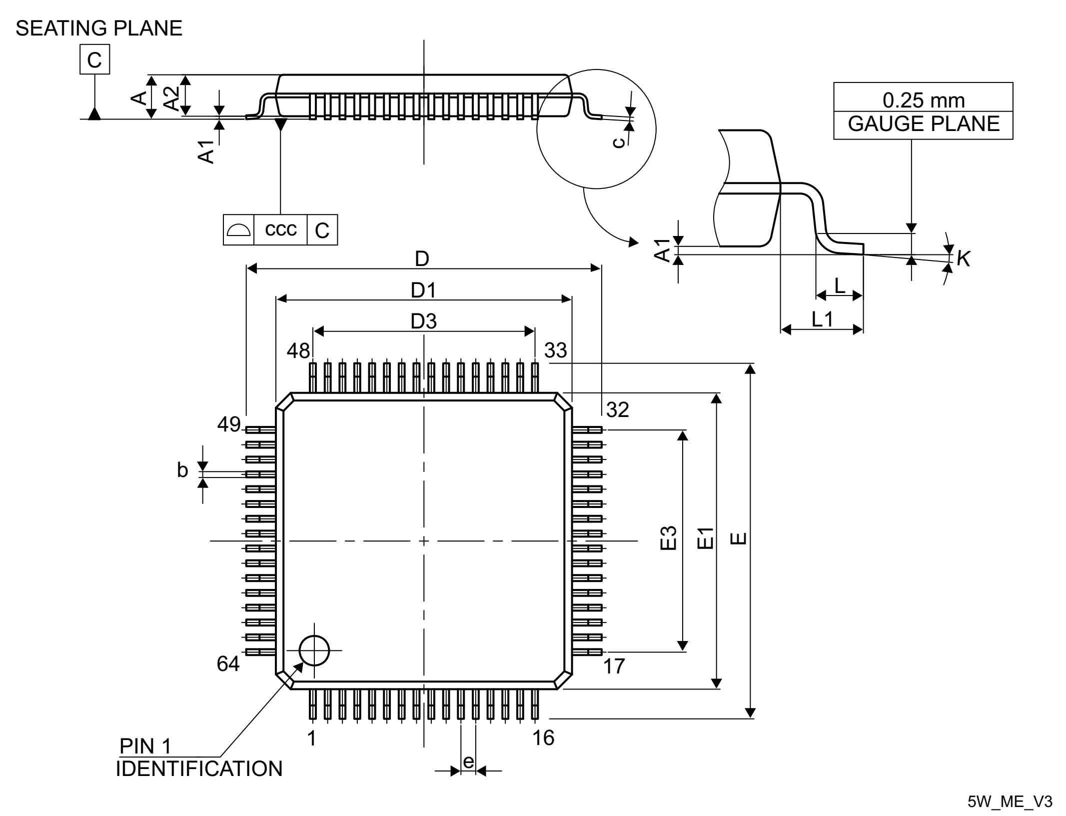
Figure 26. Typical connection diagram using the ADC



1. Refer to *Table 58: Maximum source impedance RAIN max* for the value of $R_{AIN}$ and *Table 56: ADC characteristics* for the value of $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## 7.2 LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 32. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline



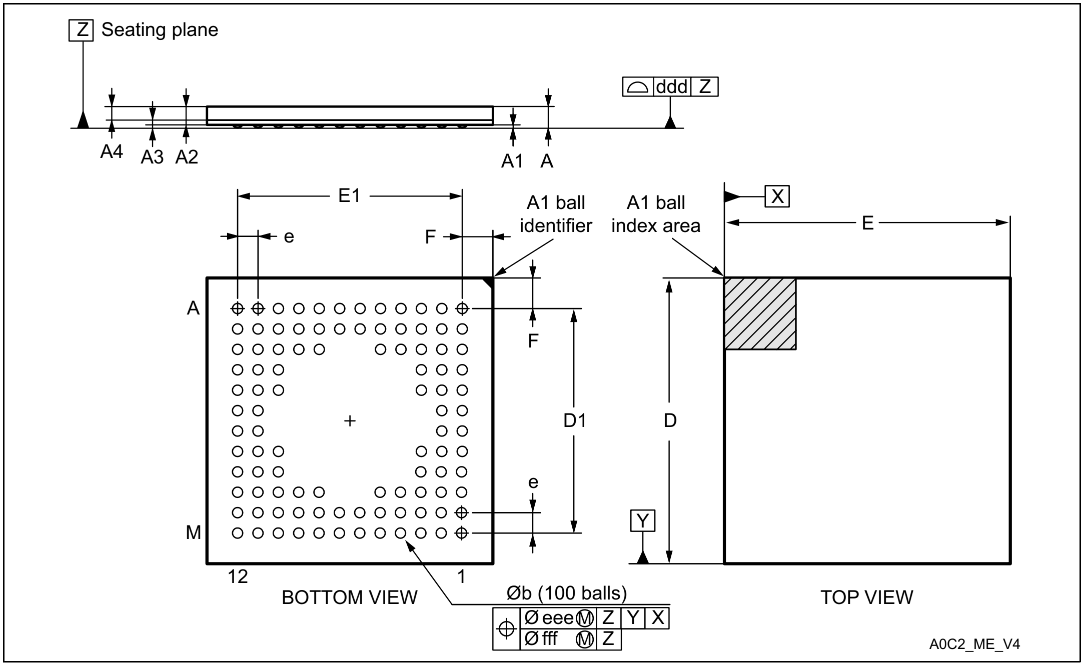
1. Drawing is not to scale.

Table 67. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

## 7.3 UFBGA100, 7 x 7 mm, 100-ball ultra thin, fine pitch ball grid array package information

Figure 35. UFBGA100, 7 x 7 mm, 0.5 mm pitch package outline



1. Drawing is not to scale.

Table 68. UFBGA100, 7 x 7 mm, 0.5 mm pitch package mechanical data

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.080 | 0.130 | 0.180 | 0.0031 | 0.0051 | 0.0071 |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| D | 6.950 | 7.000 | 7.050 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 5.450 | 5.500 | 5.550 | 0.2146 | 0.2165 | 0.2185 |
| E | 6.950 | 7.000 | 7.050 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 5.450 | 5.500 | 5.550 | 0.2146 | 0.2165 | 0.2185 |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | 0.700 | 0.750 | 0.800 | 0.0276 | 0.0295 | 0.0315 |
| ddd | - | - | 0.100 | - | - | 0.0039 |

## 7.4 Thermal characteristics

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + ($P_D$ max × $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL}$ × $I_{OL}$) + $\Sigma$(($V_{DD}$ – $V_{OH}$) × $I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 70. Thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>UFBGA100 - 7 x 7 mm | 59 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP100 - 14 x 14 mm / 0.5 mm pitch | 43 | |
| | **Thermal resistance junction-ambient**<br>LQFP64 - 10 x 10 mm / 0.5 mm pitch | 46 | |

**Figure 38. Thermal resistance suffix 6**