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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	34K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke14z128vlh7

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Table 5. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, LPIT, FlexIO, LPUART, LPI2C,LPSPI, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.

2.1.9 Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD interface.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 8 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

2.2.13 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/ Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer
- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.14 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

NOTE

The RESET_b pin is also a normal I/O pad with pseudo open-drain.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
40	26	PTC0	ADC0_SE8/ ACMP1_IN4/ TSI0_CH22	ADC0_SE8/ ACMP1_IN4/ TSI0_CH22	PTC0	FTM0_CH0					
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3			
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2			
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13	ADC0_SE13	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12	ADC0_SE12	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7/ TSI0_CH21	ADC0_SE7/ TSI0_CH21	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6/ TSI0_CH20	ADC0_SE6/ TSI0_CH20	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13						
50	—	PTC12	DISABLED		PTC12						
51	—	PTC11	DISABLED		PTC11						
52	—	PTC10	DISABLED		PTC10						
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	DISABLED		PTC9	LPUART1_TX				LPUART0_ RTS	
56	36	PTC8	DISABLED		PTC8	LPUART1_RX				LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	DISABLED		PTE7	FTM0_CH7					
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6		EWM_OUT_b			
63	—	PTB17	DISABLED		PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	DISABLED		PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	DISABLED		PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1					
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0					
69	44	PTD4	ADC1_SE6	ADC1_SE6	PTD4	FTM0_FLT3					
70	45	PTD3	NMI_b	ADC1_SE3	PTD3		LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2		LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3		LPI2C0_SCL	EWM_IN		LPUART0_TX	

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
73	48	PTA2	ADC1_SE0	ADC1_SE0	PTA2		LPI2C0_SDA	EWM_OUT_b		LPUART0_RX	
74	—	PTB11	DISABLED		PTB11		LPI2C0_HREQ				
75	—	PTB10	DISABLED		PTB10		LPI2C0_SDAS				
76	—	PTB9	DISABLED		PTB9		LPI2C0_SCLS				
77	—	PTB8	DISABLED		PTB8						
78	49	PTA1	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	PTA1	FTM1_CH1	LPI2C0_SDAS	FXIO_D3	FTM1_QD_ PHA	LPUART0_ RTS	TRGMUX_ OUT0
79	50	PTA0	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	PTA0	FTM2_CH1	LPI2C0_SCLS	FXIO_D2	FTM2_QD_ PHA	LPUART0_ CTS	TRGMUX_ OUT3
80	51	PTC7	ADC1_SE5/ TSI0_CH16	ADC1_SE5/ TSI0_CH16	PTC7	LPUART1_TX					
81	52	PTC6	ADC1_SE4/ TSI0_CH15	ADC1_SE4/ TSI0_CH15	PTC6	LPUART1_RX					
82	—	PTA16	DISABLED		PTA16	FTM1_CH3	LPSPI1_PCS2				
83	—	PTA15	DISABLED		PTA15	FTM1_CH2	LPSPI0_PCS3				
84	53	PTE6	ADC1_SE11	ADC1_SE11	PTE6	LPSPI0_PCS2				LPUART1_ RTS	
85	54	PTE2	ADC1_SE10/ TSI0_CH19	ADC1_SE10/ TSI0_CH19	PTE2	LPSPI0_SOUT	LPTMR0_ ALT3		PWT_IN3	LPUART1_ CTS	
86	—	VSS	VSS	VSS							
87	—	VDD	VDD	VDD							
88	—	PTA14	DISABLED		PTA14	FTM0_FLT0		EWM_IN			BUSOUT
89	55	PTA13	DISABLED		PTA13			LPI2C1_SCLS			
90	56	PTA12	DISABLED		PTA12			LPI2C1_SDAS			
91	57	PTA11	DISABLED		PTA11		LPUART0_RX	FXIO_D1			
92	58	PTA10	DISABLED		PTA10		LPUART0_TX	FXIO_D0			
93	59	PTE1	TSI0_CH14	TSI0_CH14	PTE1	LPSPI0_SIN	LPI2C0_HREQ	LPI2C1_SCL			
94	60	PTE0	TSI0_CH13	TSI0_CH13	PTE0	LPSPI0_SCK	TCLK1	LPI2C1_SDA		FTM1_FLT2	
95	61	PTC5	TSI0_CH12	TSI0_CH12	PTC5	FTM2_CH0	RTC_CLKOUT	LPI2C1_HREQ		FTM2_QD_ PHB	
96	62	PTC4	SWD_CLK	ACMP0_IN2	PTC4	FTM1_CH0	RTC_CLKOUT		EWM_IN	FTM1_QD_ PHB	SWD_CLK
97	63	PTA5	RESET_b		PTA5		TCLK1				RESET_b
98	64	PTA4	SWD_DIO		PTA4			ACMP0_OUT	EWM_OUT_b		SWD_DIO
99	—	PTA9	DISABLED		PTA9			FXIO_D7		FTM1_FLT3	
100	—	PTA8	DISABLED		PTA8			FXIO_D6			

4.2 Port control and interrupt summary

The following table provides more information regarding the Port Control and Interrupt configurations.

Table 6. Ports summary

Feature	Port A	Port B	Port C	Port D	Port E
Pull select control	Yes	Yes	Yes	Yes	Yes
Pull select at reset	PTA4/PTA5=Pull up, Others=No	No	PTC4=Pull down, Others=No	PTD3=Pull up, Others=No	No
Pull enable control	Yes	Yes	Yes	Yes	Yes
Pull enable at reset	PTA4/ PTA5=Enabled; Others=Disabled	Disabled	PTC4=Enabled; Others=Disabled	PTD3=Enabled; Others=Disabled	Disabled
Passive filter enable control	PTA5=Yes; Others=No	No	No	PTD3=Yes; Others=No	No
Passive filter enable at reset	PTA5=Enabled; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable control	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled	I2C and UART Tx=Enabled; Others=Disabled
Open drain enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Drive strength enable control	No	PTB4/PTB5 only	No	PTD0/PTD1/ PTD15/PTD16 only	PTE0/PTE1 only
Drive strength enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Pin mux control	Yes	Yes	Yes	Yes	Yes
Pin mux at reset	PTA4/PTA5=ALT7; Others=ALT0	ALT0	PTC4=ALT7; Others=ALT0	PTD3=ALT7; Others=ALT0	ALT0
Lock bit	Yes	Yes	Yes	Yes	Yes
Interrupt and DMA request	Yes	Yes	Yes	Yes	Yes
Digital glitch filter	No	No	No	No	Yes

4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

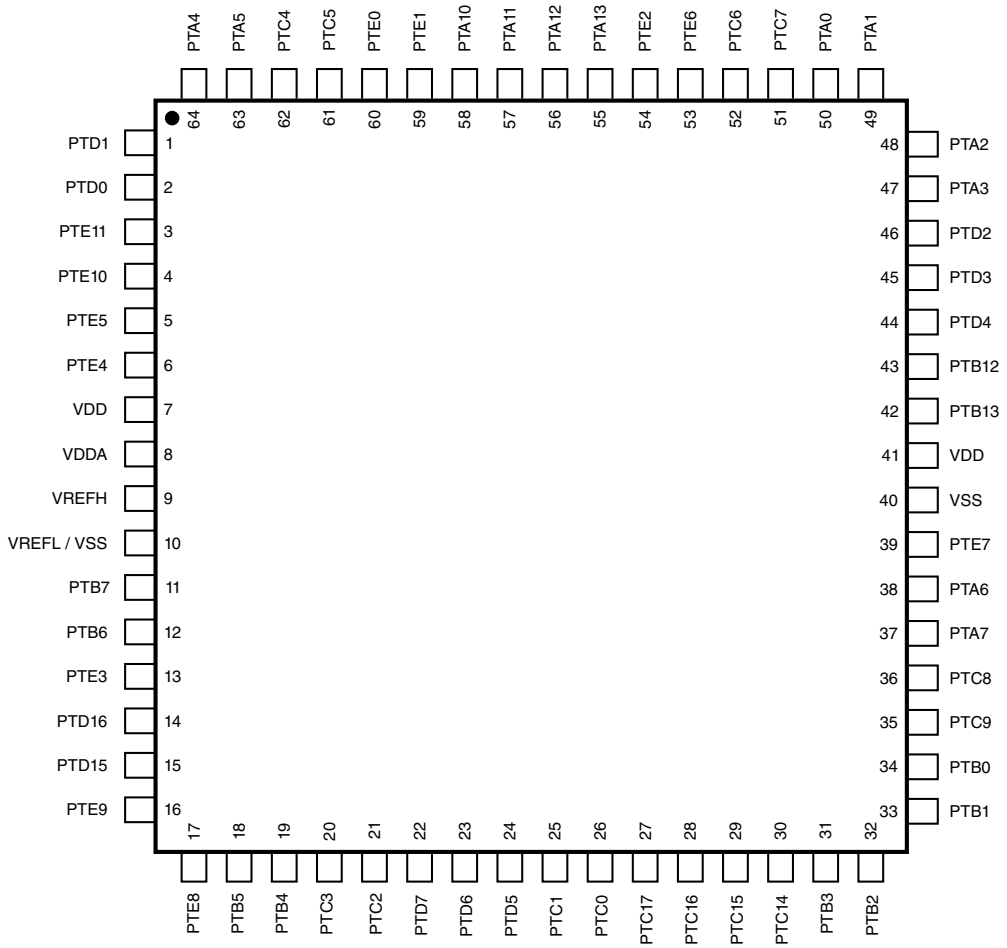
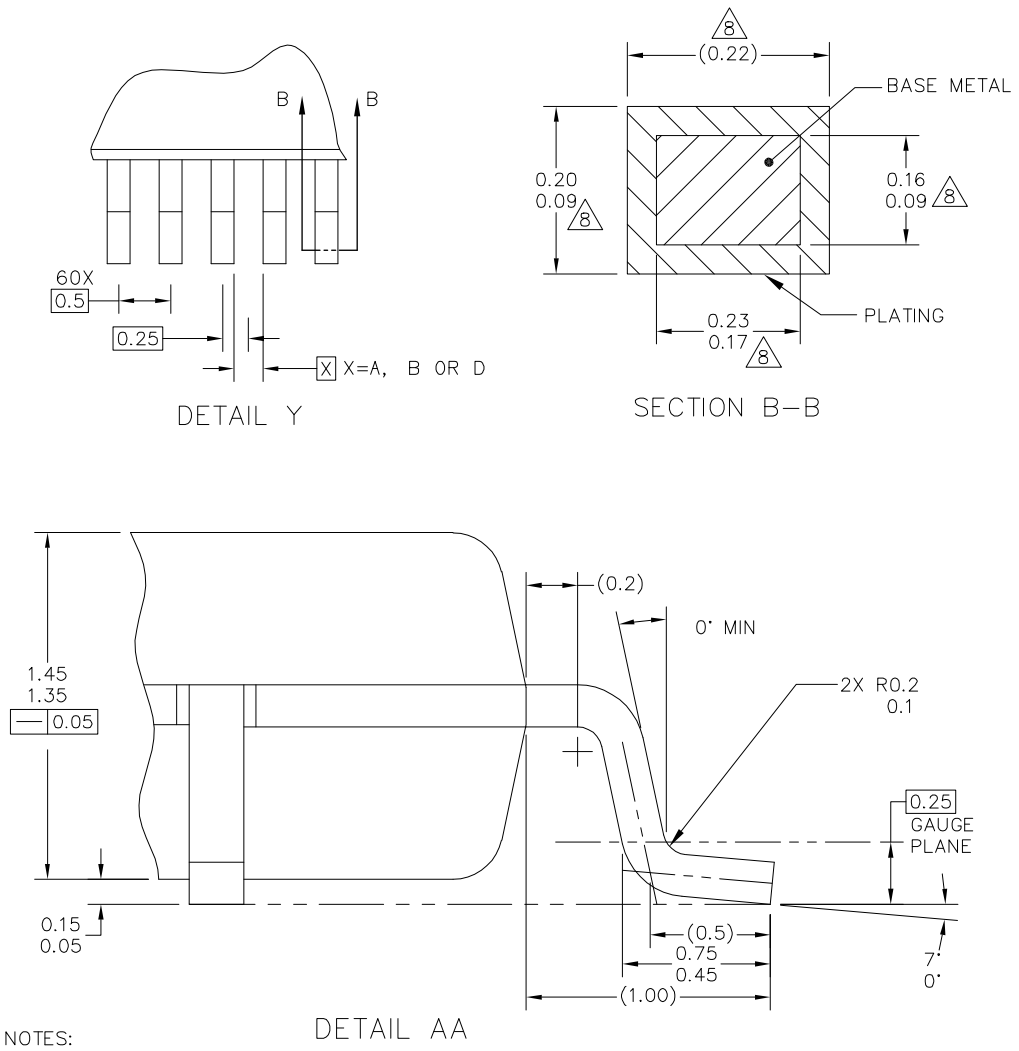


Figure 8. 64 LQFP Pinout Diagram

4.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

5.3.1 Nonswitching electrical specifications

5.3.1.1 Voltage and current operating requirements

Table 28. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	– 0.1	0.1	V	
I_{ICIO}	Analog DC injection current — single pin				
	$V_{IN} < V_{SS}$ - 0.3 V (Negative current injection)	– 5	—	mA	1, 2
	$V_{IN} > V_{DD}$ + 0.3 V (Positive current injection)	—	+ 5	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	– 25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	3

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
2. Max voltage levels that I/O pins can withstand while keeping the injection current (maximum) at 5mA:
   - Max supply V_{DD} = 6.0 V for 60 s lifetime (with no switching restrictions) or for 10 hours (if device is in reset or no switching state)
   - Max I/O pin voltage = 6.5 V (at injection current ≤ 5 mA) or 7.0 V (at injection current > 5 mA)
3. Open drain outputs must be pulled to V_{DD}.

5.3.1.2 DC electrical specifications at 3.3 V Range and 5.0 V Range

Table 29. DC electrical specifications

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{DD}	I/O Supply Voltage [1] @ V_{DD} = 3.3 V	2.7	3.3	4	V	
	@ V_{DD} = 5.0 V	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage @ V_{DD} = 3.3 V	0.7 × V_{DD}	—	V_{DD} + 0.3	V	
	@ V_{DD} = 5.0 V	0.65 × V_{DD}	—	V_{DD} + 0.3	V	

Table continues on the next page...

Symbol	Description	Typical
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in VLPS mode. ADC is configured for low power mode using SIRC clock source, 8-bit resolution and continuous conversions.	484 µA
I_{LPI2C}	LPI2C peripheral adder measured by placing the device in VLPS mode with selected clock source sending START and Slave address, waiting for RX data. Includes the DMA power consumption.	179 µA
I_{LPIT}	LPIT peripheral adder measured by placing the device in VLPS mode with internal SIRC 8 MHz enabled in Stop mode. Includes selected clock source power consumption.	18 µA
I_{LPSPI}	LPSPI peripheral adder measured by placing the device in VLPS mode with selected clock source, output data on SOUT pin with SCK 500 kbit/s. Includes the DMA power consumption.	565 µA

5.3.1.6.2 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- SCG in SOSC for both Run and VLPR modes
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

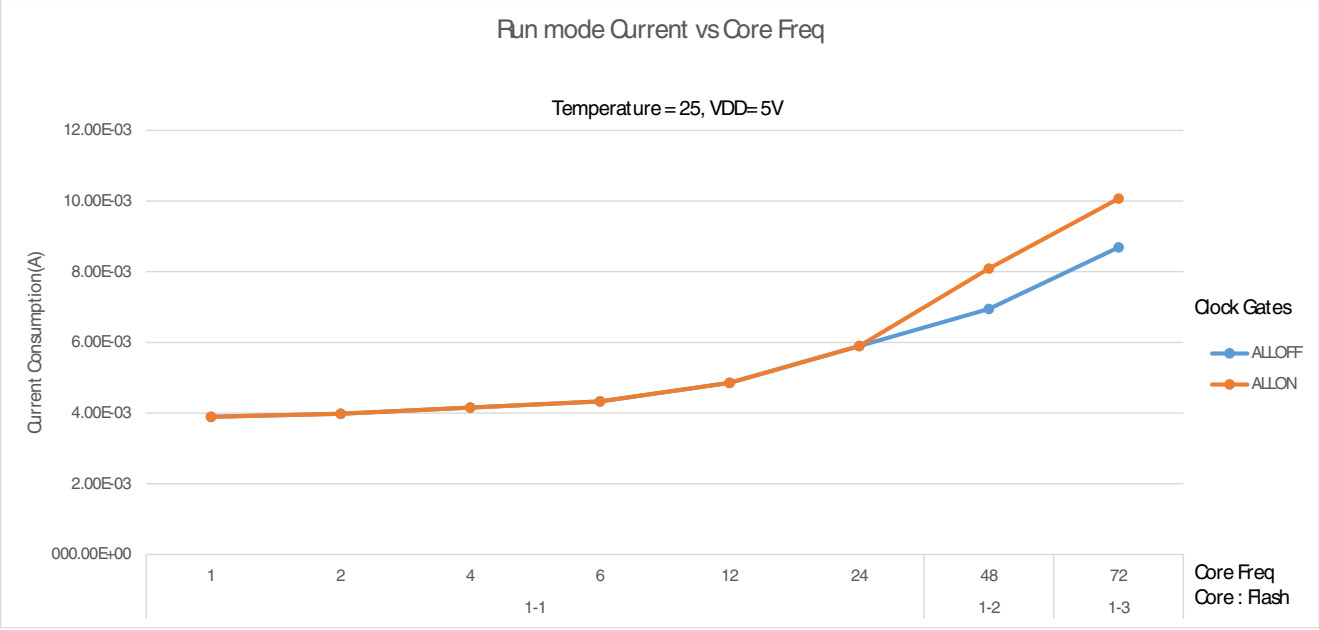


Figure 14. Run mode supply current vs. core frequency

5.3.2.4 AC specifications at 3.3 V range

Table 37. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	2.7		4	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	17.5	5	17	25
	28	9	32	50
High drive I/O pad	19	5	17	25
	26	9	33	50
CMOS Input [3]	4	1.2	3	0.5

1. Propagation delay measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.2.5 AC specifications at 5 V range

Table 38. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	4		5.5	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	12	3.6	10	25
	18	8	17	50
High drive I/O pad	13	3.6	10	25
	19	8	19	50
CMOS Input [3]	3	1.2	2.8	0.5

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

Table 43. External Oscillator electrical specifications (OSC) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		2
C_2	XTAL load capacitance	—	—	—		2
R_F	Feedback resistor					3
	Low-frequency, high-gain mode (32 kHz)	—	10	—	MΩ	
	High-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	—	—	MΩ	
	High-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	1	—	MΩ	
R_S	Series resistor					
	Low-frequency, high-gain mode (32 kHz)	—	200	—		
	High-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
	High-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					4
	Low-frequency, high-gain mode	—	3.3	—	V	
	High-frequency, low-gain mode	—	1.0	—	V	
	High-frequency, high-gain mode	—	3.3	—	V	

1. Measured at V_{DD} = 5 V, Temperature = 25 °C
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. When low power mode is selected, R_F is integrated and must not be attached externally.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.1.2 External Oscillator frequency specifications

Table 44. External Oscillator frequency specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode	30	—	40	kHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	2000	—	ms	1

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

5.4.2.2.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 47. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	Slow internal reference frequency	—	2 8	—	MHz
I_{VDD}	Supply current	—	23	—	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	—	—	—	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	—	±3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	6	—	µs[2]

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

5.4.2.2.3 Low Power Oscillator (LPO) electrical specifications

Table 48. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
I_{LPO}	Current consumption	1	3	7	µA
$T_{startup}$	Startup Time	—	—	20	µs

5.4.2.2.4 LPFLL electrical specifications

Table 49. LPFLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{avg}	Power consumption		240		µA
T_{start}	Start-up time		3.6		µs
ΔF_{ol}	Frequency accuracy over temperature and voltage in open loop after process trimmed	–10	—	10	%
ΔF_{cl}	Frequency accuracy in closed loop	–1 [1]	—	1 [1]	%

Table 51. Flash command timing specifications (continued)

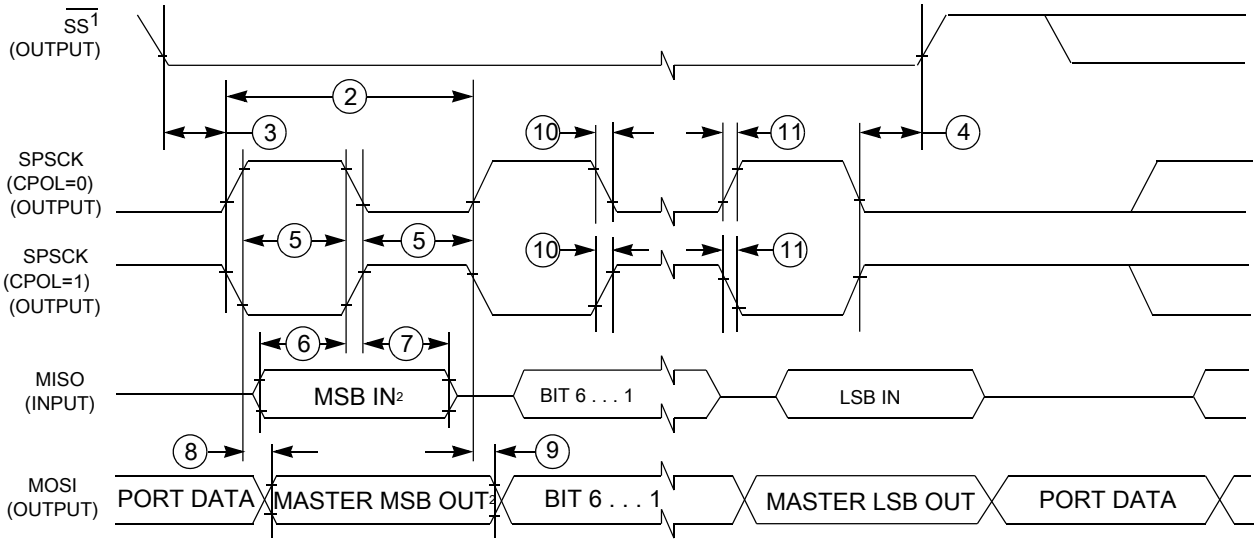
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{pgmsec512}$	Program Section execution time (512B flash)	—	2.5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2100	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2100	ms	2
	Program Partition for EEPROM execution time					
$t_{pgmpart24k}$	• 24 KB EEPROM backup	—	69	—	ms	
$t_{pgmpart32k}$	• 32 KB EEPROM backup	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram24k}$	• 24 KB EEPROM backup	—	0.6	1.1	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
	Byte-write to FlexRAM execution time:					
$t_{eewr8b24k}$	• 24 KB EEPROM backup	—	370	1625	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
	16-bit write to FlexRAM execution time:					
$t_{eewr16b24k}$	• 24 KB EEPROM backup	—	370	1625	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b24k}$	• 24 KB EEPROM backup	—	600	1950	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 52. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 25. LPSPI master mode timing (CPHA = 1)

Table 58. LPSPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

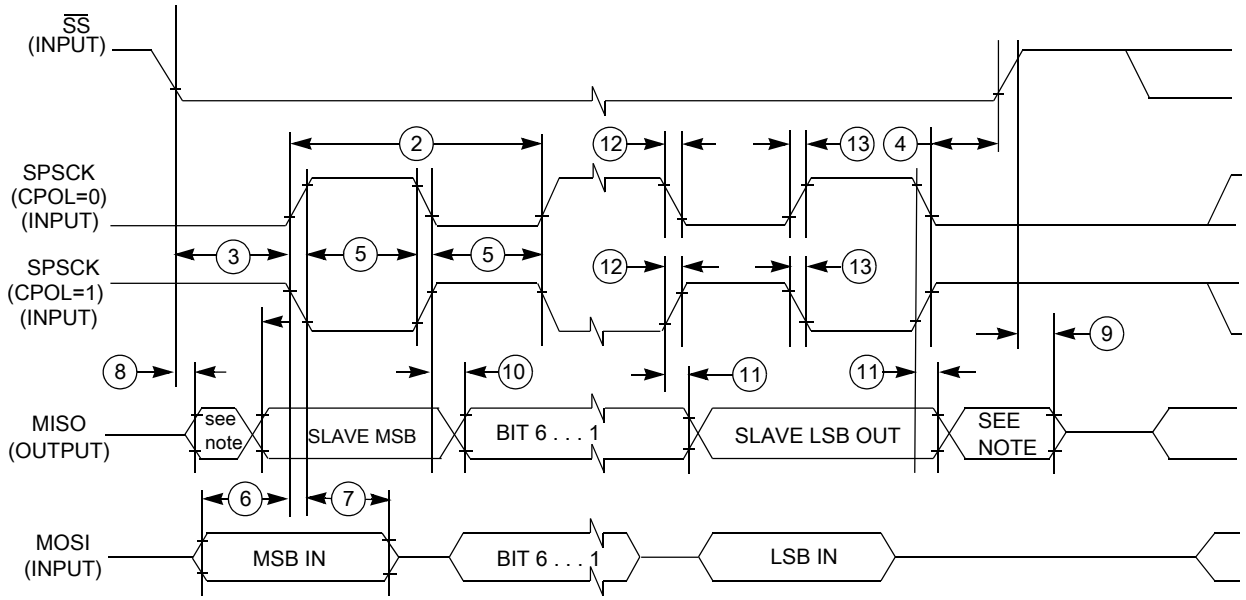


Figure 26. LPSPI slave mode timing (CPHA = 0)

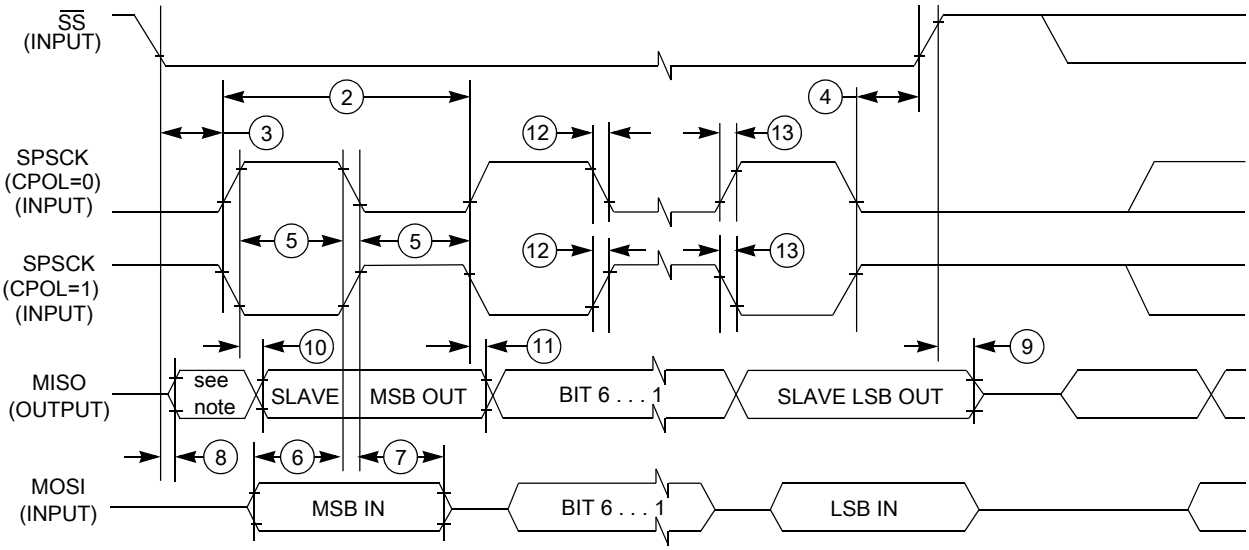


Figure 27. LPSPI slave mode timing (CPHA = 1)

5.4.6.3 LPI^{2}C

Table 59. LPI^{2}C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1, 2, 3
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		Ultra Fast mode (UFm)	0	5000		
		High speed mode (Hs-mode)	0	3400		

Table 61. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

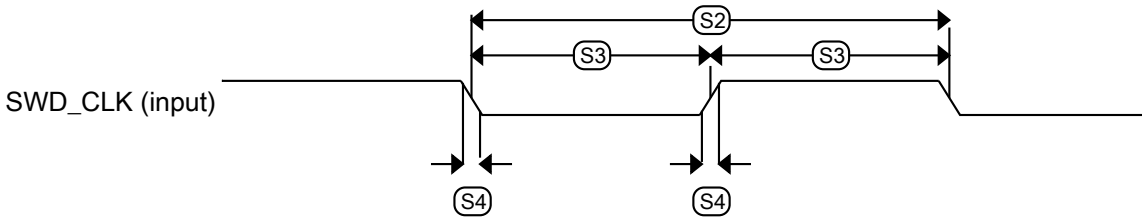


Figure 28. Serial wire clock input timing

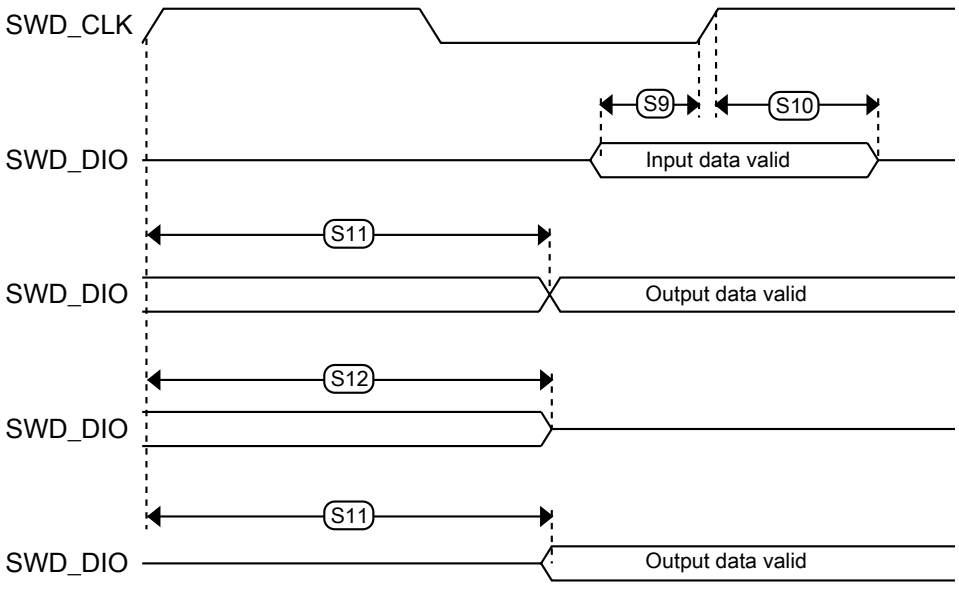


Figure 29. Serial wire data timing

6 Design considerations

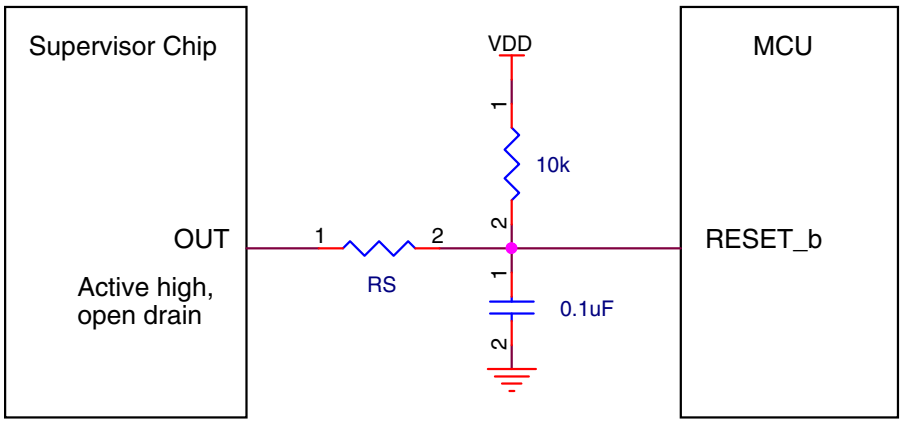


Figure 33. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

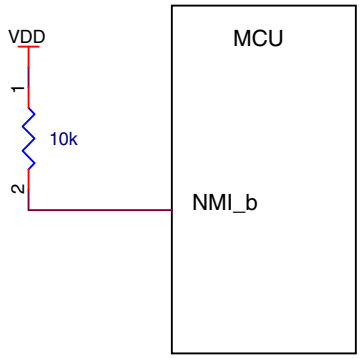


Figure 34. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

Table 63. Part number fields description (continued)

Field	Description	Values
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 7 = 72 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKE15Z256VLL7

8 Revision history

The following table provides a revision history for this document.

Table 64. Revision history

Rev. No.	Date	Substantial Changes
2	09/2016	Initial public release.