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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	89
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	34K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke14z128vll7

rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 5. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, LPIT, FlexIO, LPUART, LPI2C,LPSPI, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.

2.1.9 Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD interface.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 8 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

2.2.4 CMP

There are two analog comparators on this device.

- Each CMP has its own independent 8-bit DAC.
- Each CMP supports up to 6 analog inputs from external pins.
- Each CMP is able to convert an internal reference from the bandgap.
- Each CMP supports the round-robin sampling scheme. In summary, this allow the CMP to operate independently in VLPS and Stop modes, whilst being triggered periodically to sample up to 8 inputs. Only if an input changes state is a full wakeup generated.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising and falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, windowed, or digitally filtered

2.2.7 PDB

The Programmable Delay Block (PDB) provides controllable delays from either an internal or an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs and/or generates the interval triggers to DACs, so that the precise timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

The PDB module has the following capabilities:

- trigger input sources and one software trigger source
- 1 DAC refresh trigger output, for this device
- configurable PDB channels for ADC hardware trigger
- 1 pulse output, for this device

2.2.8 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.9 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.10 LPUART

This product contains three Low-Power UART modules, and can work in Stop and VLPS modes. The module also supports 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.

4.3.1 Core Modules

Table 7. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock	I
SWD_DIO	SWD_DIO	Serial Wire Data	I/O

4.3.2 System Modules

Table 8. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.	I
RESET_b	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 9. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_IN is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

4.3.3 Clock Modules

Table 10. OSC (in SCG) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL	EXTAL	External clock/Oscillator input	I
XTAL	XTAL	Oscillator output	O

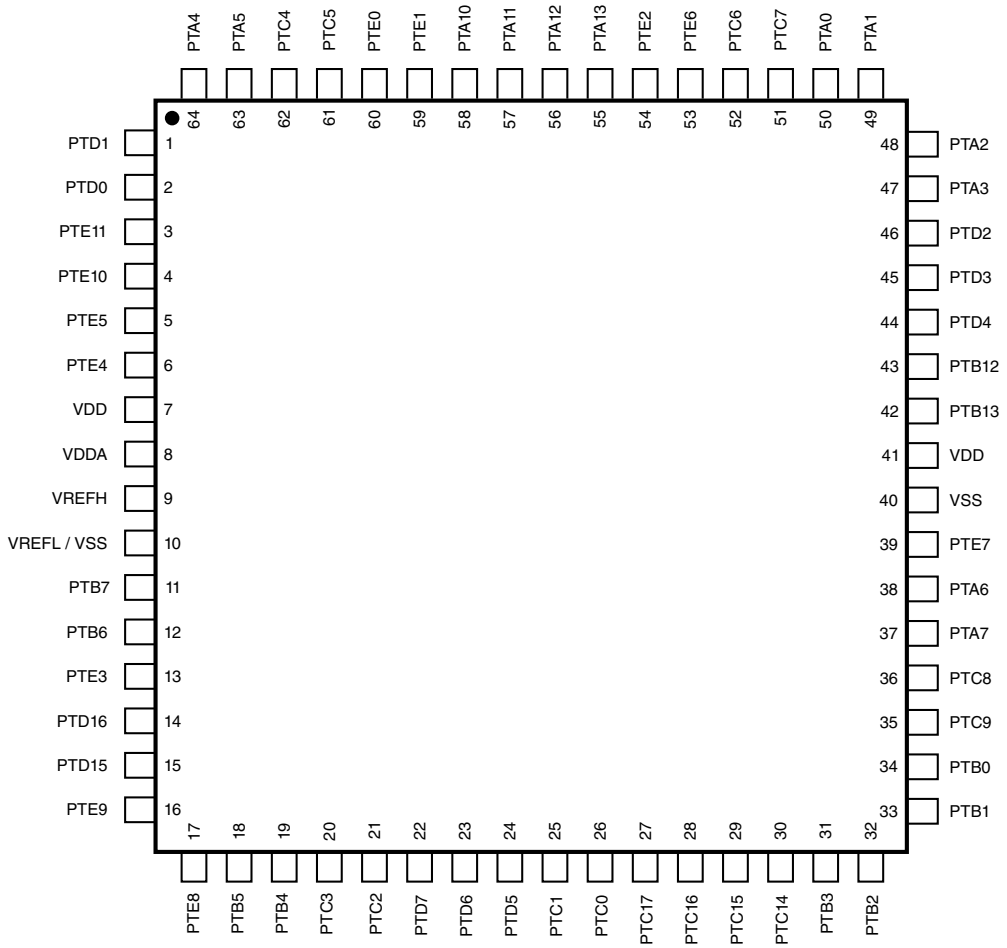
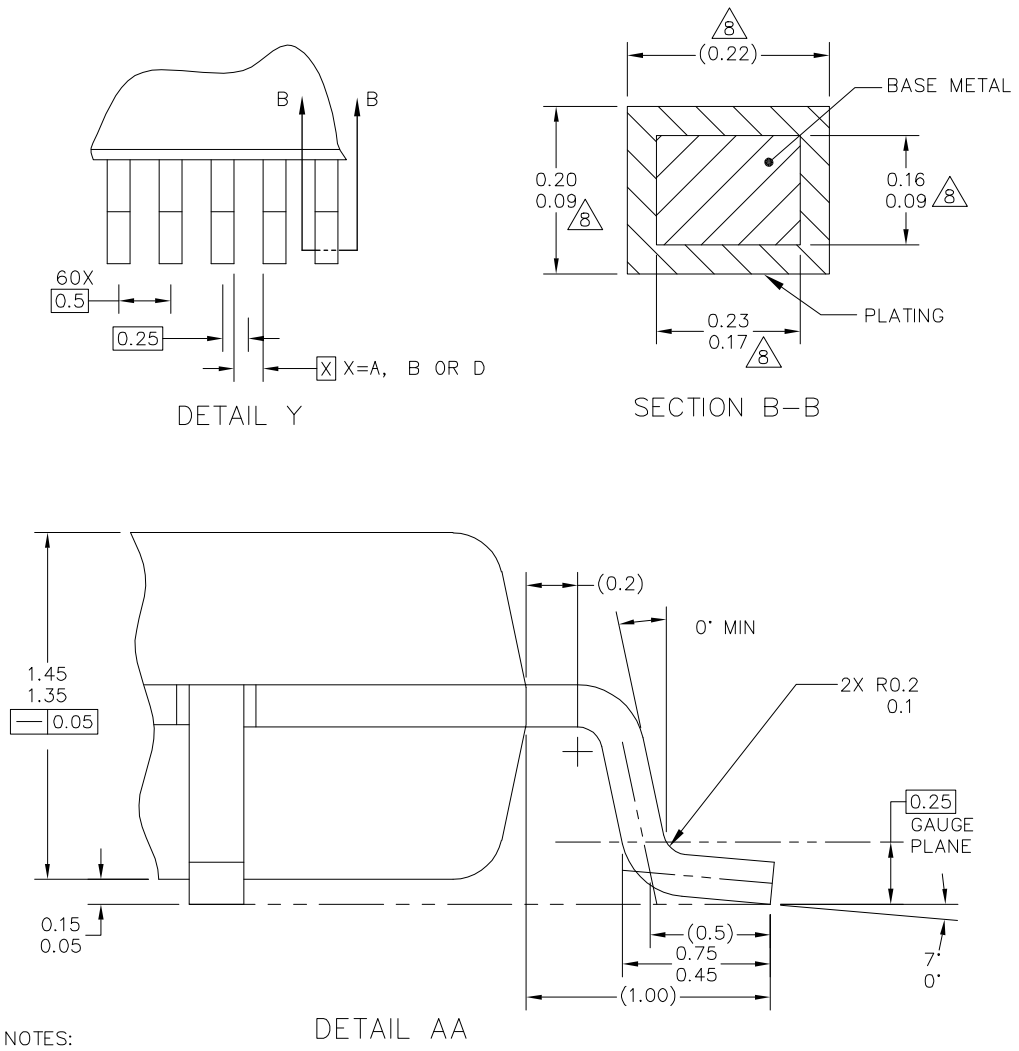


Figure 8. 64 LQFP Pinout Diagram

4.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

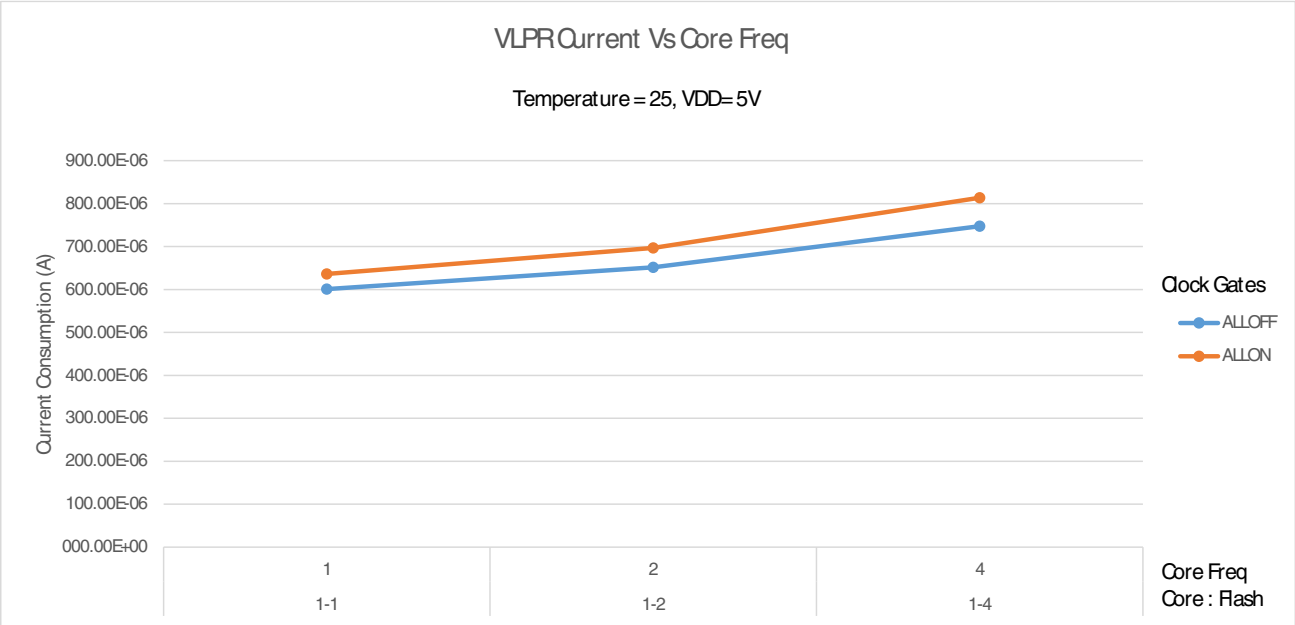


Figure 15. VLPR mode supply current vs. core frequency

5.3.1.7 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on http://www.nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3.2.4 AC specifications at 3.3 V range

Table 37. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	2.7		4	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	17.5	5	17	25
	28	9	32	50
High drive I/O pad	19	5	17	25
	26	9	33	50
CMOS Input [3]	4	1.2	3	0.5

1. Propagation delay measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.2.5 AC specifications at 5 V range

Table 38. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	4		5.5	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	12	3.6	10	25
	18	8	17	50
High drive I/O pad	13	3.6	10	25
	19	8	19	50
CMOS Input [3]	3	1.2	2.8	0.5

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

Table 40. Thermal characteristics for the 64-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	37	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	26	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	14	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.3 Thermal characteristics for the 100-pin LQFP package

Table 41. Thermal characteristics for the 100-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	59	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	46	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	49	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	40	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	31	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	16	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

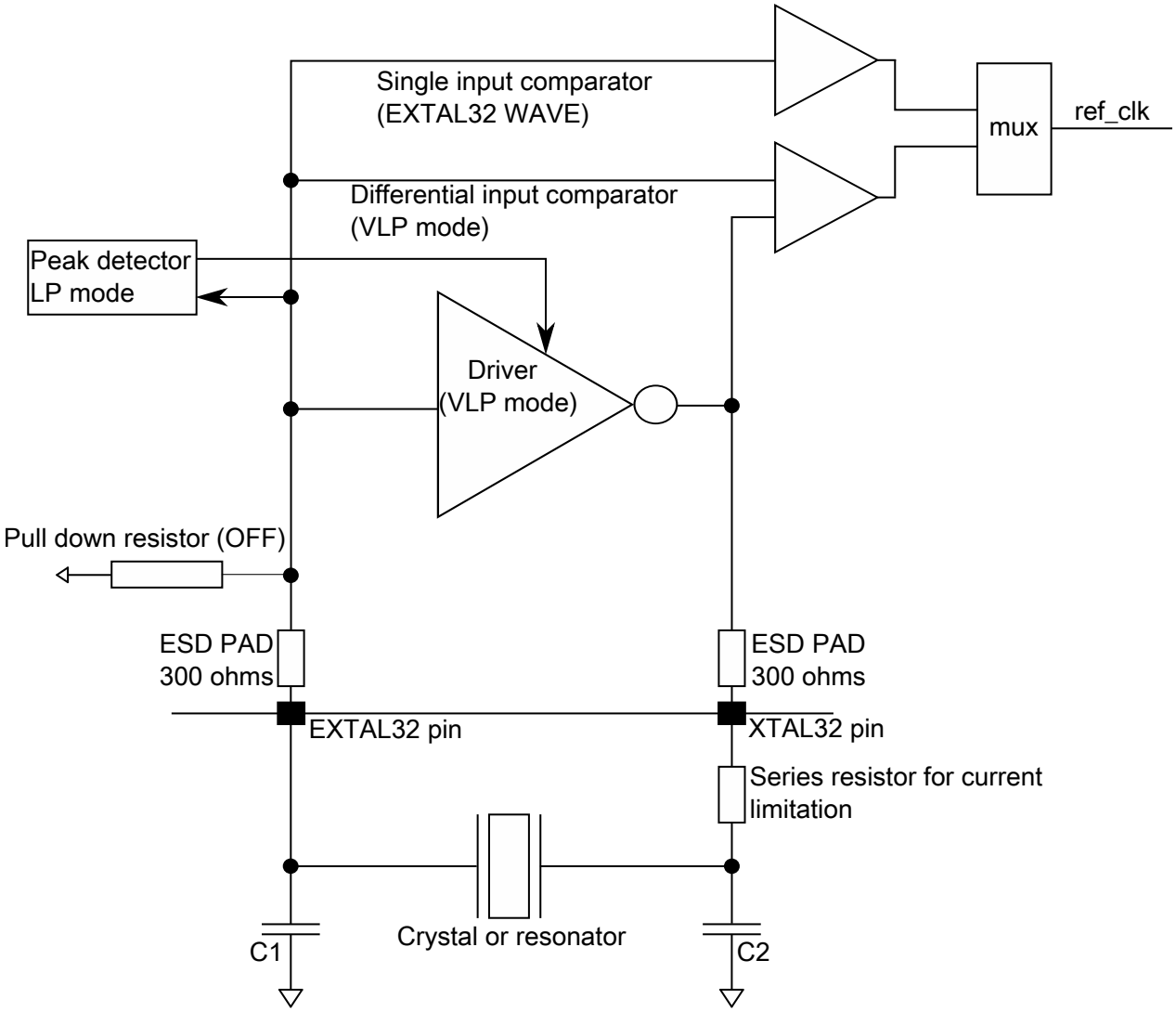


Figure 17. Oscillator connections scheme (OSC32)

Table 43. External Oscillator electrical specifications (OSC) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		2
C_2	XTAL load capacitance	—	—	—		2
R_F	Feedback resistor					3
	Low-frequency, high-gain mode (32 kHz)	—	10	—	MΩ	
	High-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	—	—	MΩ	
	High-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	1	—	MΩ	
R_S	Series resistor					
	Low-frequency, high-gain mode (32 kHz)	—	200	—		
	High-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
	High-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					4
	Low-frequency, high-gain mode	—	3.3	—	V	
	High-frequency, low-gain mode	—	1.0	—	V	
	High-frequency, high-gain mode	—	3.3	—	V	

1. Measured at V_{DD} = 5 V, Temperature = 25 °C
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. When low power mode is selected, R_F is integrated and must not be attached externally.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.1.2 External Oscillator frequency specifications

Table 44. External Oscillator frequency specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode	30	—	40	kHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	2000	—	ms	1

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

Table 45. External Oscillator frequency specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — Low Frequency, High Gain Mode	32	—	40	kHz	
f_{osc_me}	Oscillator crystal or resonator frequency — Medium Frequency	1	—	8	MHz	
f_{osc_hi}	Oscillator crystal or resonator frequency — High Frequency	8	—	32		
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz Low Frequency, High-Gain Mode	—	500	—	ms	1
	Crystal startup time — 8 MHz High Frequency, Low-Power Mode	—	1.5	—		
	Crystal startup time — 8 MHz High Frequency, High-Gain Mode	—	2.5	—		
	Crystal startup time — 40 MHz High Frequency, Low-Power Mode	—	2	—		
	Crystal startup time — 40 MHz High Frequency, High-Gain Mode	—	2.5	—		

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

5.4.2.2 System Clock Generation (SCG) specifications

5.4.2.2.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 46. Fast internal RC Oscillator electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	Fast internal reference frequency Trim range = 00 range = 01 (Note: 52/56 MHz are not trimmed) range = 10 (Note: 52/56 MHz are not trimmed) Trim range = 11	—	48 52 56 60	—	MHz
I_{VDD}	Supply current	—	400	500	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	F_{IRC}× (1-0.3)	—	F_{IRC}× (1+0.3)	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	±0.5	±1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		—	3	µs[2]
T_{JIT}	Period jitter (RMS)	—	35	150	ps

1. ΔF_{cl} is dependent on reference clock accuracy. For example, if locked to crystal oscillator, ΔF_{cl} is typically limited by trimming ability of the module itself; if locked to other clock source which has 3% accuracy, then ΔF_{cl} can only be ±3%.

5.4.3 Memories and memory interfaces

5.4.3.1 Flash memory module (FTFE) electrical specifications

This section describes the electrical characteristics of the flash memory module (FTFE).

5.4.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 50. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Flash Block high-voltage time for 32 KB	—	26	226	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.1.2 Flash timing specifications — commands

Table 51. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.3	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.8	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	28	240	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2

Table continues on the next page...

Table 51. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{pgmsec512}$	Program Section execution time (512B flash)	—	2.5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	250	2100	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	250	2100	ms	2
	Program Partition for EEPROM execution time					
$t_{pgmpart24k}$	• 24 KB EEPROM backup	—	69	—	ms	
$t_{pgmpart32k}$	• 32 KB EEPROM backup	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram24k}$	• 24 KB EEPROM backup	—	0.6	1.1	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
	Byte-write to FlexRAM execution time:					
$t_{eewr8b24k}$	• 24 KB EEPROM backup	—	370	1625	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
	16-bit write to FlexRAM execution time:					
$t_{eewr16b24k}$	• 24 KB EEPROM backup	—	370	1625	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b24k}$	• 24 KB EEPROM backup	—	600	1950	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 52. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.5.1.1 12-bit ADC operating conditions

Table 54. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	5.5	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		2.5	V_{DDA}	V_{DDA} + 100m	V	3
V_{REFL}	ADC reference voltage low		– 100	0	100	mV	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance		—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)		—	—	5	kΩ	4
f_{ADCK}	ADC conversion clock frequency		2	40	50	MHz	5, 6
C_{rate}	ADC conversion rate	No ADC hardware averaging[7] Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	8

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. Clock and compare cycle need to be set according the guidelines in the block guide.
6. ADC conversion will become less reliable above maximum frequency.
7. When using ADC hardware averaging, refer to the device *Reference Manual* to determine the most appropriate setting for AVGS.
8. Max ADC conversion rate of 1200 Ksps is with 10-bit mode

Table 55. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.[3]	Unit	Notes
	Sample Time		275	—	Refer to the device's *Reference Manual*	ns	
TUE	Total unadjusted error at 2.7 to 5.5 V		—	±4.5	±6.11	LSB[5]	6
DNL	Differential non-linearity at 2.7 to 5.5 V		—	±0.8	±1.07	LSB[5]	6
INL	Integral non-linearity at 2.7 to 5.5 V		—	±1.4	±3.54	LSB[5]	6
E_{FS}	Full-scale error at 2.7 to 5.5 V		—	–2	-3.60	LSB[5]	V_{ADIN} = V_{DDA}[6]
E_{ZS}	Zero-scale error at 2.7 to 5.5 V		—	–2.7	-4.24	LSB[5]	
E_Q	Quantization error at 2.7 to 5.5 V		—	—	±0.5	LSB[5]	
ENOB	Effective number of bits at 2.7 to 5.5 V		—	11.3	—	bits	7
SINAD	Signal-to-noise plus distortion at 2.7 to 5.5 V	See ENOB	—	70	—	dB	SINAD = 6.02 × ENOB + 1.76
E_{IL}	Input leakage error at 2.7 to 5.5 V		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
V_{TEMP_S}	Temp sensor slope at 2.7 to 5.5 V	Across the full temperature range of the device	1.492	1.564	1.636	mV/°C	8, 9
V_{TEMP25}	Temp sensor voltage at 2.7 to 5.5 V	25 °C	730	740.5	751	mV	8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

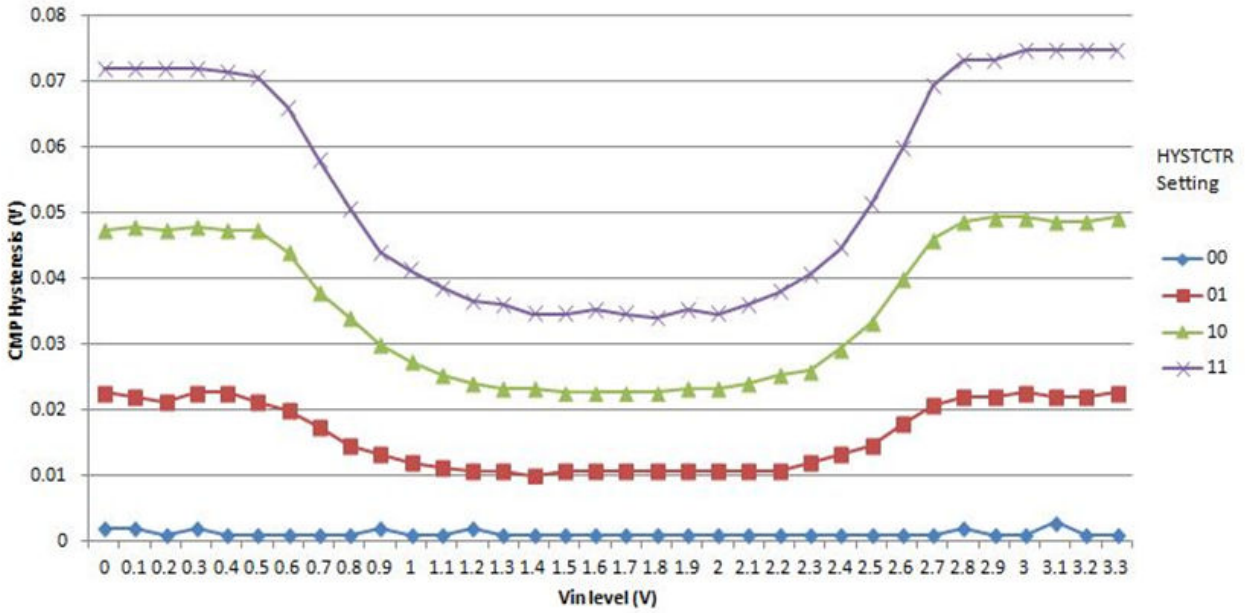


Figure 21. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

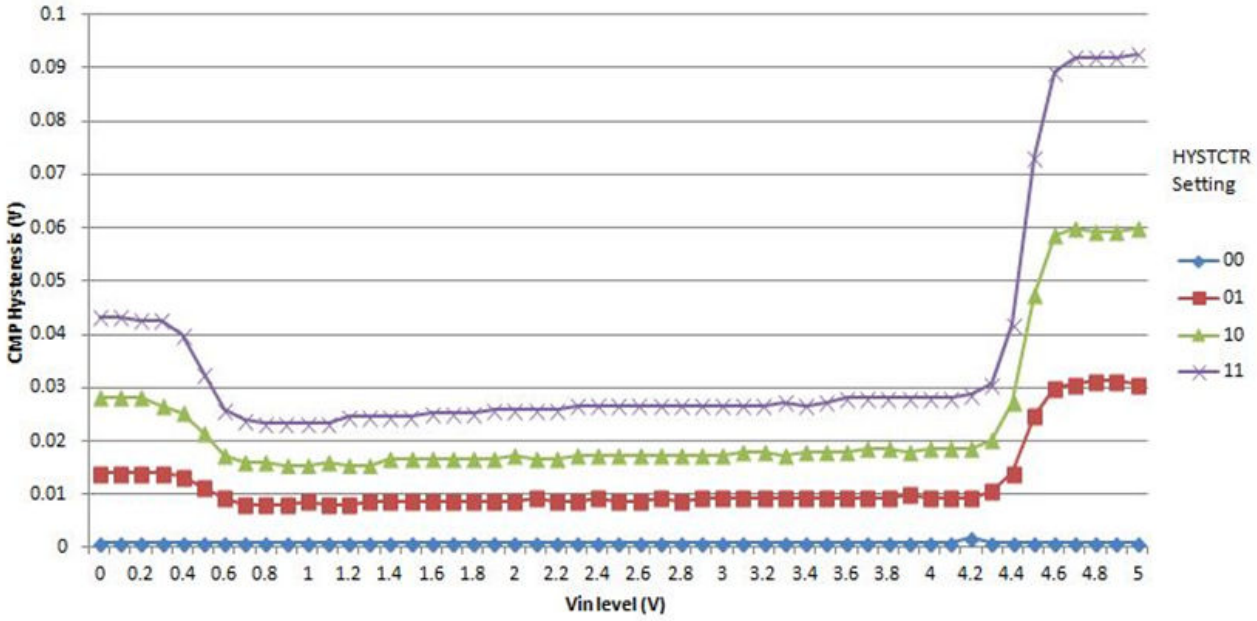


Figure 22. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)