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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	58
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	34K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke15z256vlh7

Clock interfaces

- 3 - 40 MHz fast external oscillator (OSC)
- 32 kHz slow external oscillator (OSC32)
- 48 - 60 MHz high-accuracy (up to 1%) fast internal reference clock (FIRC) for normal Run
- 8 MHz / 2 MHz high-accuracy (up to 3%) slow internal reference clock (SIRC) for low-speed Run
- 128 kHz low power oscillator (LPO)
- Low-power FLL (LPFLL)
- Up to 60 MHz DC external square wave input clock
- System clock generator (SCG)
- Real time counter (RTC)

Power management

- Low-power ARM Cortex-M0+ core with excellent energy efficiency
- Power management controller (PMC) with multiple power modes: Run, Wait, Stop, VLPR, VLPW and VLPS
- Supports clock gating for unused modules, and specific peripherals remain working in low power modes
- POR, LVD/LVR

Connectivity and communications interfaces

- 3× low-power universal asynchronous receiver/ transmitter (LPUART) modules with DMA support and low power availability
- 2× low-power serial peripheral interface (LPSPI) modules with DMA support and low power availability
- 2× low-power inter-integrated circuit (LPI2C) modules with DMA support and low power availability
- FlexIO module for flexible and high performance serial interfaces

Debug functionality

- Serial Wire Debug (SWD) debug interface
- Debug Watchpoint and Trace (DWT)
- Micro Trace Buffer (MTB)

Operating Characteristics

- Voltage range: 2.7 to 5.5 V
- Ambient temperature range: –40 to 105 °C

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KE1xZ256PB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KE1xZP100M72SF0RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document: KE1xZP100M72SF0
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_E_1N36S [1]
Package drawing	Package dimensions are provided in package drawings.	100-LQFP: 98ASS23308W 64-LQFP: 98ASS23234W

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

Table of Contents

- All data movement via dual-address transfers: read from source, write to destination
- 8-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Channel activation via one of three methods
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.2 FTM

This device contains three FlexTimer modules.

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

Several key enhancements of this module are made:
- Signed up counter
- Deadtime insertion hardware
- Fault control inputs
- Enhanced triggering functionality
- Initialization and polarity control

2.2.3 ADC

This device contains two 12-bit SAR ADC modules. The ADC module supports hardware triggers from FTM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:
- Linear successive approximation algorithm with up to 12-bit resolution
- Up to 16 single-ended external analog inputs
- Support 12-bit, 10-bit, and 8-bit single-ended output modes

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	7	VDD	VDD	VDD							
11	8	VDDA	VDDA	VDDA							
12	9	VREFH	VREFH	VREFH							
13	—	VREFL	VREFL	VREFL							
14	—	VSS	VSS	VSS							
15	11	PTB7	EXTAL	EXTAL	PTB7	LPI2C0_SCL					
16	12	PTB6	XTAL	XTAL	PTB6	LPI2C0_SDA					
17	—	PTE14	DISABLED		PTE14	FTM0_FLT1					
18	13	PTE3	TSI0_CH24	TSI0_CH24	PTE3	FTM0_FLT0	LPUART2_ RTS			TRGMUX_IN6	
19	—	PTE12	DISABLED		PTE12	FTM0_FLT3	LPUART2_TX				
20	—	PTD17	DISABLED		PTD17	FTM0_FLT2	LPUART2_RX				
21	14	PTD16	DISABLED		PTD16	FTM0_CH1					
22	15	PTD15	DISABLED		PTD15	FTM0_CH0					
23	16	PTE9	DAC0_OUT	DAC0_OUT	PTE9	FTM0_CH7	LPUART2_ CTS				
24	—	PTD14	DISABLED		PTD14						CLKOUT
25	—	PTD13	DISABLED		PTD13						RTC_CLKOUT
26	17	PTE8	ACMP0_IN3/ TSI0_CH11	ACMP0_IN3/ TSI0_CH11	PTE8	FTM0_CH6					
27	18	PTB5	TSI0_CH9	TSI0_CH9	PTB5	FTM0_CH5	LPSPI0_PCS1			TRGMUX_IN0	ACMP1_OUT
28	19	PTB4	ACMP1_IN2/ TSI0_CH8	ACMP1_IN2/ TSI0_CH8	PTB4	FTM0_CH4	LPSPI0_SOUT			TRGMUX_IN1	
29	20	PTC3	ADC0_SE11/ ACMP0_IN4/ EXTAL32	ADC0_SE11/ ACMP0_IN4/ EXTAL32	PTC3	FTM0_CH3					
30	21	PTC2	ADC0_SE10/ ACMP0_IN5/ XTAL32	ADC0_SE10/ ACMP0_IN5/ XTAL32	PTC2	FTM0_CH2					
31	22	PTD7	TSI0_CH10	TSI0_CH10	PTD7	LPUART2_TX		FTM2_FLT3			
32	23	PTD6	TSI0_CH7	TSI0_CH7	PTD6	LPUART2_RX		FTM2_FLT2			
33	24	PTD5	TSI0_CH6	TSI0_CH6	PTD5	FTM2_CH3	LPTMR0_ ALT2		PWT_IN2	TRGMUX_IN7	
34	—	PTD12	DISABLED		PTD12	FTM2_CH2	LPI2C1_HREQ			LPUART2_ RTS	
35	—	PTD11	DISABLED		PTD11	FTM2_CH1	FTM2_QD_ PHA			LPUART2_ CTS	
36	—	PTD10	DISABLED		PTD10	FTM2_CH0	FTM2_QD_ PHB				
37	—	VSS	VSS	VSS							
38	—	VDD	VDD	VDD							
39	25	PTC1	ADC0_SE9/ ACMP1_IN3/ TSI0_CH23	ADC0_SE9/ ACMP1_IN3/ TSI0_CH23	PTC1	FTM0_CH1					

4.3.1 Core Modules

Table 7. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock	I
SWD_DIO	SWD_DIO	Serial Wire Data	I/O

4.3.2 System Modules

Table 8. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.	I
RESET_b	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 9. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_IN is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

4.3.3 Clock Modules

Table 10. OSC (in SCG) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL	EXTAL	External clock/Oscillator input	I
XTAL	XTAL	Oscillator output	O

Table 11. RTC Oscillator (OSC32) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

4.3.4 Analog

Table 12. ADC*0* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC*0*_SE[15:0]	AD[15:0]	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I

Table 13. ADC*1* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC*1*_SE[11:0]	AD[11:0]	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I

Table 14. ACMP*0* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*0*_IN[5:0]	IN[5:0]	Analog voltage inputs	I
ACMP*0*_OUT	CMPO	Comparator output	O
DAC0_OUT	—	DAC output	O

Table 15. ACMP*1* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*1*_IN[5:0]	IN[5:0]	Analog voltage inputs	I
ACMP*1*_OUT	CMPO	Comparator output	O

4.3.7 Human-Machine Interfaces (HMI)

Table 25. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[17:0]	PORTA17–PORTA0	General-purpose input/output	I/O
PTB[17:0]	PORTB17–PORTB0	General-purpose input/output	I/O
PTC[17:0]	PORTC17–PORTC0	General-purpose input/output	I/O
PTD[17:0]	PORTD17–PORTD0	General-purpose input/output	I/O
PTE[16:0]	PORTE16–PORTE0	General-purpose input/output	I/O

Table 26. TSI0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TSI0_CH[24:0]	TSI[24:0]	TSI sensing pins or GPIO pins	I/O

4.4 Pinout diagram

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous table of Pin Assignments.

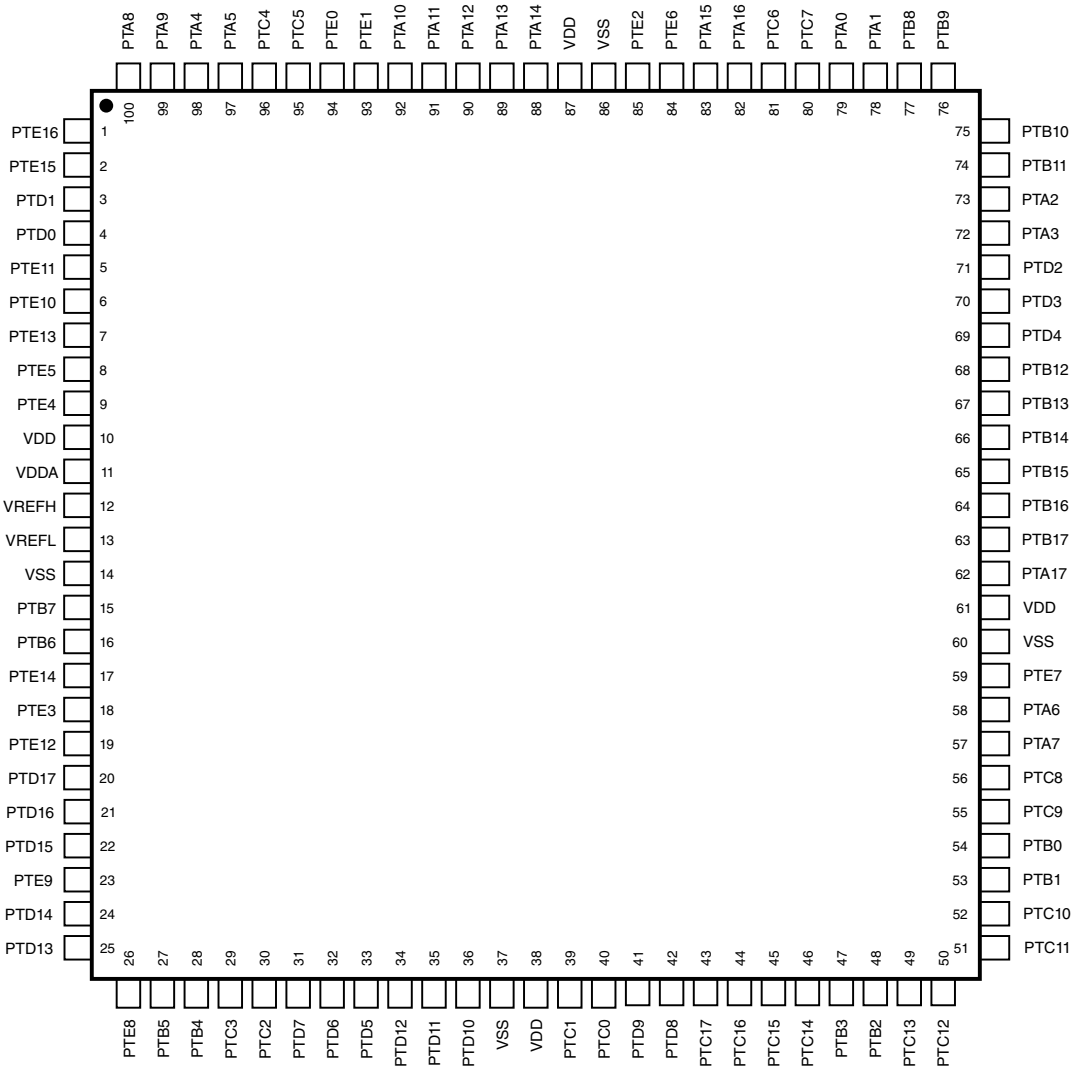


Figure 7. 100 LQFP Pinout Diagram

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 34. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

5.3.2 Switching specifications

5.3.2.1 Device clock specifications

Table 35. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	48	MHz	
VLPR / VLPW mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	13	MHz	

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.3 Thermal specifications

5.3.3.1 Thermal operating requirements

Table 39. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

5.3.3.2 Thermal attributes

5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.3.3.2.2 Thermal characteristics for the 64-pin LQFP package

Table 40. Thermal characteristics for the 64-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	62	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	44	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	50	°C/W

Table continues on the next page...

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

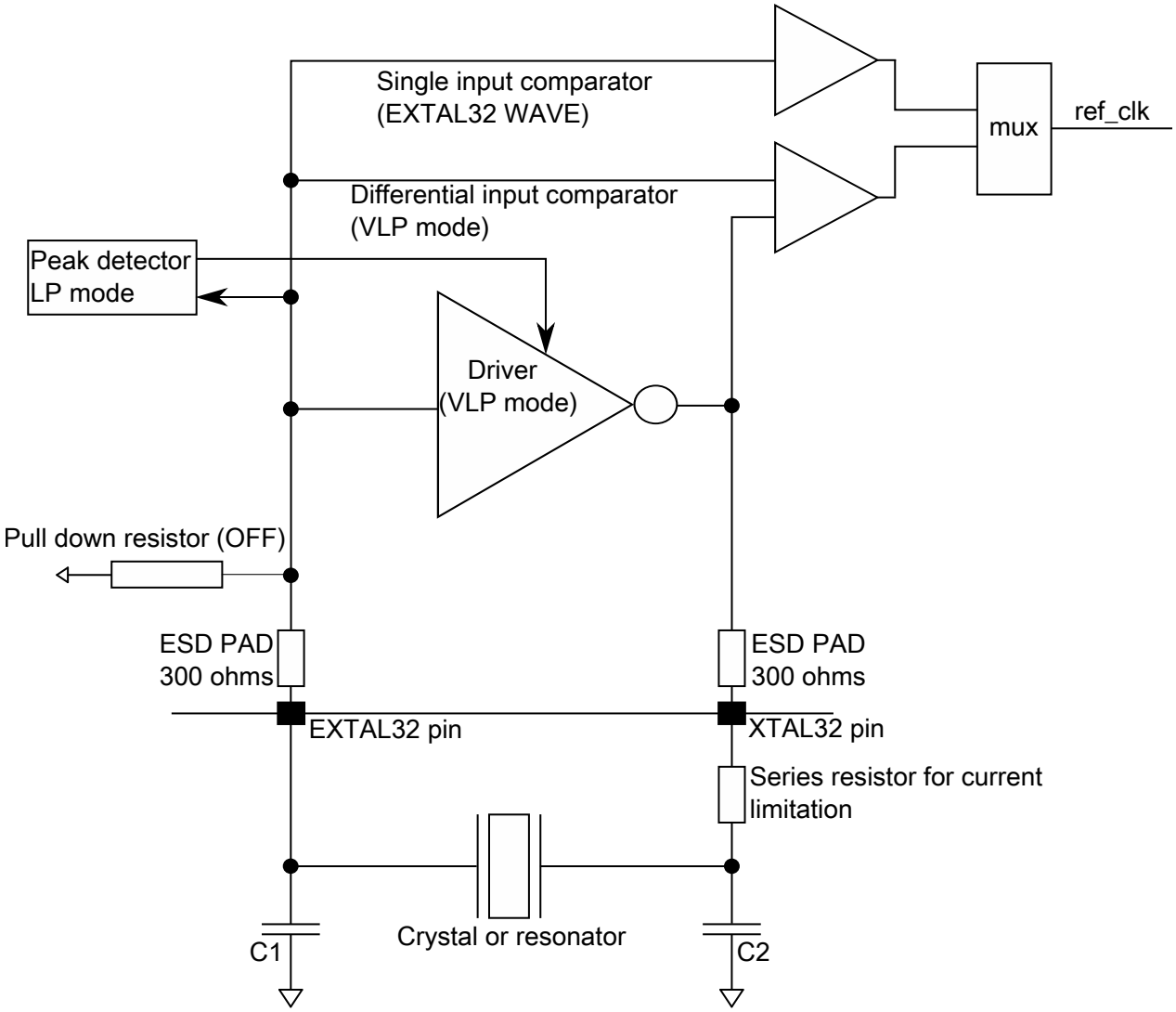
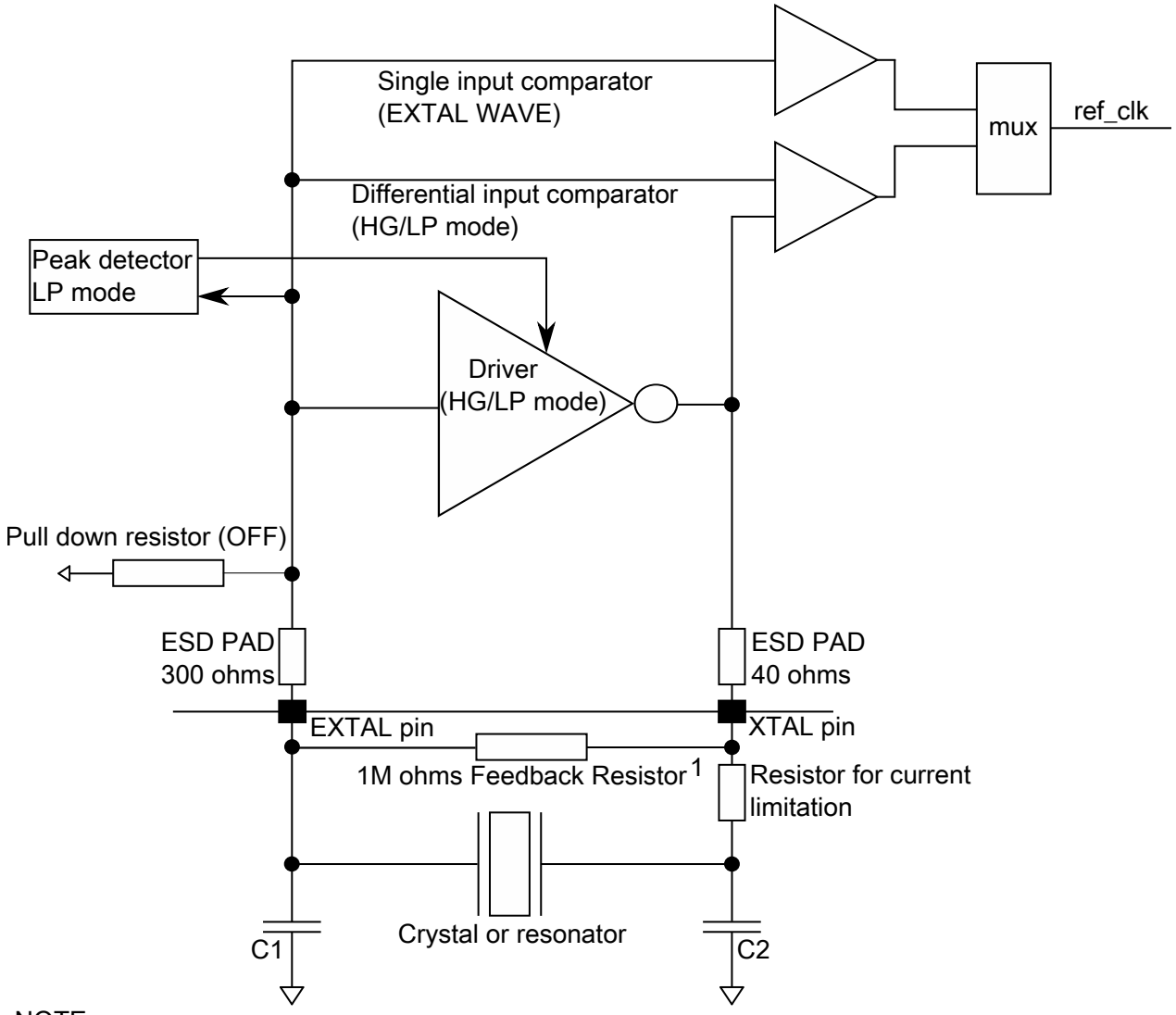


Figure 17. Oscillator connections scheme (OSC32)



NOTE:

1. 1M Feedback resistor is needed only for HG mode.

Figure 18. Oscillator connections scheme (OSC)

NOTE

Data values in the following "External Oscillator electrical specifications" tables are from simulation.

Table 42. External Oscillator electrical specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current	—	25	—	µA	1
g_{mXOSC}	Oscillator transconductance	6	—	9	µA/V	
V_{EXTAL}	EXTAL32 input voltage — external clock mode	0	—	3.6	V	

Table continues on the next page...

5.4.3.1.4 Reliability specifications

Table 53. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree1k}$	• EEPROM backup to FlexRAM ratio = 1,024	10 M	25 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

5.4.5.2 CMP with 8-bit DAC electrical specifications

Table 56. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit
V_{DD}	Supply voltage	2.7	—	5.5	V
I_{DDHS}	Supply current, High-speed mode[2]				µA
	within ambient temperature range	—	145	200	
I_{DDLS}	Supply current, Low-speed mode[2]				µA
	within ambient temperature range	—	5	10	
V_{AIN}	Analog input voltage	0	0 - V_{DDX}	V_{DDX}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	within ambient temperature range	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	within ambient temperature range	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[3]				ns
	within ambient temperature range	—	30	200	
t_{DLSB}	Propagation delay, Low-speed mode[3]				µs
	within ambient temperature range	—	0.5	2	
t_{DHSS}	Propagation delay, High-speed mode[4]				ns
	within ambient temperature range	—	70	400	
t_{DLSS}	Propagation delay, Low-speed mode[4]				µs
	within ambient temperature range	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode [3]				µs
	within ambient temperature range	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[3]				µs
	within ambient temperature range	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0 (V_{AIO})				mV
	within ambient temperature range	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	within ambient temperature range	—	16	53	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	within ambient temperature range	—	11	30	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	within ambient temperature range	—	32	90	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	within ambient temperature range	—	22	53	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV

Table continues on the next page...

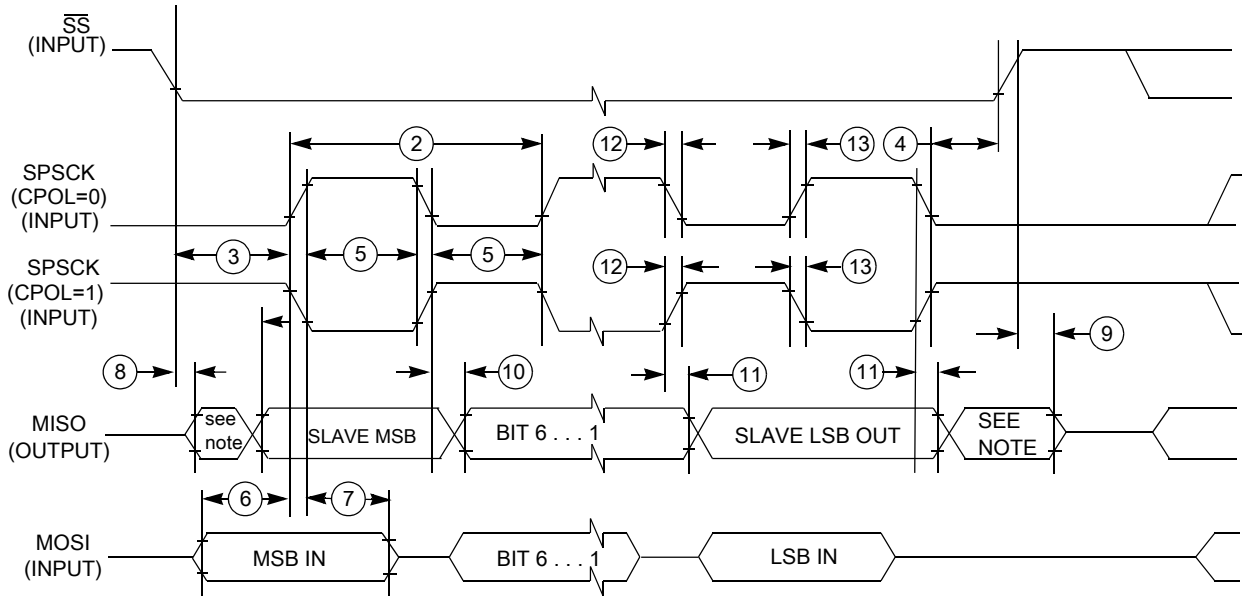


Figure 26. LPSPI slave mode timing (CPHA = 0)

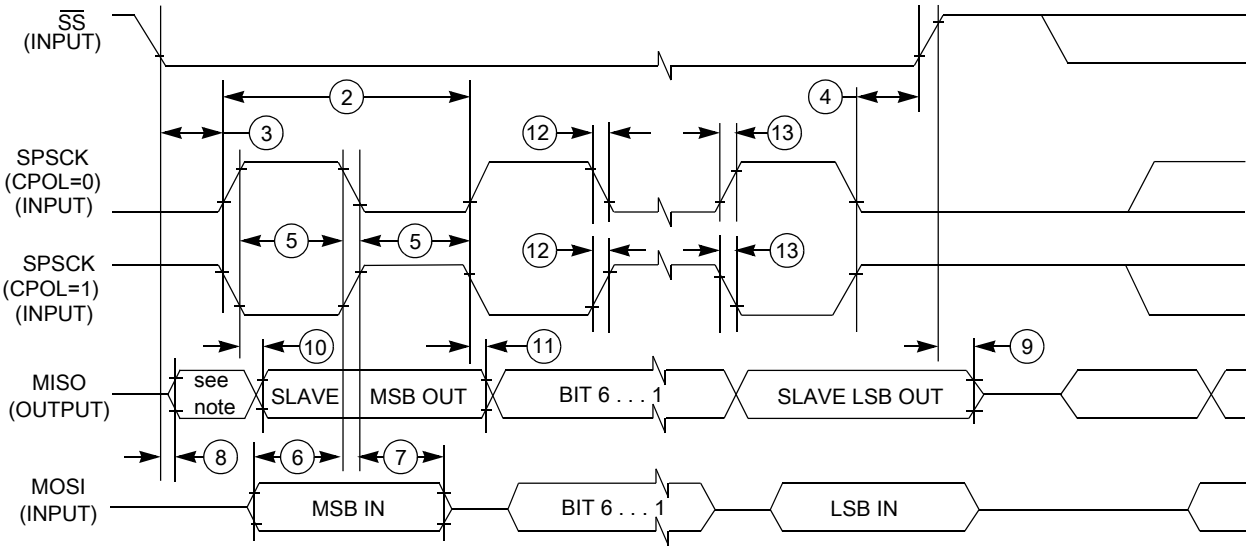


Figure 27. LPSPI slave mode timing (CPHA = 1)

5.4.6.3 LPI^{2}C

Table 59. LPI^{2}C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1, 2, 3
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		Ultra Fast mode (UFm)	0	5000		
		High speed mode (Hs-mode)	0	3400		

1. Hs-mode is only supported in slave mode.
2. The maximum SCL clock frequency in Fast mode with maximum bus loading (400pF) can only be achieved with appropriate pull-up devices on the bus when using the high or normal drive pins across the full voltage range . The maximum SCL clock frequency in Fast mode Plus can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. The maximum SCL clock frequency in Ultra Fast mode can support maximum bus loading (400pF) when using the high drive pins. The maximum SCL clock frequency for slave in High speed mode can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. For more information on the required pull-up devices, see I^2C Bus Specification.
3. See General switching specifications

5.4.7 Human-machine interfaces (HMI)

5.4.7.1 Touch sensing input (TSI) electrical specifications

Table 60. TSI electrical specifications

Symbol	Description	Value			Unit
		Min	Typ	Max	
I_{DD_EN}	Power consumption in operation mode	—	500	600	µA
I_{DD_DIS}	Power consumption in disable mode	—	20	355	nA
V_{BG}	Internal bandgap reference voltage	—	1.21	—	V
V_{PRE}	Internal bias voltage	—	1.51	—	V
C_I	Internal integration capacitance	—	90	—	pF
F_{CLK}	Internal main clock frequency	—	16	—	MHz

5.4.8 Debug modules

5.4.8.1 SWD electricals

Table 61. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
S1	SWD_CLK frequency of operation	0	25	MHz

Table continues on the next page...

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is a pseudo open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

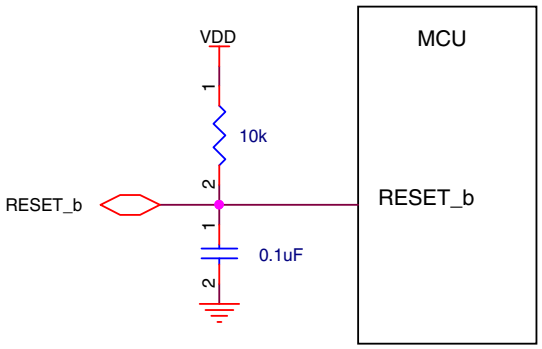


Figure 32. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

Table 63. Part number fields description (continued)

Field	Description	Values
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 7 = 72 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKE15Z256VLL7

8 Revision history

The following table provides a revision history for this document.

Table 64. Revision history

Rev. No.	Date	Substantial Changes
2	09/2016	Initial public release.

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