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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	89
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	34K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke15z256vll7

2.1.1 ARM Cortex-M0+ core

The enhanced ARM Cortex M0+ is the member of the Cortex-M Series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 4 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 2 bits. It also differs in number of interrupt sources and supports 32 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency to up to 15 clock cycles for Cortex-M0+. It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

Table 2. AWIC Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	RESET pin, WDOG , loss of clock(LOC) reset and loss of lock (LOL) reset
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	ADCx is optional functional with clock source from SIRC or OSC
CMPx	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPI2C	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPUART	Functional in Stop/VLPS modes with clock source from SIRC or OSC

Table continues on the next page...

Table 5. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, LPIT, FlexIO, LPUART, LPI2C,LPSPI, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.

2.1.9 Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD interface.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 8 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

2.2.4 CMP

There are two analog comparators on this device.

- Each CMP has its own independent 8-bit DAC.
- Each CMP supports up to 6 analog inputs from external pins.
- Each CMP is able to convert an internal reference from the bandgap.
- Each CMP supports the round-robin sampling scheme. In summary, this allow the CMP to operate independently in VLPS and Stop modes, whilst being triggered periodically to sample up to 8 inputs. Only if an input changes state is a full wakeup generated.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising and falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, windowed, or digitally filtered

2.2.13 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/ Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer
- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.14 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

NOTE

The RESET_b pin is also a normal I/O pad with pseudo open-drain.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
40	26	PTC0	ADC0_SE8/ ACMP1_IN4/ TSI0_CH22	ADC0_SE8/ ACMP1_IN4/ TSI0_CH22	PTC0	FTM0_CH0					
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3			
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2			
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13	ADC0_SE13	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12	ADC0_SE12	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7/ TSI0_CH21	ADC0_SE7/ TSI0_CH21	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6/ TSI0_CH20	ADC0_SE6/ TSI0_CH20	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13						
50	—	PTC12	DISABLED		PTC12						
51	—	PTC11	DISABLED		PTC11						
52	—	PTC10	DISABLED		PTC10						
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	DISABLED		PTC9	LPUART1_TX				LPUART0_ RTS	
56	36	PTC8	DISABLED		PTC8	LPUART1_RX				LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	DISABLED		PTE7	FTM0_CH7					
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6		EWM_OUT_b			
63	—	PTB17	DISABLED		PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	DISABLED		PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	DISABLED		PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1					
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0					
69	44	PTD4	ADC1_SE6	ADC1_SE6	PTD4	FTM0_FLT3					
70	45	PTD3	NMI_b	ADC1_SE3	PTD3		LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2		LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3		LPI2C0_SCL	EWM_IN		LPUART0_TX	

4.3.7 Human-Machine Interfaces (HMI)

Table 25. GPIO Signal Descriptions

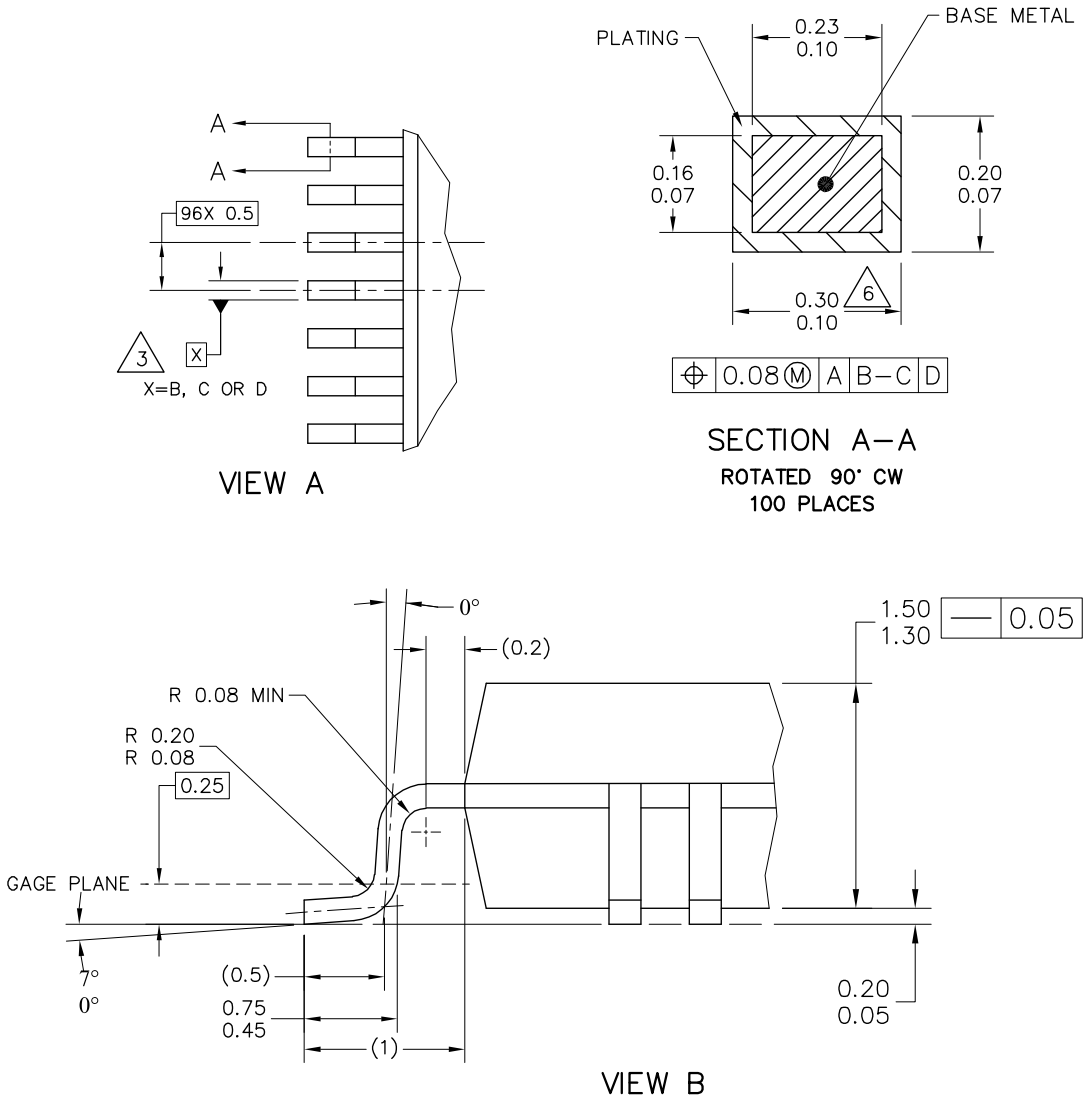
Chip signal name	Module signal name	Description	I/O
PTA[17:0]	PORTA17–PORTA0	General-purpose input/output	I/O
PTB[17:0]	PORTB17–PORTB0	General-purpose input/output	I/O
PTC[17:0]	PORTC17–PORTC0	General-purpose input/output	I/O
PTD[17:0]	PORTD17–PORTD0	General-purpose input/output	I/O
PTE[16:0]	PORTE16–PORTE0	General-purpose input/output	I/O

Table 26. TSI0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TSI0_CH[24:0]	TSI[24:0]	TSI sensing pins or GPIO pins	I/O

4.4 Pinout diagram

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous table of Pin Assignments.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.
5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 10. 100-pin LQFP package dimensions 2

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 6000	6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature upper limit	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Table 27. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	2.7	5.5	V
I_{DD}	Digital supply current	—	60	mA
V_{IO}	IO pin input voltage	V_{SS} – 0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.1	V_{DD} + 0.1	V

5.3 General

5.3.1 Nonswitching electrical specifications

5.3.1.1 Voltage and current operating requirements

Table 28. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	– 0.1	0.1	V	
I_{ICIO}	Analog DC injection current — single pin				
	$V_{IN} < V_{SS}$ - 0.3 V (Negative current injection)	– 5	—	mA	1, 2
	$V_{IN} > V_{DD}$ + 0.3 V (Positive current injection)	—	+ 5	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	– 25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	3

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
2. Max voltage levels that I/O pins can withstand while keeping the injection current (maximum) at 5mA:
   - Max supply V_{DD} = 6.0 V for 60 s lifetime (with no switching restrictions) or for 10 hours (if device is in reset or no switching state)
   - Max I/O pin voltage = 6.5 V (at injection current ≤ 5 mA) or 7.0 V (at injection current > 5 mA)
3. Open drain outputs must be pulled to V_{DD}.

5.3.1.2 DC electrical specifications at 3.3 V Range and 5.0 V Range

Table 29. DC electrical specifications

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{DD}	I/O Supply Voltage [1] @ V_{DD} = 3.3 V	2.7	3.3	4	V	
	@ V_{DD} = 5.0 V	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage @ V_{DD} = 3.3 V	0.7 × V_{DD}	—	V_{DD} + 0.3	V	
	@ V_{DD} = 5.0 V	0.65 × V_{DD}	—	V_{DD} + 0.3	V	

Table continues on the next page...

Table 29. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range @ V_{DD} = 3.3 V					8, 7
	All pins other than high drive port pins	—	0.002	0.5	µA	
	High drive port pins	—	0.004	0.5	µA	
	Input leakage current (per pin) for full temperature range @ V_{DD} = 5.5 V					
	All pins other than high drive port pins	—	0.005	0.5	µA	
	High drive port pins	—	0.010	0.5	µA	
R_{PU}	Internal pull-up resistors @ V_{DD} = 3.3 V	20	—	65	kΩ	9
	@ V_{DD} = 5.0 V	20	—	50	kΩ	
R_{PD}	Internal pull-down resistors @ V_{DD} = 3.3 V	20	—	65	kΩ	10
	@ V_{DD} = 5.0 V	20	—	50	kΩ	

1. Max power supply ramp rate is 500 V/ms.
2. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_5 value given above.
3. The 20 mA I/O pin is capable of switching a 50 pF load at up to 40 MHz.
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_5 value given above.
5. Refers to the current that leaks into the core when the pad is in Hi-Z (Off state).
6. Maximum pin leakage current at the ambient temperature upper limit.
7. PTD0, PTD1, PTD15, PTD16, PTB4, PTB5, PTE0 and PTE1 I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
8. Refers to the pin leakage on the GPIOs when they are OFF.
9. Measured at V_{DD} supply voltage = V_{DD} min and input V = V_{SS}
10. Measured at V_{DD} supply voltage = V_{DD} min and input V = V_{DD}

Table 33. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Unit
			Core@72MHz, bus @24MHz, flash @24MHz, VDD=5V					
		LPFLL	Running CoreMark in Flash all peripheral clock disabled. Core@72MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	12.15	12.41	
				105 °C	—	12.67	12.99	
		LPFLL	Running CoreMark in Flash, all peripheral clock enabled. Core@72MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	13.53	13.82	
				105 °C	—	14.07	14.43	
		LPFLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@72MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	8.81	9.00	
				105 °C	—	9.26	9.49	
		LPFLL	Running While(1) loop in Flash all peripheral clock enabled. Core@72MHz , bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	10.22	10.44	
				105 °C	—	10.67	10.94	
		IRC48M	Running CoreMark in Flash in **Compute Operation** mode. Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	8.50	8.69	
				105 °C	—	8.88	9.08	
		IRC48M	Running CoreMark in Flash all peripheral clock disabled. Core@48MHz, bus @24MHz, flash @24MHz, VDD=5V	25 °C	—	9.37	9.58	
				105 °C	—	9.76	9.98	
		IRC48M	Running CoreMark in Flash, all peripheral clock enabled. Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	10.51	10.75	
				105 °C	—	10.90	11.15	
		IRC48M	Running While(1) loop in Flash, all peripheral clock disabled. Core@48MHz, bus@24MHz, flash @24MHz, VDD=5V	25 °C	—	7.00	7.16	
				105 °C	—	7.41	7.58	
VLPR	I_{DD_VLPR}	IRC8M	Very Low Power Run Core Mark in Flash in **Compute Operation** mode. Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	1070	1136	µA
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock disabled. Core@4MHz, bus @1MHz, flash @1MHz, VDD=5V	25 °C	—	1110	1178	

Table continues on the next page...

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 34. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

5.3.2 Switching specifications

5.3.2.1 Device clock specifications

Table 35. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus clock	—	24	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	48	MHz	
VLPR / VLPW mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	1	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	13	MHz	

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

5.3.2.4 AC specifications at 3.3 V range

Table 37. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	2.7		4	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	17.5	5	17	25
	28	9	32	50
High drive I/O pad	19	5	17	25
	26	9	33	50
CMOS Input [3]	4	1.2	3	0.5

1. Propagation delay measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.2.5 AC specifications at 5 V range

Table 38. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	4		5.5	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	12	3.6	10	25
	18	8	17	50
High drive I/O pad	13	3.6	10	25
	19	8	19	50
CMOS Input [3]	3	1.2	2.8	0.5

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

5.4.3.1.4 Reliability specifications

Table 53. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree1k}$	• EEPROM backup to FlexRAM ratio = 1,024	10 M	25 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

Table 55. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.[3]	Unit	Notes
	Sample Time		275	—	Refer to the device's *Reference Manual*	ns	
TUE	Total unadjusted error at 2.7 to 5.5 V		—	±4.5	±6.11	LSB[5]	6
DNL	Differential non-linearity at 2.7 to 5.5 V		—	±0.8	±1.07	LSB[5]	6
INL	Integral non-linearity at 2.7 to 5.5 V		—	±1.4	±3.54	LSB[5]	6
E_{FS}	Full-scale error at 2.7 to 5.5 V		—	–2	-3.60	LSB[5]	V_{ADIN} = V_{DDA}[6]
E_{ZS}	Zero-scale error at 2.7 to 5.5 V		—	–2.7	-4.24	LSB[5]	
E_Q	Quantization error at 2.7 to 5.5 V		—	—	±0.5	LSB[5]	
ENOB	Effective number of bits at 2.7 to 5.5 V		—	11.3	—	bits	7
SINAD	Signal-to-noise plus distortion at 2.7 to 5.5 V	See ENOB	—	70	—	dB	SINAD = 6.02 × ENOB + 1.76
E_{IL}	Input leakage error at 2.7 to 5.5 V		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
V_{TEMP_S}	Temp sensor slope at 2.7 to 5.5 V	Across the full temperature range of the device	1.492	1.564	1.636	mV/°C	8, 9
V_{TEMP25}	Temp sensor voltage at 2.7 to 5.5 V	25 °C	730	740.5	751	mV	8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

1. Hs-mode is only supported in slave mode.
2. The maximum SCL clock frequency in Fast mode with maximum bus loading (400pF) can only be achieved with appropriate pull-up devices on the bus when using the high or normal drive pins across the full voltage range . The maximum SCL clock frequency in Fast mode Plus can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. The maximum SCL clock frequency in Ultra Fast mode can support maximum bus loading (400pF) when using the high drive pins. The maximum SCL clock frequency for slave in High speed mode can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. For more information on the required pull-up devices, see I^2C Bus Specification.
3. See General switching specifications

5.4.7 Human-machine interfaces (HMI)

5.4.7.1 Touch sensing input (TSI) electrical specifications

Table 60. TSI electrical specifications

Symbol	Description	Value			Unit
		Min	Typ	Max	
I_{DD_EN}	Power consumption in operation mode	—	500	600	µA
I_{DD_DIS}	Power consumption in disable mode	—	20	355	nA
V_{BG}	Internal bandgap reference voltage	—	1.21	—	V
V_{PRE}	Internal bias voltage	—	1.51	—	V
C_I	Internal integration capacitance	—	90	—	pF
F_{CLK}	Internal main clock frequency	—	16	—	MHz

5.4.8 Debug modules

5.4.8.1 SWD electricals

Table 61. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
S1	SWD_CLK frequency of operation	0	25	MHz

Table continues on the next page...

Table 61. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

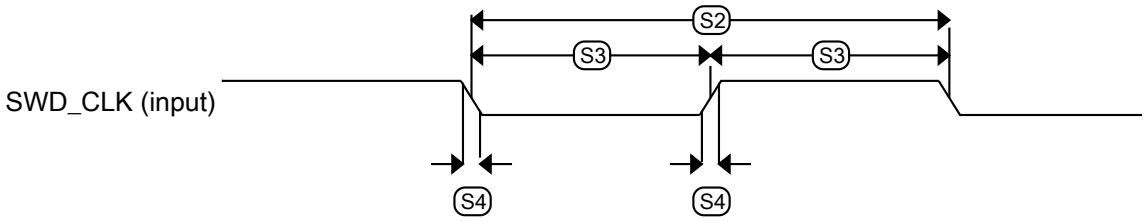


Figure 28. Serial wire clock input timing

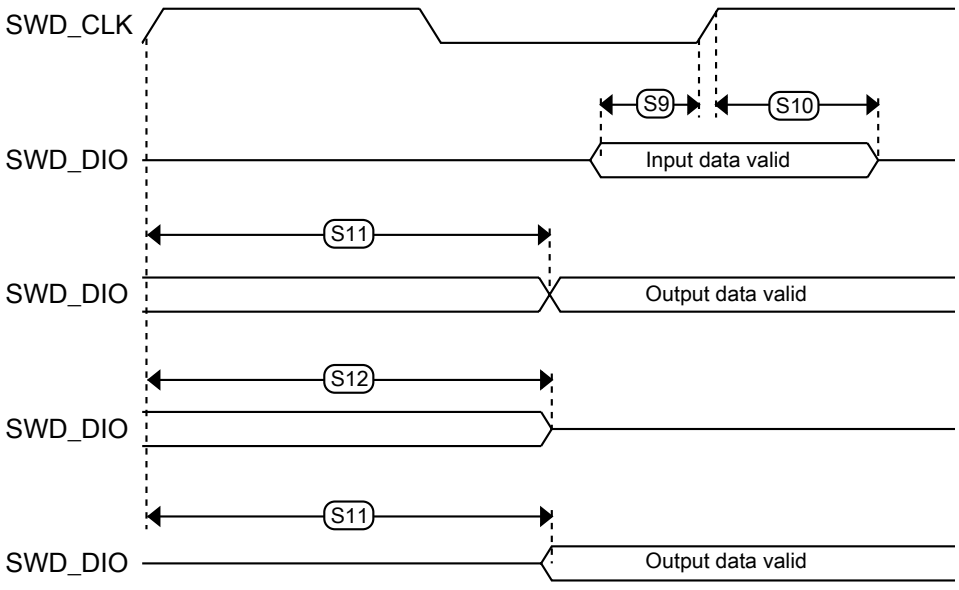


Figure 29. Serial wire data timing

6 Design considerations

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.nxp.com/kds
- Partner IDEs: http://www.nxp.com/kide

Run-time Software

- Kinetis SDK: http://www.nxp.com/ksdk
- Kinetis Bootloader: http://www.nxp.com/kboot
- ARM mbed Development Platform: http://www.nxp.com/mbed

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 63. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE15, KE14
A	Key attribute	• Z = Cortex-M0+

Table continues on the next page...

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