Renesas Electronics America Inc - R5F21366CNFA#W4 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21366cnfa-w4

Table 1.2 Specifications for R8C/36C Group (2)

Item	Function	Specification
Timer	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 (with 2 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I^2C mode (I^2C bus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I^2C bus)
I^2C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution × 2 circuits
Comparator B		2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance:10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current consumption		Typ. 7.0 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		−20 to 85°C (N version) −40 to 85°C (D version) (1)
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin TQFP • Package code: PTQP0064LB-A

Note:
1. Specify the D version if D version functions are to be used.

1.2 Product List

Tables 1.3 and 1.4 list Product List for R8C/36C Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/36C Group.

Table 1.3 Product List for R8C/36C Group (1) Current of Nov 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21364CNFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	
R5F21365CNFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CNFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CNFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACNFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CNFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CNFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CNFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CNFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CNFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACNFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CNFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CNFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CNFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CNFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CNFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACNFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCNFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		
R5F21364CNXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	Factory programming product (1)
R5F21365CNXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CNXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CNXXXFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CNXXXFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACNXXXFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCNXXXFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CNXXXFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CNXXXFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CNXXXFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CNXXXFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CNXXXFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACNXXXFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCNXXXFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CNXXXFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CNXXXFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CNXXXFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CNXXXFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CNXXXFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACNXXXFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCNXXXFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		

(D): Under development

Note:

1. The user ROM is programmed before shipment.

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

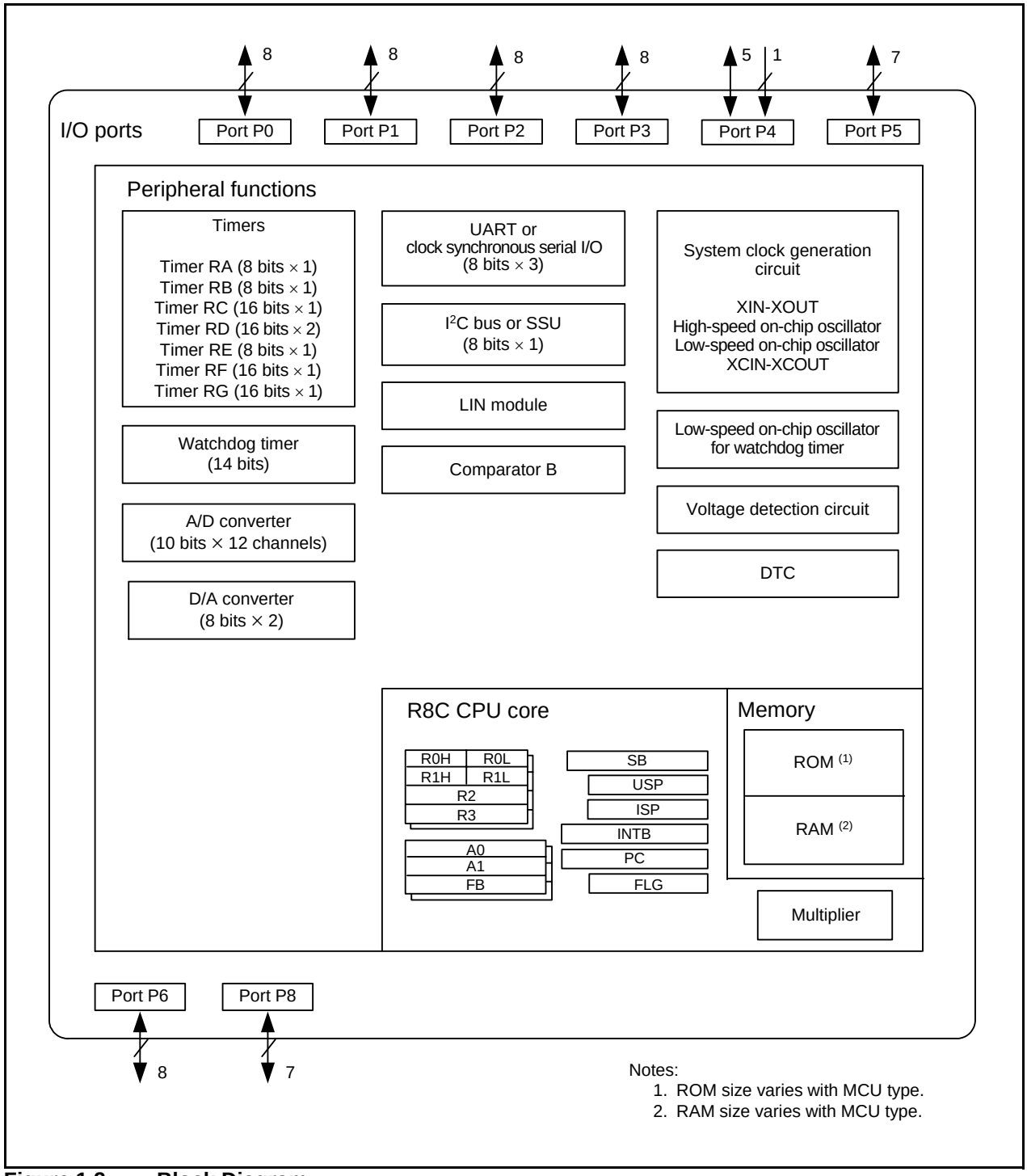


Figure 1.2 Block Diagram

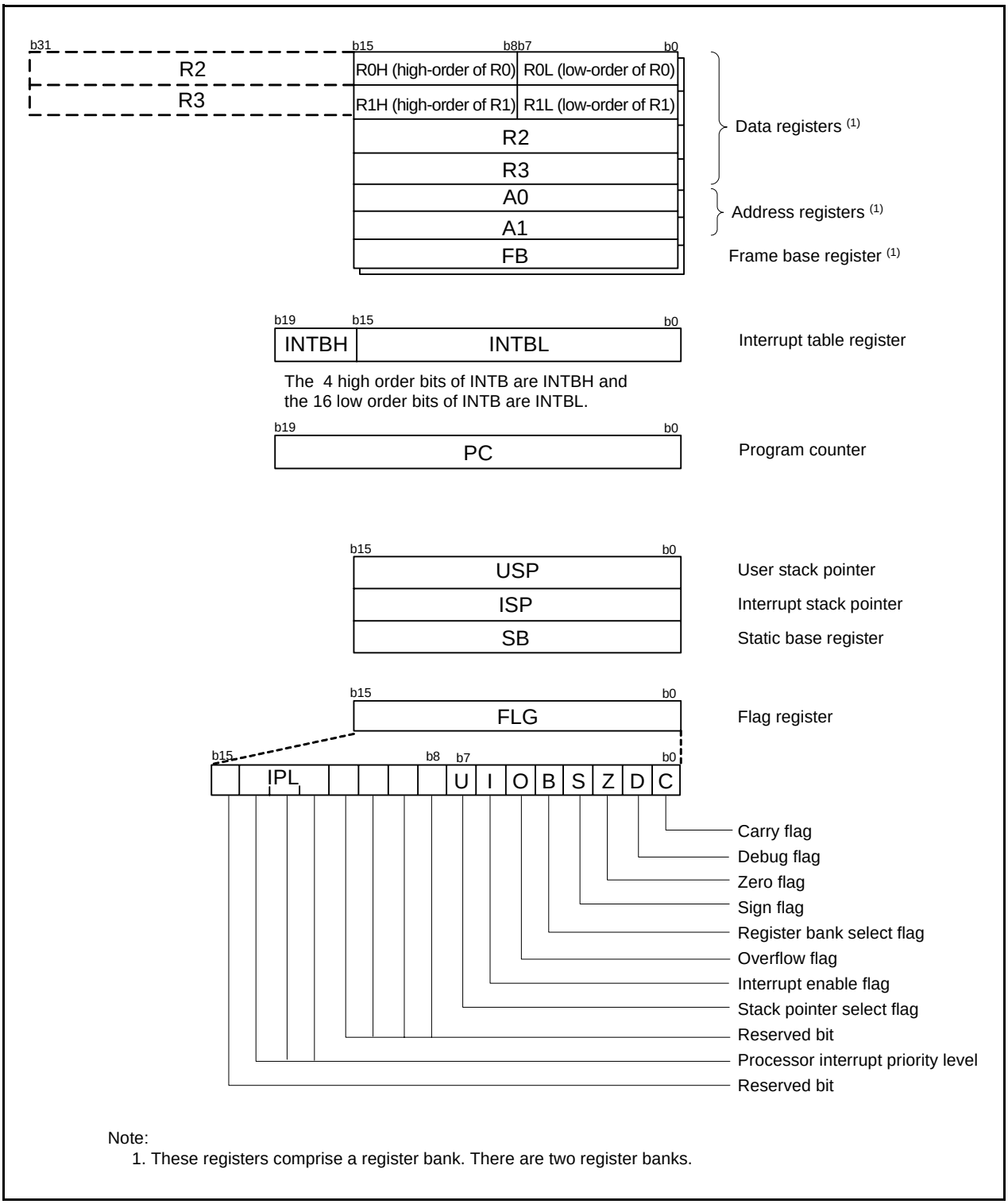
Table 1.8 Pin Functions (2)

Item	Pin Name	I/O Type	Description
SSU	SSI	I/O	Data I/O pin.
	$\overline{SCS}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter.
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter.
	$\overline{ADTRG}$	I	AD external trigger input pin.
D/A converter	DA0, DA1	O	D/A converter output pins.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_4, P5_6, P5_7, P6_0 to P6_7, P8_0 to P8_6	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port.

I: Input O: Output I/O: Input and output

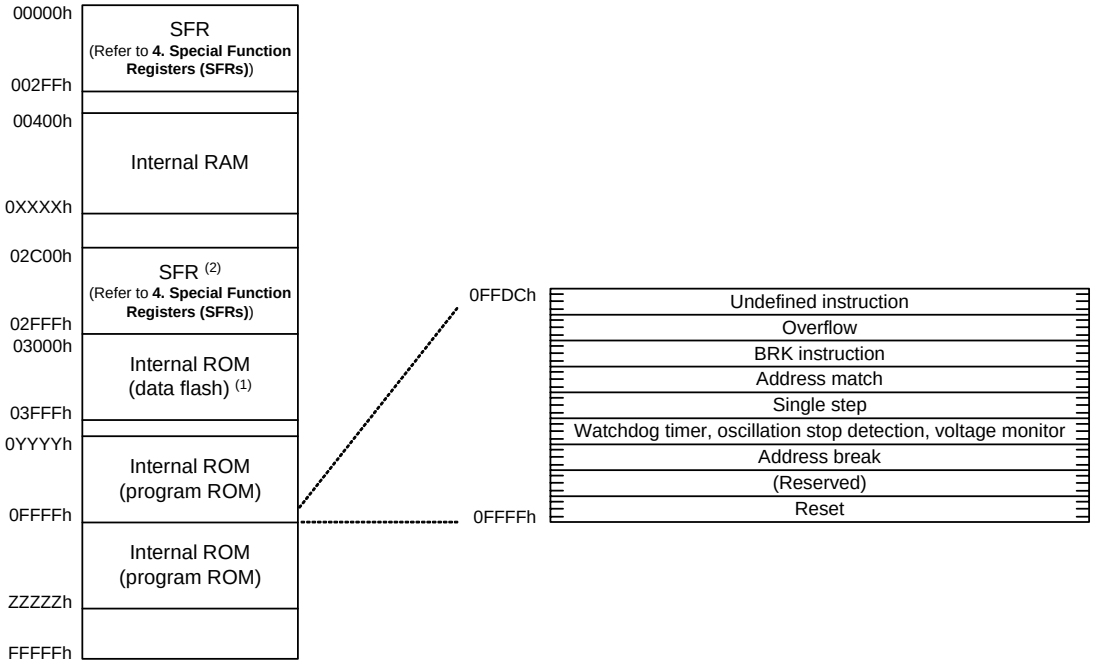
2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers



Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21364CNFP, R5F21364CDFP, R5F21364CNFA, R5F21364CDFA, R5F21364CNFB, R5F21364CDFB, R5F21364CNXXXFP, R5F21364CDXXXFP, R5F21364CNXXXFA, R5F21364CDXXXFA, R5F21364CNXXXFB, R5F21364CDXXXFB	16 Kbytes	0C000h	–	1.5 Kbytes	009FFh
R5F21365CNFP, R5F21365CDFP, R5F21365CNFA, R5F21365CDFA, R5F21365CNFB, R5F21365CDFB, R5F21365CNXXXFP, R5F21365CDXXXFP, R5F21365CNXXXFA, R5F21365CDXXXFA, R5F21365CNXXXFB, R5F21365CDXXXFB	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21366CNFP, R5F21366CDFP, R5F21366CNFA, R5F21366CDFA, R5F21366CNFB, R5F21366CDFB, R5F21366CNXXXFP, R5F21366CDXXXFP, R5F21366CNXXXFA, R5F21366CDXXXFA, R5F21366CNXXXFB, R5F21366CDXXXFB	32 Kbytes	08000h	–	2.5 Kbytes	00DFFh
R5F21367CNFP, R5F21367CDFP, R5F21367CNFA, R5F21367CDFA, R5F21367CNFB, R5F21367CDFB, R5F21367CNXXXFP, R5F21367CDXXXFP, R5F21367CNXXXFA, R5F21367CDXXXFA, R5F21367CNXXXFB, R5F21367CDXXXFB	48 Kbytes	04000h	–	4 Kbytes	013FFh
R5F21368CNFP, R5F21368CDFP, R5F21368CNFA, R5F21368CDFA, R5F21368CNFB, R5F21368CDFB, R5F21368CNXXXFP, R5F21368CDXXXFP, R5F21368CNXXXFA, R5F21368CDXXXFA, R5F21368CNXXXFB, R5F21368CDXXXFB	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2136ACNFP, R5F2136ACDFP, R5F2136ACNFA, R5F2136ACDFA, R5F2136ACNFB, R5F2136ACDFB, R5F2136ACNXXXFP, R5F2136ACDXXXFP, R5F2136ACNXXXFA, R5F2136ACDXXXFA, R5F2136ACNXXXFB, R5F2136ACDXXXFB	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2136CCNFP, R5F2136CCDFP, R5F2136CCNFA, R5F2136CCDFA, R5F2136CCNFB, R5F2136CCDFB, R5F2136CCNXXXFP, R5F2136CCDXXXFP, R5F2136CCNXXXFA, R5F2136CCDXXXFA, R5F2136CCNXXXFB, R5F2136CCDXXXFB	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map of R8C/36C Group

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h	Port P8 Register	P8	XXh
00F1h			
00F2h	Port P8 Direction Register	PD8	00h
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		−0.3 to 6.5	V
V_I	Input voltage		−0.3 to V_{CC} + 0.3	V
V_O	Output voltage		−0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	−40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		−20 to 85 (N version)/ −40 to 85 (D version)	°C
T_{stg}	Storage temperature		−65 to 150	°C

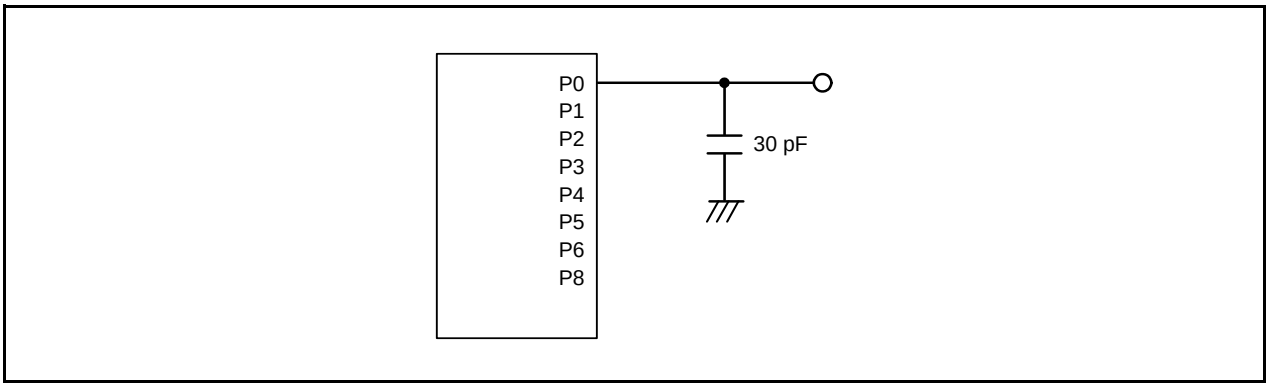


Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AV_{CC}		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
I_{Vref}	V_{ref} current		V_{CC} = 5.0 V, XIN = f1 = ϕAD = 20 MHz		—	45	—	µA
V_{ref}	Reference voltage				2.2	—	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.15 Timing Requirements of Synchronous Serial Communication Unit (SSU)

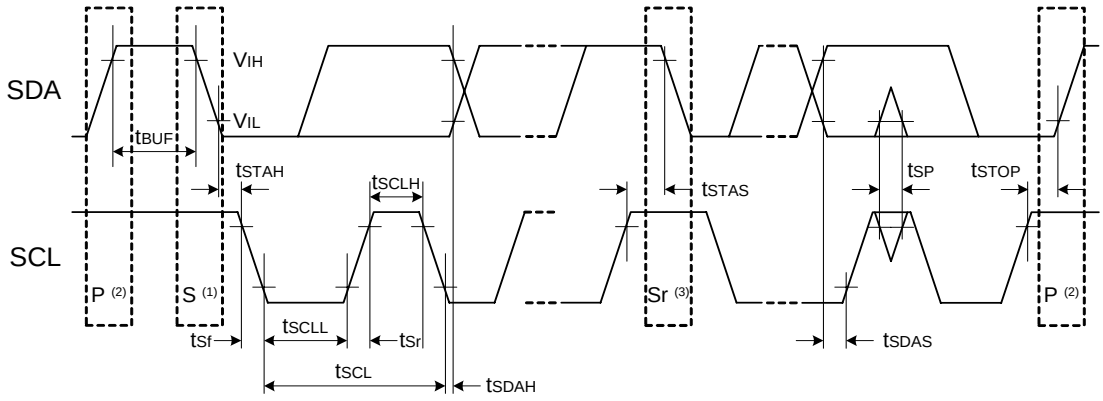
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

Table 5.16 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

Table 5.18 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	—	85	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	—	47	—	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Table 5.24 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRFI, TRGIOA, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO	V_{CC} = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	V_{CC} = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V, T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), and f(XIN) = 10 MHz, unless otherwise specified.

Table 5.29 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input “H” width	150	—	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 2

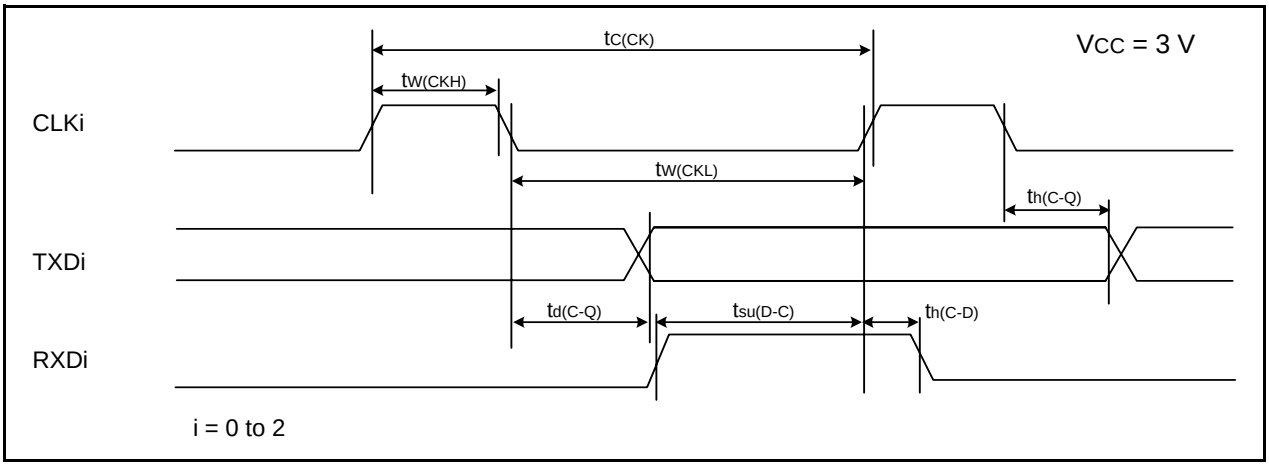


Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.30 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

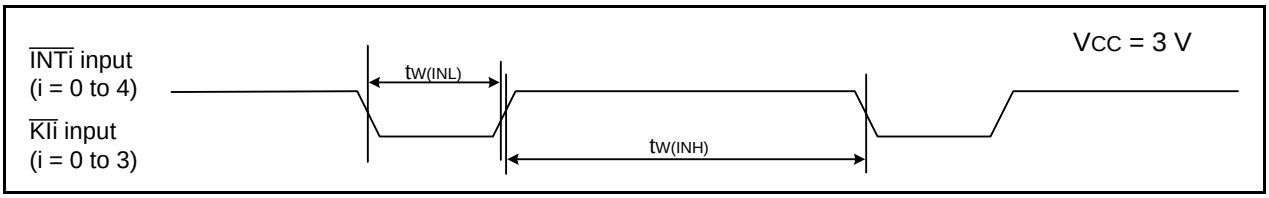


Figure 5.17 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Timing requirements (Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 5.33 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	—	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	—	µs

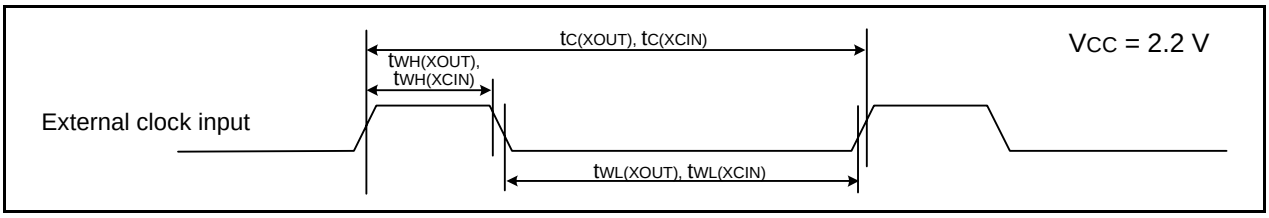


Figure 5.18 External Clock Input Timing Diagram when VCC = 2.2 V

Table 5.34 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

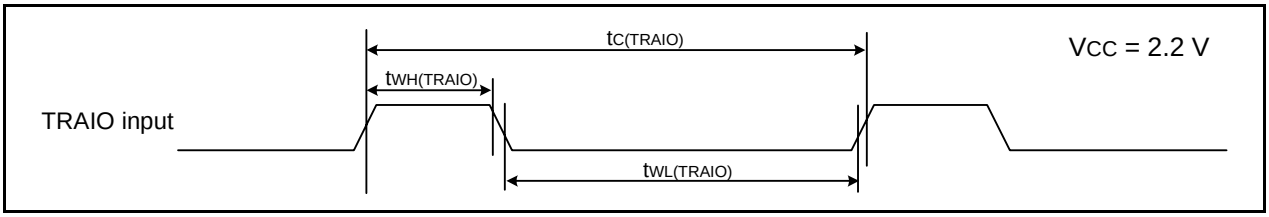


Figure 5.19 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.35 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	2000 (1)	—	ns
$t_{WH(TRFI)}$	TRFI input “H” width	1000 (2)	—	ns
$t_{WL(TRFI)}$	TRFI input “L” width	1000 (2)	—	ns

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

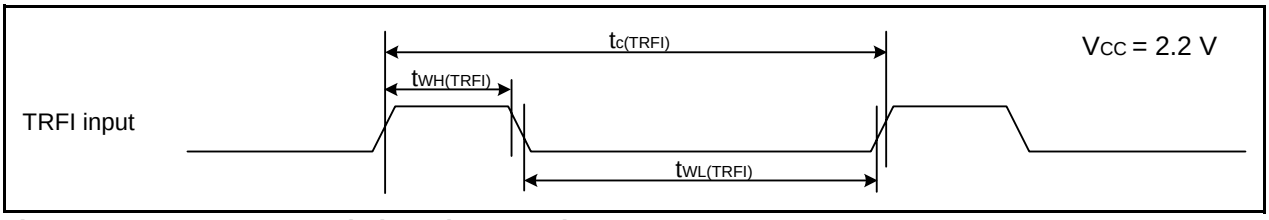
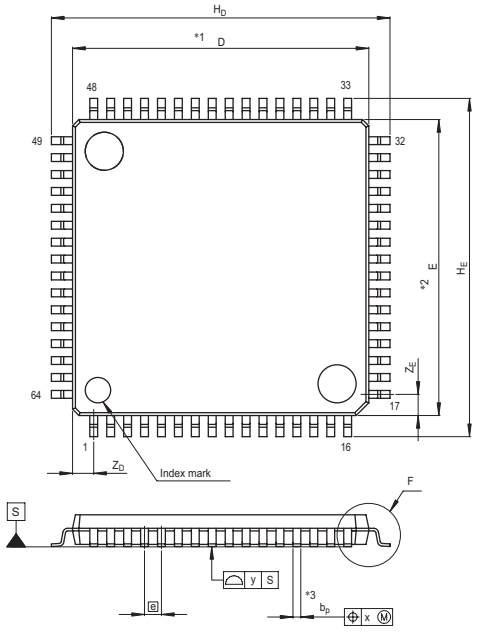
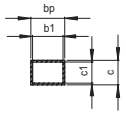


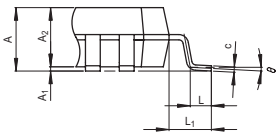
Figure 5.20 TRFI Input Timing Diagram when Vcc = 2.2 V

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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