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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	59
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21367cdfp-v0

Table 1.2 Specifications for R8C/36C Group (2)

Item	Function	Specification
Timer	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 (with 2 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channel
	UART2	Clock synchronous serial I/O, UART, I ² C mode (I ² C bus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I ² C bus)
I ² C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution × 2 circuits
Comparator B		2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current consumption		Typ. 7.0 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		−20 to 85°C (N version) −40 to 85°C (D version) ⁽¹⁾
Package		64-pin LQFP • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin TQFP • Package code: PTQP0064LB-A

Note:

1. Specify the D version if D version functions are to be used.

Table 1.4 Product List for R8C/36C Group (2)

Current of Nov 2010

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F21364CDFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	D version	
R5F21365CDFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CDFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CDFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CDFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACDFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CDFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CDFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CDFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CDFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CDFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACDFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CDFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CDFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CDFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CDFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CDFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACDFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCDFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		
R5F21364CDXXXFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064KB-A	N version	Factory programming product
R5F21365CDXXXFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064KB-A		
R5F21366CDXXXFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064KB-A		
R5F21367CDXXXFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064KB-A		
R5F21368CDXXXFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A		
R5F2136ACDXXXFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A		
R5F2136CCDXXXFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A		
R5F21364CDXXXFA	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0064GA-A		
R5F21365CDXXXFA	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0064GA-A		
R5F21366CDXXXFA	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0064GA-A		
R5F21367CDXXXFA	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0064GA-A		
R5F21368CDXXXFA	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A		
R5F2136ACDXXXFA	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A		
R5F2136CCDXXXFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A		
R5F21364CDXXXFB (D)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PTQP0064LB-A		
R5F21365CDXXXFB (D)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PTQP0064LB-A		
R5F21366CDXXXFB (D)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PTQP0064LB-A		
R5F21367CDXXXFB (D)	48 Kbytes	1 Kbyte × 4	4 Kbytes	PTQP0064LB-A		
R5F21368CDXXXFB (D)	64 Kbytes	1 Kbyte × 4	6 Kbytes	PTQP0064LB-A		
R5F2136ACDXXXFB (D)	96 Kbytes	1 Kbyte × 4	8 Kbytes	PTQP0064LB-A		
R5F2136CCDXXXFB (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PTQP0064LB-A		

(D): Under development

Note:

1. The user ROM is programmed before shipment.

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. ⁽¹⁾ To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
INT interrupt input	INT0 to INT4	I	INT interrupt input pins.
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRA0	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTR	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIO, TRCIOD	I/O	Timer RC I/O pins.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	O	Divided clock output pin.
Timer RF	TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12	O	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pins.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins.
	RXD0, RXD1, RXD2	I	Serial data input pins.
	TXD0, TXD1, TXD2	O	Serial data output pins.
	CTS2	I	Transmission control input pin.
	RTS2	O	Reception control output pin.
	SCL2	I/O	I ² C mode clock I/O pin.
	SDA2	I/O	I ² C mode data I/O pin.

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

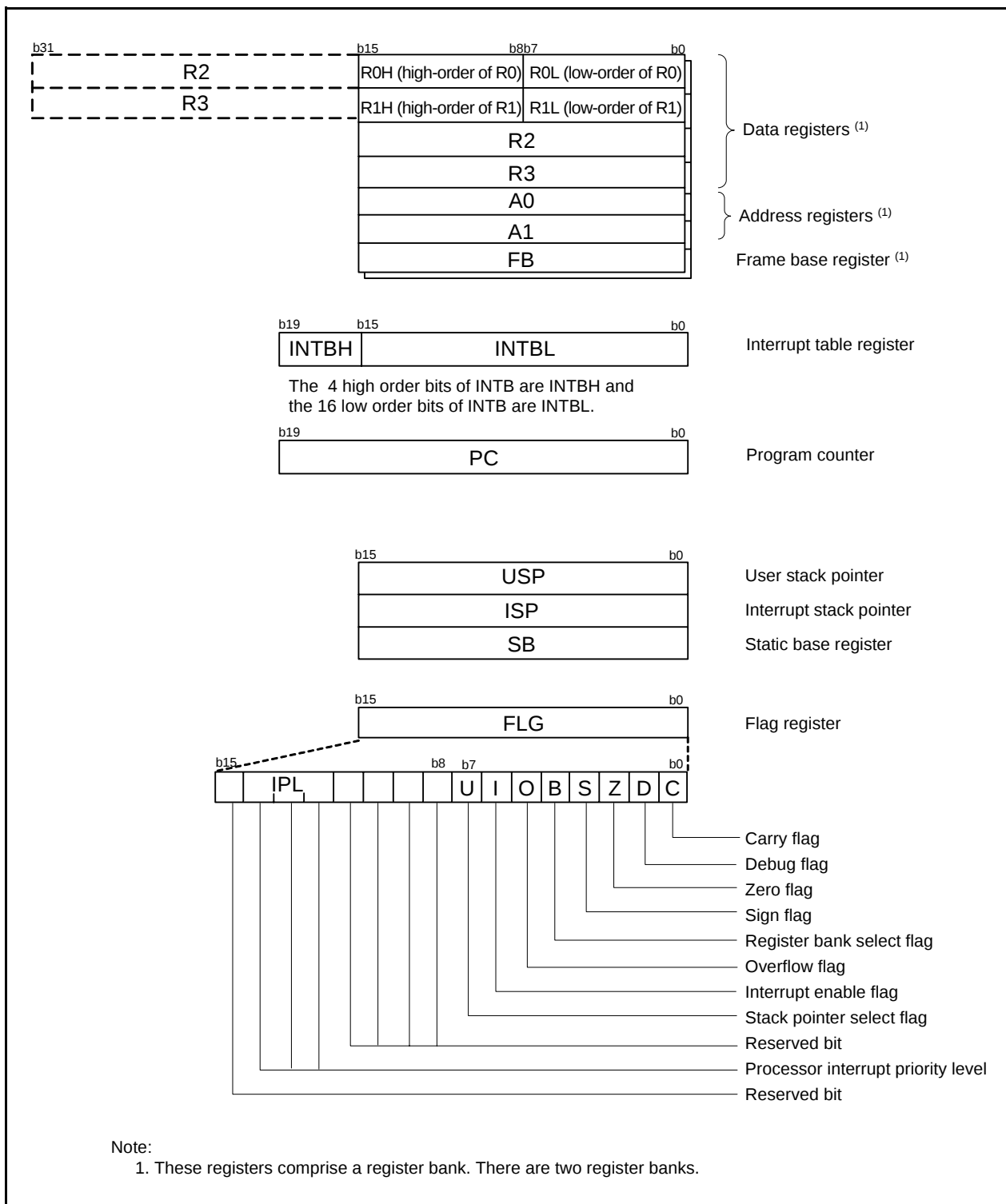


Figure 2.1 CPU Registers

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) ⁽¹⁾

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb ⁽²⁾
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTs	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽³⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h ⁽⁴⁾ 00100000b ⁽⁵⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽⁴⁾ 1100X011b ⁽⁵⁾
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) ⁽¹⁾

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h	Timer RF Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Timer RF Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			XXh
00A9h	UART2 Transmit/Receive Mode Register	U2MR	00h
00AAh	UART2 Bit Rate Register	U2BRG	XXh
00ABh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) ⁽¹⁾

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h			XXh
00C3h	A/D Register 1	AD1	000000XXb
00C4h			XXh
00C5h			000000XXb
00C6h	A/D Register 2	AD2	XXh
00C7h			000000XXb
00C8h			XXh
00C9h	A/D Register 3	AD3	000000XXb
00CAh			XXh
00CBh			000000XXb
00CCh	A/D Register 4	AD4	XXh
00CDh			000000XXb
00CEh			XXh
00CFh	A/D Register 5	AD5	000000XXb
00D0h			XXh
00D1h			000000XXb
00D2h	A/D Register 6	AD6	XXh
00D3h			000000XXb
00D4h			XXh
00D5h	A/D Register 7	AD7	000000XXb
00D6h			XXh
00D7h			000000XXb
00D8h	A/D Mode Register	ADMOD	00h
00D9h			11000000b
00DAh			00h
00DBh	A/D Input Select Register	ADINSEL	00h
00DCh			00h
00DDh			00h
00DEh	A/D Control Register 0	ADCON0	00h
00DFh			00h
00E0h			00h
00E1h	A/D Control Register 1	ADCON1	00h
00E2h			00h
00E3h			00h
00E4h	D/A0 Register	DA0	00h
00E5h			00h
00E6h			00h
00E7h	D/A1 Register	DA1	00h
00E8h			00h
00E9h			00h
00EAh	D/A Control Register	DACON	00h
00EBh			00h
00ECh			00h
00EDh	Port P0 Register	P0	XXh
00EEh			XXh
00EFh			00h
00F0h	Port P1 Register	P1	XXh
00F1h			00h
00F2h			00h
00F3h	Port P0 Direction Register	PD0	00h
00F4h			00h
00F5h			00h
00F6h	Port P1 Direction Register	PD1	00h
00F7h			00h
00F8h			00h
00F9h	Port P2 Register	P2	XXh
00FAh			XXh
00FBh			00h
00FCh	Port P3 Register	P3	XXh
00FDh			XXh
00FEh			00h
00FFh	Port P2 Direction Register	PD2	00h
			00h
			00h
	Port P3 Direction Register	PD3	00h
			00h
			00h
	Port P4 Register	P4	XXh
			XXh
			00h
	Port P5 Register	P5	XXh
			XXh
			00h
	Port P4 Direction Register	PD4	00h
			00h
			00h
	Port P5 Direction Register	PD5	00h
			00h
			00h
	Port P6 Register	P6	XXh
			XXh
			00h
	Port P6 Direction Register	PD6	00h
			00h
			00h
	Port P8 Register	P8	XXh
			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
⋮			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
⋮			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
⋮			
FFDFh	ID1		(Note 2)
⋮			
FFE3h	ID2		(Note 2)
⋮			
FFEBh	ID3		(Note 2)
⋮			
FFEFh	ID4		(Note 2)
⋮			
FFF3h	ID5		(Note 2)
⋮			
FFF7h	ID6		(Note 2)
⋮			
FFFBh	ID7		(Note 2)
⋮			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		Vref = AVCC		—	—	10	Bit
—	Absolute accuracy	10-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	Vref = AVCC = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			Vref = AVCC = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
φAD	A/D conversion clock		4.0 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ Vref = AVCC ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
tCONV	Conversion time	10-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
		8-bit mode	Vref = AVCC = 5.0 V, φAD = 20 MHz		2.2	—	—	μs
tsAMP	Sampling time		φAD = 20 MHz		0.8	—	—	μs
Ivref	Vref current		Vcc = 5.0 V, XIN = f1 = φAD = 20 MHz		—	45	—	μA
Vref	Reference voltage				2.2	—	AVCC	V
VIA	Analog input voltage (3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ φAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2\text{ to }5.5\text{ V}$, $V_{SS} = 0\text{ V}$, and $T_{opr} = -20\text{ to }85\text{ }^{\circ}\text{C}$ (N version)/ $-40\text{ to }85\text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
- The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$k\Omega$
I_{vref}	Reference power input current	(Note 2)	—	—	1.5	mA

Notes:

1. $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAi register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_i	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽²⁾	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Notes:

1. $V_{CC} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85 °C (N version)/ -40 to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 5.7 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		−20 ⁽⁷⁾	—	85	°C
—	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 5.5 V and T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. −40 °C for D version.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

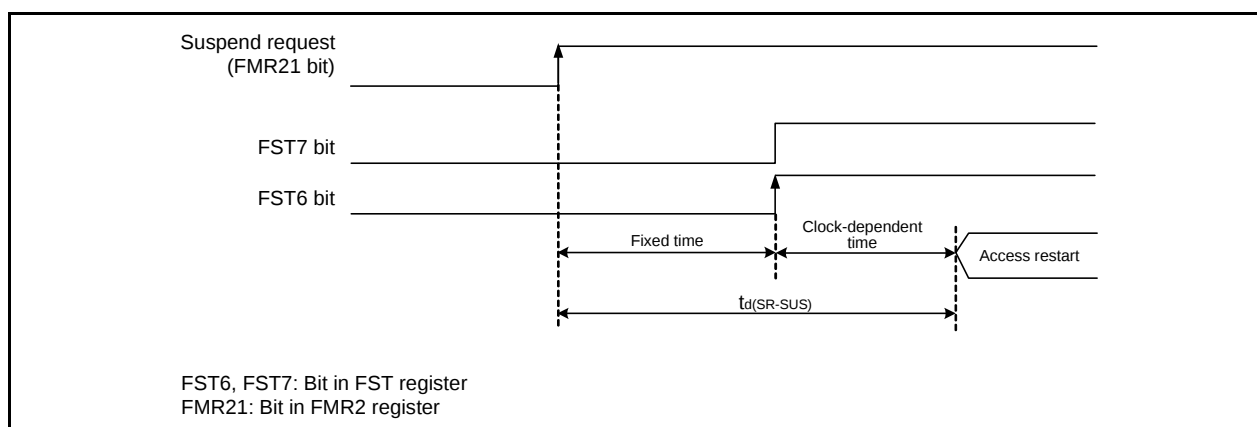
**Figure 5.2 Time delay until Suspend**

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0	At the falling of Vcc	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts (3)		—	—	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient	(1)	0	—	50,000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85 °C (N version)/–40 to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

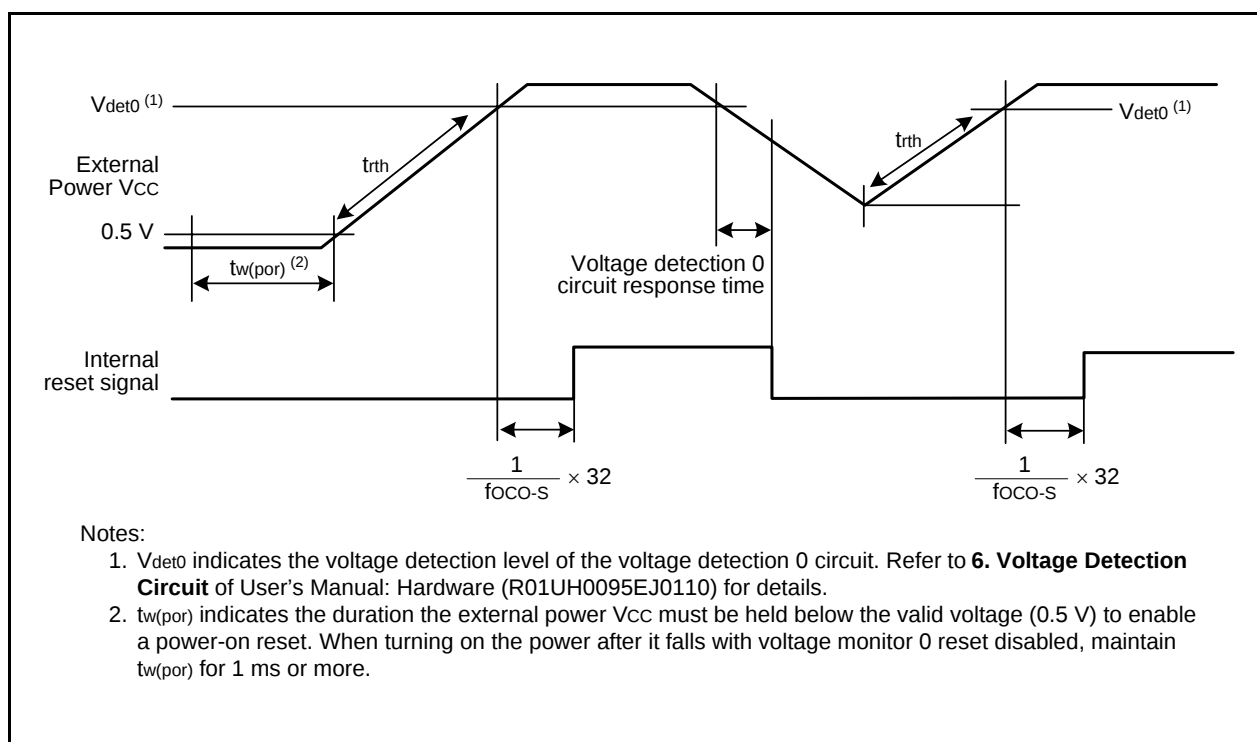
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.12 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	38.4	40	41.6	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	38.0	40	42.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register ⁽²⁾	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	35.389	36.864	38.338	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	35.020	36.864	38.707	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-20 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	30.72	32	33.28	MHz
		$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ $-40 \text{ }^{\circ}\text{C} \leq T_{opr} \leq 85 \text{ }^{\circ}\text{C}$	30.40	32	33.60	MHz
—	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	0.5	3	ms
—	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	400	—	μA

Notes:

1. $V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to $85 \text{ }^{\circ}\text{C}$ (N version)/ -40 to $85 \text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 5.13 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	30	100	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25 \text{ }^{\circ}\text{C}$	—	2	—	μA

Note:

1. $V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to $85 \text{ }^{\circ}\text{C}$ (N version)/ -40 to $85 \text{ }^{\circ}\text{C}$ (D version), unless otherwise specified.

Table 5.14 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on ⁽²⁾		—	—	2,000	μs

Notes:

1. The measurement condition is $V_{CC} = 1.8$ to 5.5 V and $T_{opr} = 25 \text{ }^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.15 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	—	—	tcyc (2)
tHI	SSCK clock "H" width			0.4	—	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	—	0.6	tsucyc
tRISE	SSCK clock rising time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tFALL	SSCK clock falling time	Master		—	—	1	tcyc (2)
		Slave		—	—	1	μs
tsu	SSO, SSI data input setup time			100	—	—	ns
tH	SSO, SSI data input hold time			1	—	—	tcyc (2)
tLEAD	SCS setup time	Slave		1tcyc + 50	—	—	ns
tLAG	SCS hold time	Slave		1tcyc + 50	—	—	ns
tOD	SSO, SSI data output delay time			—	—	1	tcyc (2)
tsA	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns
toR	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5tcyc + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5tcyc + 200	ns

Notes:

1. Vcc = 1.8 to 5.5 V, Vss = 0 V, and T_{opr} = −20 to 85 °C (N version)/−40 to 85 °C (D version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

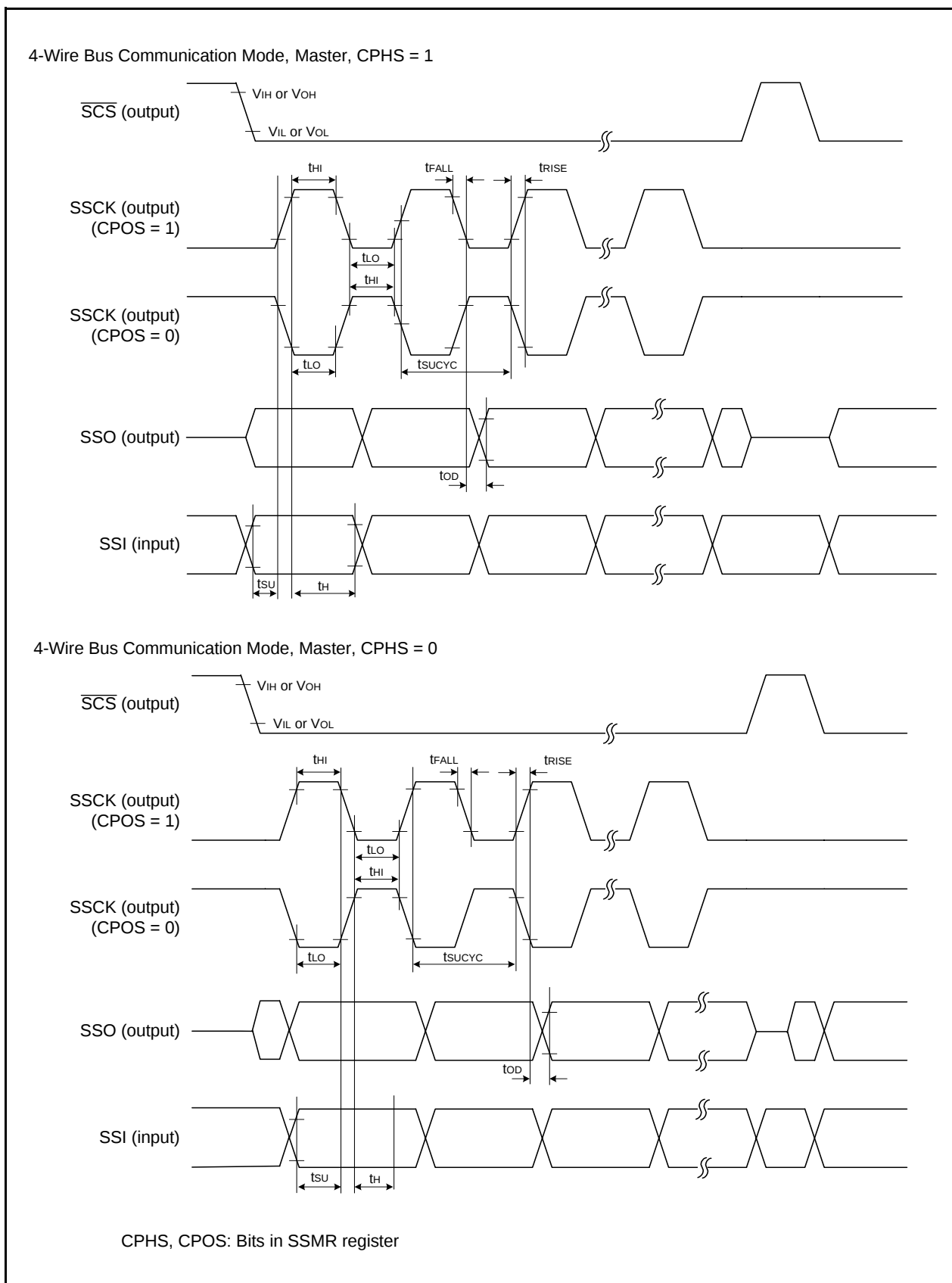


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

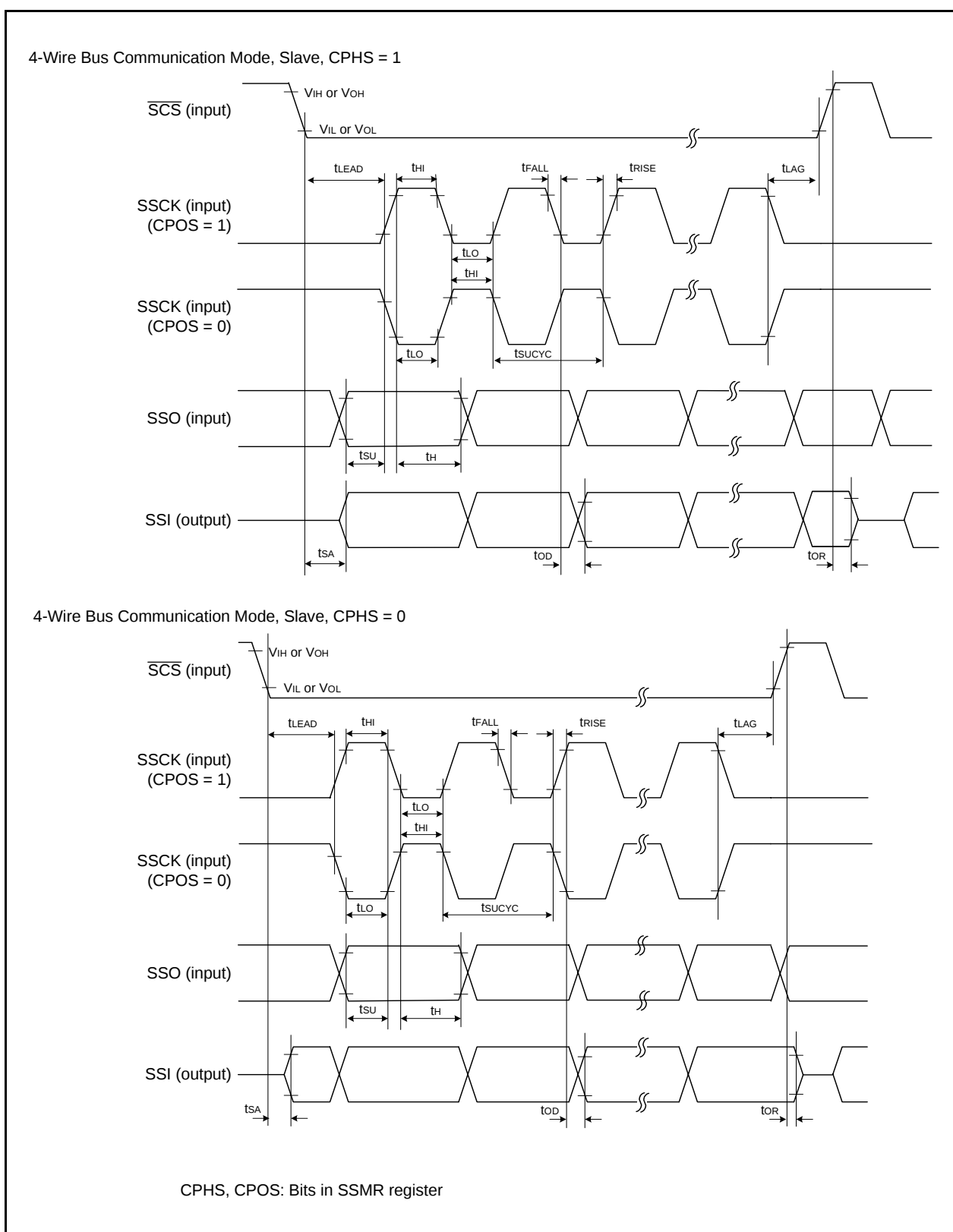


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

NOTE)

1. DIMENSIONS **1" AND "**2"
2. DO NOT INCLUDE MOLD FLASH.
3. DIMENSION "**3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A ₂	—	1.4	—
H _D	11.8	12.0	12.2
H _E	11.8	12.0	12.2
A	—	—	1.7
A ₁	0.05	0.1	0.15
b _p	0.15	0.20	0.25
b ₁	—	0.18	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
⌀	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z _D	—	1.25	—
Z _E	—	1.25	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

